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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300c4s
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Security; SEC 3.0
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 125°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	689-BBGA Exposed Pad
Supplier Device Package	689-TEPBGA II (31x31)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8377evranga

1.12 Enhanced Secured Digital Host Controller (eSDHC)

The enhanced SD host controller (eSDHC) has the following features:

- Conforms to *SD Host Controller Standard Specification, Rev 2.0* with Test Event register support.
- Compatible with the *MMC System Specification, Rev 4.0*
- Compatible with the *SD Memory Card Specification, Rev 2.0*, and supports High Capacity SD memory cards
- Compatible with the *SDIO Card Specification Rev, 1.2*
- Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC*plus*, MMC 4x, and RS-MMC cards
- SD bus clock frequency up to 50 MHz
- Supports 1-/4-bit SD and SDIO modes, 1-/4-bit MMC modes
- Supports internal DMA capabilities

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the chip. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Characteristic	Symbol	Max Value	Unit	Note
Core supply voltage	V_{DD}	–0.3 to 1.1	V	—
PLL supply voltage (e300 core, eLBC, and system)	AV_{DD}	–0.3 to 1.1	V	—
DDR1 and DDR2 DRAM I/O voltage	GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
Three-speed Ethernet I/O, MII management voltage	LV_{DD}[1,2]	–0.3 to 3.63	V	—
PCI, DUART, system control and power management, I^2C, and JTAG I/O voltage	OV_{DD}	–0.3 to 3.63	V	—
Local bus	LBV_{DD}	–0.3 to 3.63	V	—
SerDes	L[1,2]_nV_{DD}	–0.3 to 1.1	V	6

voltage supplies—GV_{DD}, LV_{DD}, and OV_{DD}—do not have any ordering requirements with respect to one another.

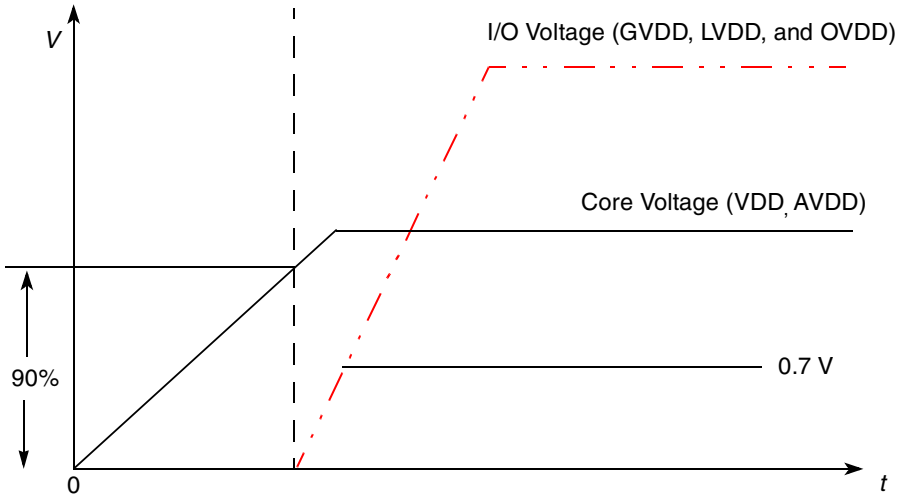

Figure 3. Power-Up Sequencing Example

Note that the SerDes power supply (L[1,2]_$n$$V_{DD}$) should follow the same timing as the core supply (V_{DD}).

The device does not require the core supply voltage and I/O supply voltages to be powered down in any particular order.

3 Power Characteristics

The estimated typical power dissipation for the chip device is shown in this table.

Table 5. Power Dissipation [1]

Core Frequency (MHz)	CSB/DDR Frequency (MHz)	Sleep Power at T_j = 65°C (W) [2]	Typical Application at T_j = 65°C (W) [2]	Typical Application at T_j = 125°C (W) [3]	Max Application at T_j = 125°C (W) [4]
333	333	1.45	1.9	3.2	3.8
	167	1.45	1.8	3.0	3.6
400	400	1.45	2.0	3.3	4.0
	266	1.45	1.9	3.1	3.8
450	300	1.45	2.0	3.2	3.8
	225	1.45	1.9	3.1	3.7
500	333	1.45	2.0	3.3	3.9
	250	1.45	1.9	3.2	3.8
533	355	1.45	2.0	3.3	4.0
	266	1.45	2.0	3.2	3.9

4.3 eTSEC Gigabit Reference Clock Timing

This table provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications.

Table 9. EC_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
EC_GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK rise and fall time LV_{DD} = 2.5 V LV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 47	—	 53	%	2
EC_GTX_CLK125 jitter	—	—	—	±150	ps	2

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. The EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.2, "RGMII and RTBI AC Timing Specifications," for the duty cycle for 10Base-T and 100Base-T reference clock.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the chip.

5.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins of the device.

Table 10. RESET Pins DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	± 30	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:

- This table applies for pins $\overline{\text{PORESET}}$ and $\overline{\text{HRESET}}$. The $\overline{\text{PORESET}}$ is input pin, thus stated output voltages are not relevant.
- $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are open drain pin, thus V_{OH} is not relevant for these pins.

5.2 RESET AC Electrical Characteristics

This table provides the reset initialization AC timing specifications of the device.

Table 11. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of $\overline{\text{HRESET}}$ to activate reset flow	32	—	$t_{PCI\_SYNC\_IN}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the device is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_CLK when the device is in PCI agent mode	32	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ negation to negation (output)	16	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR config signals (CFG_RESET_SOURCE[0:3], CFG_CLKIN_DIV, and CFG_LBMUX) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR config signals (CFG_RESET_SOURCE[0:3], CFG_CLKIN_DIV, and CFG_LBMUX) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the device to turn off POR config signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the device to start driving functional output signals multiplexed with the POR configuration signals with respect to the negation of HRESET	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8379E Integrated Host Processor Reference Manual* for more details.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the device is in PCI host mode. See the *MPC8379E Integrated Host Processor Reference Manual* for more details.
3. POR config signals consists of CFG_RESET_SOURCE[0:3], CFG_LBMUX, and CFG_CLKIN_DIV.

Table 12 provides the PLL lock times.

Table 12. PLL Lock Times

Parameter	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

Note:

- The device guarantees the PLL lock if the clock settings are within spec range. The core clock also depends on the core PLL ratio. See Section 23, “Clocking,” for more information.

6 DDR1 and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the chip. Note that DDR1 SDRAM is GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

6.1 DDR1 and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the device when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 5
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.140	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.140	V	—
Output leakage current	I_{OZ}	–50	50	μA	4
Output high current (V_{OUT} = 1.40 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.3 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.
5. See AN3665, “MPC837xE Design Checklist,” for proper DDR termination.

Table 14 provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 14. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) when GV_{DD}(typ) = 2.5 V.

Table 15. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 5
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.18	GV_{DD} + 0.3	V	—

6.2.2 DDR1 and DDR2 SDRAM Output AC Timing Specifications

This table shows the DDR1 and DDR2 SDRAM output AC timing specifications.

Table 21. DDR1 and DDR2 SDRAM Output AC Timing Specifications

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK*n* cycle time, MCK*n*/$\overline{\text{MCK}n}$ crossing	t_{MCK}	5	10	ns	2
ADDR/CMD output setup with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHAS}	 1.95 2.40 3.15 4.20	 — — — —	ns	3, 7
ADDR/CMD output hold with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHAX}	 1.95 2.40 3.15 4.20	 — — — —	ns	3, 7
$\overline{\text{MCS}n}$ output setup with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHCS}	 1.95 2.40 3.15 4.20	 — — — —	ns	3
$\overline{\text{MCS}n}$ output hold with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHCX}	 1.95 2.40 3.15 4.20	 — — — —	ns	3
MCK to MDQS skew	t_{DDKHMH}	–0.6	0.6	ns	4, 8
MDQ//MDM output setup with respect to MDQS 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHDS}, t_{DDKLDS}	 550 800 1100 1200	 — — — —	ps	5, 8
MDQ//MDM output hold with respect to MDQS 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHDX}, t_{DDKLDX}	 700 800 1100 1200	 — — — —	ps	5, 8
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6, 8

Table 22. DUART DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current, (0 V ≤V_{IN} ≤ OV_{DD})	I_{IN}	—	±30	µA

Note: The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2.

7.2 DUART AC Electrical Specifications

this table provides the AC timing parameters for the DUART interface of the device.

Table 23. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	256	baud	—
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate will be limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RGMII/RTBI/RMII DC Electrical Characteristics

The electrical characteristics specified here apply to media independent interface (MII), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), reduced media independent interface (RMII) signals, management data input/output (MDIO) and management data clock (MDC).

The MII and RMII interfaces are defined for 3.3 V, while the RGMII and RTBI interfaces can be operated at 2.5 V. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3*. The RMII interface follows the *RMII Consortium RMII Specification Version 1.2*.

This figure shows the RMII receive AC timing diagram.

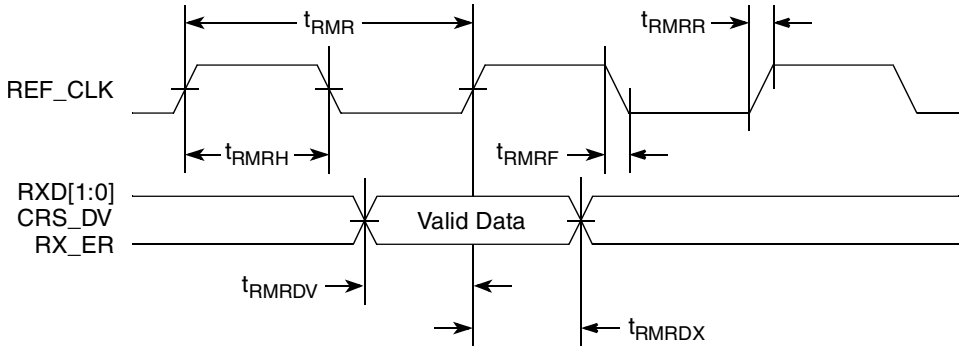

Figure 14. RMII Receive AC Timing Diagram

8.3 Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock).

This figure provides the AC test load for eTSEC.

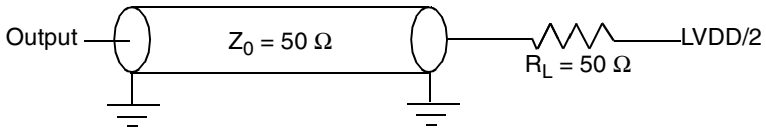

Figure 15. eTSEC AC Test Load

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 2.5 V or 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 31 and Table 32.

Table 31. MII Management DC Electrical Characteristics When Powered at 2.5 V

Parameter	Conditions		Symbol	Min	Max	Unit
Supply voltage (2.5 V)	—		LV_{DD1}	2.37	2.63	V
Output high voltage	I_{OH} = –1.0 mA	LV_{DD1} = Min	V_{OH}	2.00	LV_{DD1} + 0.3	V
Output low voltage	I_{OL} = 1.0 mA	LV_{DD1} = Min	V_{OL}	GND – 0.3	0.40	V
Input high voltage	—	LV_{DD1} = Min	V_{IH}	1.7	—	V
Input low voltage	—	LV_{DD1} = Min	V_{IL}	–0.3	0.70	V
Input high current	V_{IN} = LV_{DD1}		I_{IH}	—	20	μA
Input low current	V_{IN} = LV_{DD1}		I_{IL}	–15	—	μA

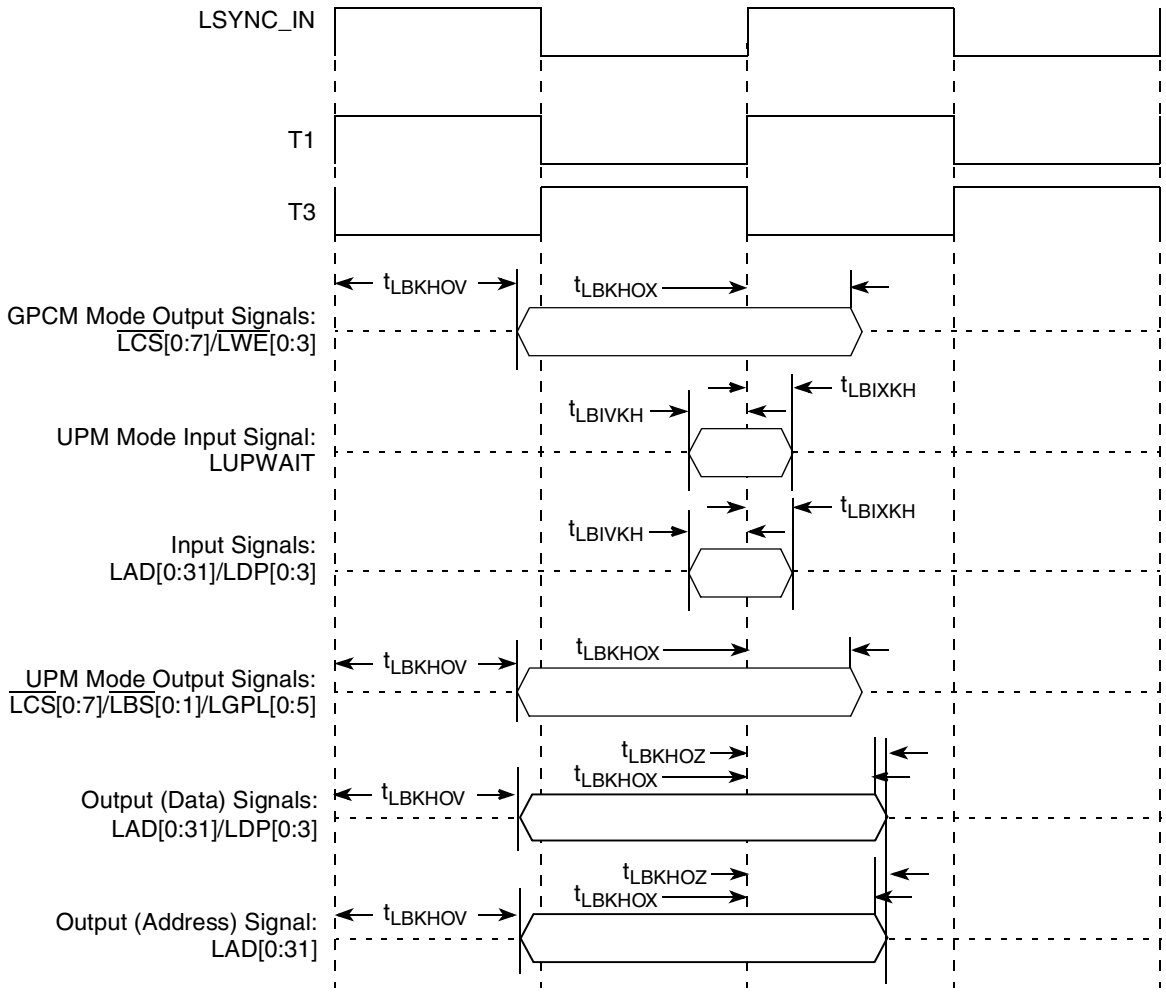

Figure 22. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (PLL Enable Mode)

This figure provides the AC test load for PCI.

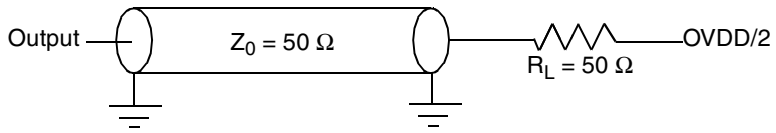

Figure 39. PCI AC Test Load

This figure shows the PCI input AC timing conditions.

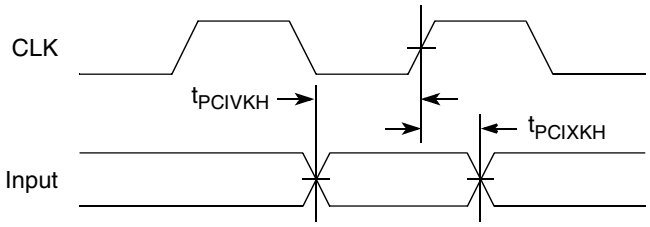

Figure 40. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.

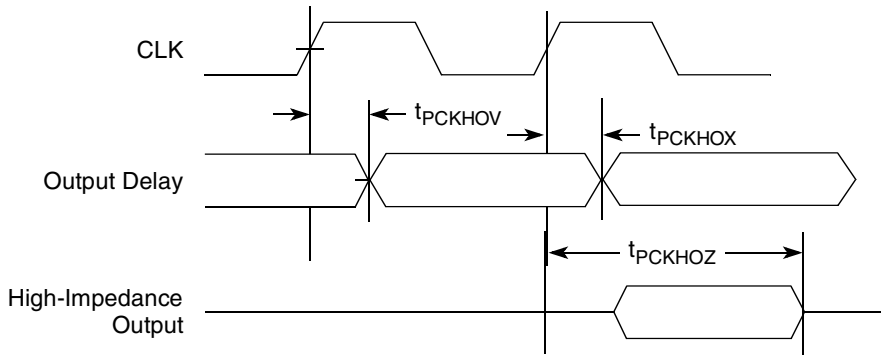

Figure 41. PCI Output AC Timing Measurement Condition

15 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus.

15.1 DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK

For more information see Section 21, “High-Speed Serial Interfaces (HSSI).”

15.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 44.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

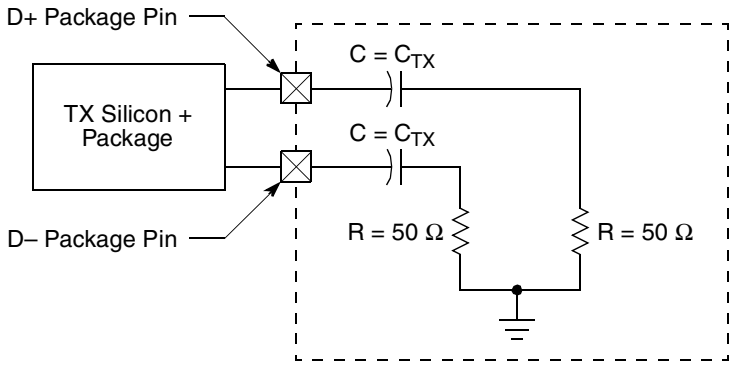

Figure 44. Compliance Test/Measurement Load

16 Serial ATA (SATA)

This section describes the DC and AC electrical specifications for the serial ATA (SATA) of the MPC8377E. Note that the external cabled applications or long backplane applications (Gen1x and Gen2x) are not supported.

16.1 Requirements for SATA REF_CLK

The reference clock is a single ended input clock required for the SATA interface operation. The AC requirements for the SATA reference clock are listed in the Table 54.

Table 54. SATA Reference Clock Input Requirements

Parameter	Condition	Symbol	Min	Typical	Max	Unit	Note
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ frequency range	—	t_{CLK_REF}	—	100/125/150	—	MHz	1
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance	—	t_{CLK_TOL}	–350	0	+350	ppm	—
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle	Measured at 1.6V	t_{CLK_DUTY}	40	50	60	%	—

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen1i or 1.5 Gbits/s transmission.

Table 56. Gen1i/1.5G Transmitter AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Channel speed	t_{CH_SPEED}	—	1.5	—	Gbps	—
Unit interval	T_{UI}	666.4333	666.667	670.2333	ps	—
Total jitter, data-data 5 UI	$U_{SATA\_TXTJ5UI}$	—	—	0.355	UI_{p-p}	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	—	—	0.47	UI_{p-p}	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	—	—	0.175	UI_{p-p}	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ250UI}$	—	—	0.22	UI_{p-p}	1

Note:
1. Measured at Tx output pins peak to peak phase variation, random data pattern.

16.2.2 Gen2i/3G Transmitter Specifications

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission.

Table 57. Gen 2i/3G Transmitter DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Tx differential output voltage	V_{SATA_TXDIFF}	400	550	700	mV_{p-p}	1
Tx differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	—

Note:
1. Terminated by 50 Ω load.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission.

Table 58. Gen 2i/3G Transmitter AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Channel speed	t_{CH_SPEED}	—	3.0	—	Gbps	—
Unit interval	T_{UI}	333.2	333.33	335.11	ps	—
Total jitter $f_{C3dB}=f_{BAUD}/10$	$U_{SATA\_TXTJfB/10}$	—	—	0.3	UI_{p-p}	1
Total jitter $f_{C3dB} = f_{BAUD}/500$	$U_{SATA\_TXTJfB/500}$	—	—	0.37	UI_{p-p}	1

Table 58. Gen 2i/3G Transmitter AC Specifications (continued)

Parameter	Symbol	Min	Typical	Max	Units	Note
Total jitter $f_{C3dB} = f_{BAUD}/1667$	$U_{SATA\_TXTJfB/1667}$	—	—	0.55	UI_{p-p}	1
Deterministic jitter $f_{C3dB} = f_{BAUD}/10$	$U_{SATA\_TXDJfB/10}$	—	—	0.17	UI_{p-p}	1
Deterministic jitter $f_{C3dB} = f_{BAUD}/500$	$U_{SATA\_TXDJfB/500}$	—	—	0.19	UI_{p-p}	1
Deterministic jitter $f_{C3dB} = f_{BAUD}/1667$	$U_{SATA\_TXDJfB/1667}$	—	—	0.35	UI_{p-p}	1

Note:
1. Measured at Tx output pins peak to peak phase variation, random data pattern.

16.3 Differential Receiver (Rx) Input Characteristics

This section discusses the Gen1i/1.5G and Gen2i/3G differential receiver input AC characteristics.

16.3.1 Gen1i/1.5G Receiver Specifications

This table provides the Gen1i or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 59. Gen1i/1.5G Receiver Input DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Differential input voltage	V_{SATA_RXDIFF}	240	500	600	mV_{p-p}	1
Differential Rx input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	—

Note:
1. Voltage relative to common of either signal comprising a differential pair.

This table provides the Gen1i or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface.

Table 60. Gen 1i/1.5G Receiver AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Unit interval	T_{UI}	666.4333	666.667	670.2333	ps	—
Total jitter, data-data 5 UI	$U_{SATA\_TXTJ5UI}$	—	—	0.43	UI_{p-p}	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	—	—	0.60	UI_{p-p}	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	—	—	0.25	UI_{p-p}	1

— The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.

- The maximum average current requirement that also determines the common mode voltage range
  — When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  — This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND_SRDS*n* (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  — If the device driving the SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ inputs cannot drive 50 Ω to SGND_SRDS*n* (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  — This requirement is described in detail in the following sections.

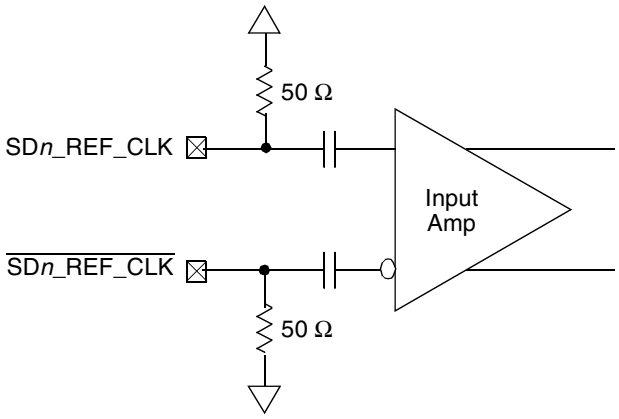

Figure 52. Receiver of SerDes Reference Clocks

21.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the device SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  — The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and

greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

— For **external DC-coupled** connection, as described in Section 21.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 53 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

— For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDS*n*. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDS*n*). Figure 54 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

- **Single-ended Mode**

— The reference clock can also be single-ended. The SD _REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV_{p-p} (from V_{min} to V_{max}) with $\overline{SDn\_REF\_CLK}$ either left unconnected or tied to ground.

— The SD*n*_REF_CLK input average voltage must be between 200 mV and 400 mV. Figure 55 shows the SerDes reference clock input requirement for single-ended signaling mode.

— To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{SDn\_REF\_CLK}$) through the same source impedance as the clock input (SD*n*_REF_CLK) in use.

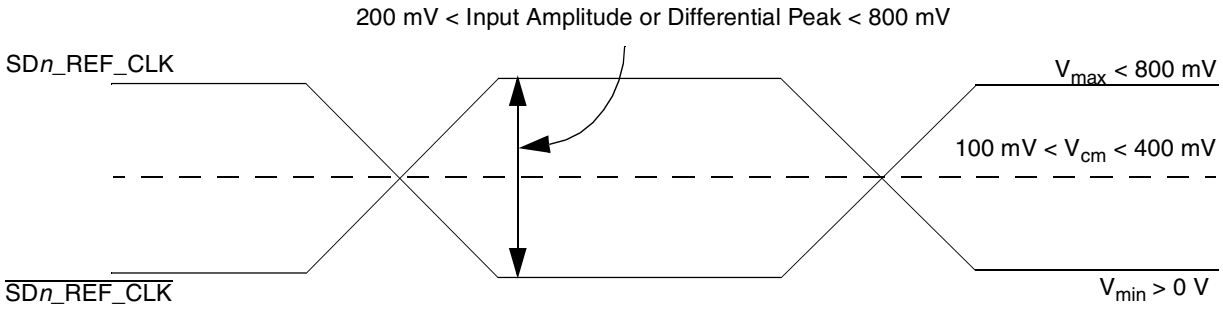

Figure 53. Differential Reference Clock Input DC Requirements (External DC-Coupled)

driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

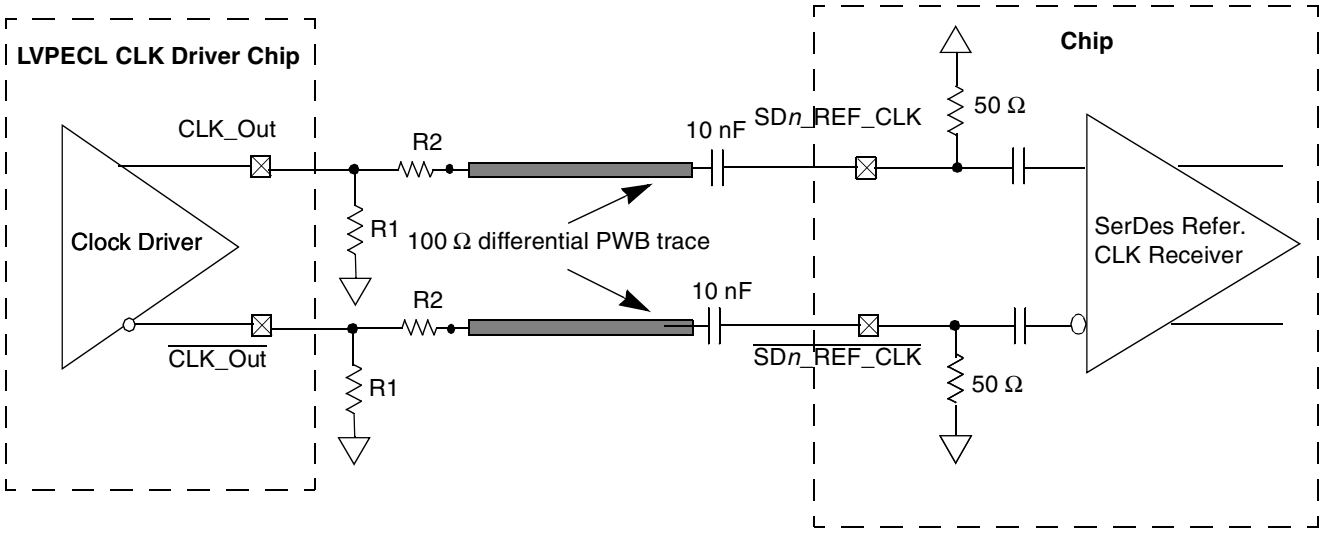

Figure 58. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with device SerDes reference clock input's DC requirement.

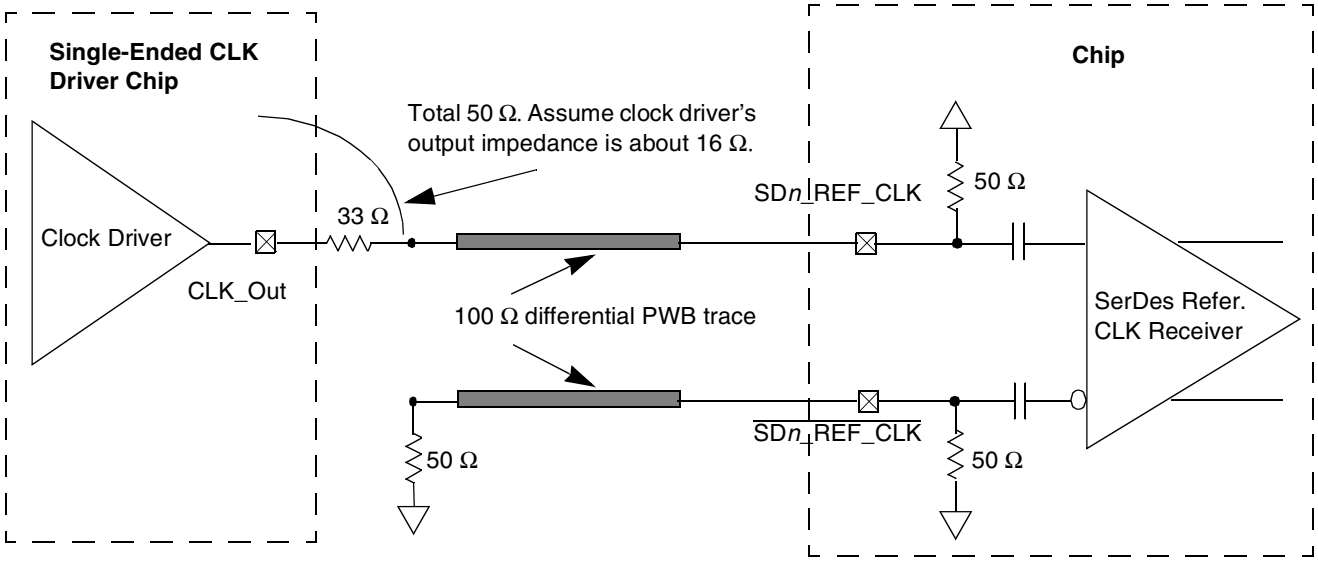

Figure 59. Single-Ended Connection (Reference Only)

21.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 KHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MBA2	M3	O	GVDD	—
MCAS_B	W5	O	GVDD	—
MCK_B0	H1	O	GVDD	—
MCK_B1	K1	O	GVDD	—
MCK_B2	V1	O	GVDD	—
MCK_B3	W2	O	GVDD	—
MCK_B4	AA1	O	GVDD	—
MCK_B5	AB2	O	GVDD	—
MCK0	J1	O	GVDD	—
MCK1	L1	O	GVDD	—
MCK2	V2	O	GVDD	—
MCK3	W1	O	GVDD	—
MCK4	Y1	O	GVDD	—
MCK5	AB1	O	GVDD	—
MCKE0	M4	O	GVDD	3
MCKE1	R5	O	GVDD	3
MCS_B0	W3	O	GVDD	—
MCS_B1	P3	O	GVDD	—
MCS_B2	T4	O	GVDD	—
MCS_B3	R4	O	GVDD	—
MDIC0	AH8	I/O	GVDD	9
MDIC1	AJ8	I/O	GVDD	9
MDM0	B6	O	GVDD	—
MDM1	B2	O	GVDD	—
MDM2	E2	O	GVDD	—
MDM3	E1	O	GVDD	—
MDM4	Y6	O	GVDD	—
MDM5	AC6	O	GVDD	—
MDM6	AE6	O	GVDD	—
MDM7	AJ4	O	GVDD	—
MDM8	L6	O	GVDD	—
MDQ0	A8	I/O	GVDD	11
MDQ1	A6	I/O	GVDD	11

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MDQS4	AB5	I/O	GVDD	11
MDQS5	AD1	I/O	GVDD	11
MDQS6	AH1	I/O	GVDD	11
MDQS7	AJ3	I/O	GVDD	11
MDQS8	G1	I/O	GVDD	11
MECC0/MSRCID0	J6	I/O	GVDD	—
MECC1/MSRCID1	J3	I/O	GVDD	—
MECC2/MSRCID2	K2	I/O	GVDD	—
MECC3/MSRCID3	K3	I/O	GVDD	—
MECC4/MSRCID4	J5	I/O	GVDD	—
MECC5/MDVAL	J2	I/O	GVDD	—
MECC6	L5	I/O	GVDD	—
MECC7	L2	I/O	GVDD	—
MODT0	N5	O	GVDD	6
MODT1	U6	O	GVDD	6
MODT2	M6	O	GVDD	6
MODT3	P6	O	GVDD	6
MRAS_B	AA3	O	GVDD	—
MVREF1	K4	I	GVDD	11
MVREF2	W4	I	GVDD	11
MWE_B	Y2	O	GVDD	—
DUART Interface				
UART_SIN1/ MSRCID2/LSRCID2	L28	I/O	OVDD	—
UART_SOUT1/ MSRCID0/LSRCID0	L27	O	OVDD	—
UART_CTS_B[1]/ MSRCID4/LSRCID4	K26	I/O	OVDD	—
UART_RTS_B1	N27	O	OVDD	—
UART_SIN2/ MSRCID3/LSRCID3	K27	I/O	OVDD	—
UART_SOUT2/ MSRCID1/LSRCID1	K28	O	OVDD	—
UART_CTS_B[2]/ MDVAL/LDVAL	K29	I/O	OVDD	—

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the VDD, OVDD, GVDD, and LVDD planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

25.3 Connection Recommendations

To ensure reliable operation, it is highly recommended that unused inputs be connected to an appropriate signal level. Unused active low inputs should be tied to OVDD, GVDD, or LVDD as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external VDD, GVDD, LVDD, OVDD, and GND pins of the device.

25.4 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OVDD or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 66). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

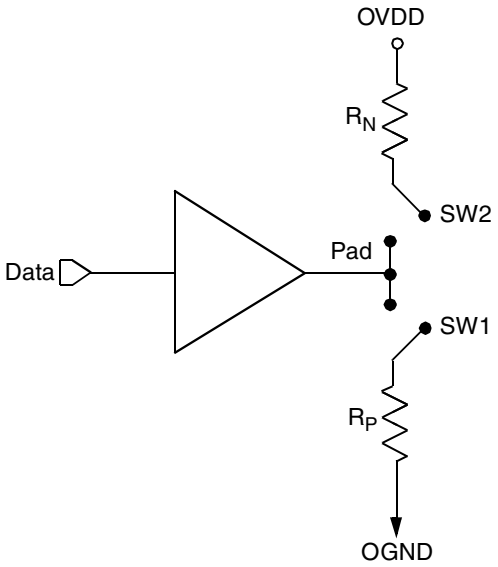

Figure 66. Driver Impedance Measurement

Table 87. Document Revision History (continued)

Revision	Date	Substantive Change(s)
2	10/2009	• In Table 3, “Recommended Operating Conditions,” added “Operating temperature range” values. • In Table 5, “Power Dissipation [1],” corrected maximal application for 800/400 MHz to 4.3 W. • In Table 5, “Power Dissipation [1],” added a column for “Typical Application at T_j = 65°C (W)”. • In Table 5, “Power Dissipation [1],” added a column for “Sleep Power at T_j = 65°C (W)”. • In Table 11, removed overbar from CFG_CLKIN_DIV. • In Table 17, “Current Draw Characteristics for MV_{REF},” updated I_{MVREF} maximum value for both DDR1 and DDR2 to 600 and 400 µA, respectively. Also, updated Note 1 and added Note 2. • In Table 20, “DDR1 and DDR2 SDRAM Input AC Timing Specifications,” column headings renamed to “Min” and “Max”. Footnote 2 updated to state “T is the MCK clock period”. • In Table 20, “DDR1 and DDR2 SDRAM Input AC Timing Specifications,” and Table 21, “DDR1 and DDR2 SDRAM Output AC Timing Specifications,” clarified that the frequency parameters are data rates. • In Table 29, “RMII Transmit AC Timing Specifications,” updated t_{RMTDX}I to 2.0 ns. • In Table 60, Gen 1i/1.5G Transmitter AC Specifications,” and Table 62, Gen 2i/3G Transmitter AC Specifications,” corrected titles from “Transmitter” to “Receiver”. • In Table 72, “TePBGA II Pinout Listing,” removed pin THERM0; it is now Reserved. Also added 1.05 V to VDD pin. • In Table 74, “Operating Frequencies for TePBGA II,” corrected “DDR2 memory bus frequency (MCK)” range to 125–200. • In Table 79, “e300 Core PLL Configuration,” added 3.5:1 and 4:1 core_clk: csb_clk ratio options. • In Table 80, “Example Clock Frequency Combinations,” updated column heading to “DDR data rate” . • In Section 20.2, “SPI AC Timing Specifications,” corrected t_{NIKHOX} and t_{NEKHOX} to t_{NIKHOV} and t_{NEKHOV}, respectively.
1	02/2009	• In Table 3, “Recommended Operating Conditions,” added two new rows for 800 MHz, and created two rows for SerDes. In addition, changed 666 to 667 MHz. • In Table 5, “Power Dissipation [1],” added Notes 4 and 5. In addition, changed 666 to 667 MHz. • In Table 13, “DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V,” Table 21, “DDR1 and DDR2 SDRAM Output AC Timing Specifications,” and Table 72, “TePBGA II Pinout Listing,” added footnote to references to MVREF, MDQ, and MDQS, referencing AN3665, *MPC837xE Design Checklist*. • In Table 21, updated t_{DDKHCX} minimum value for 333 MHz to 2.40. • In Table 72, “TePBGA II Pinout Listing,” added footnote to USBDR_STP_SUSPEND and modified footnote 10 and added footnote 14. • In Table 74, “Operating Frequencies for TePBGA II,” changed 667 to 800 MHz for *core_clk*. • In Table 80, “Example Clock Frequency Combinations,” added 800 MHz cells for e300 core. • Updated part numbering information in AF column in Table 84, “Part Numbering Nomenclature.” In addition, modified extended temperature information in notes 1 and 4. • In Table 85, “Available Parts (Core/DDR Data Rate),” added new row for 800/400 MHz.
0	12/2008	Initial public release.