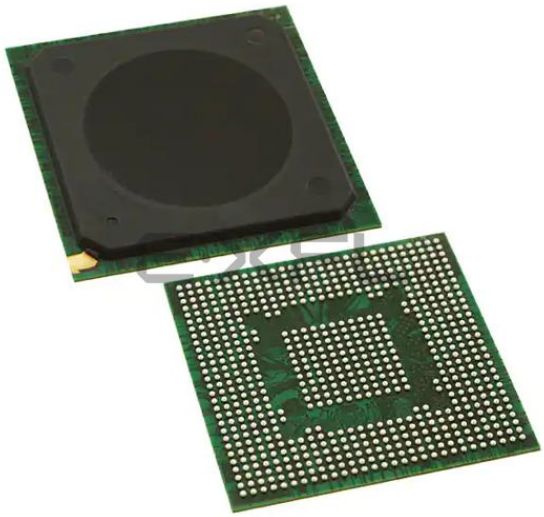

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c4s
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 125°C (TA)
Security Features	-
Package / Case	689-BBGA Exposed Pad
Supplier Device Package	689-TEPBGA II (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8377vragd

voltage supplies—GV_{DD}, LV_{DD}, and OV_{DD}—do not have any ordering requirements with respect to one another.

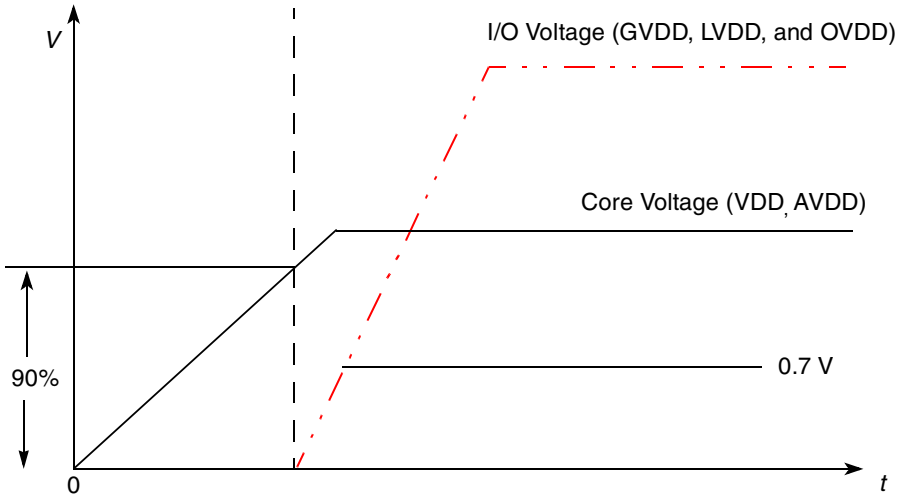

Figure 3. Power-Up Sequencing Example

Note that the SerDes power supply (L[1,2]_$n$$V_{DD}$) should follow the same timing as the core supply (V_{DD}).

The device does not require the core supply voltage and I/O supply voltages to be powered down in any particular order.

3 Power Characteristics

The estimated typical power dissipation for the chip device is shown in this table.

Table 5. Power Dissipation [1]

Core Frequency (MHz)	CSB/DDR Frequency (MHz)	Sleep Power at T_j = 65°C (W) [2]	Typical Application at T_j = 65°C (W) [2]	Typical Application at T_j = 125°C (W) [3]	Max Application at T_j = 125°C (W) [4]
333	333	1.45	1.9	3.2	3.8
	167	1.45	1.8	3.0	3.6
400	400	1.45	2.0	3.3	4.0
	266	1.45	1.9	3.1	3.8
450	300	1.45	2.0	3.2	3.8
	225	1.45	1.9	3.1	3.7
500	333	1.45	2.0	3.3	3.9
	250	1.45	1.9	3.2	3.8
533	355	1.45	2.0	3.3	4.0
	266	1.45	2.0	3.2	3.9

This figure shows the MII receive AC timing diagram.

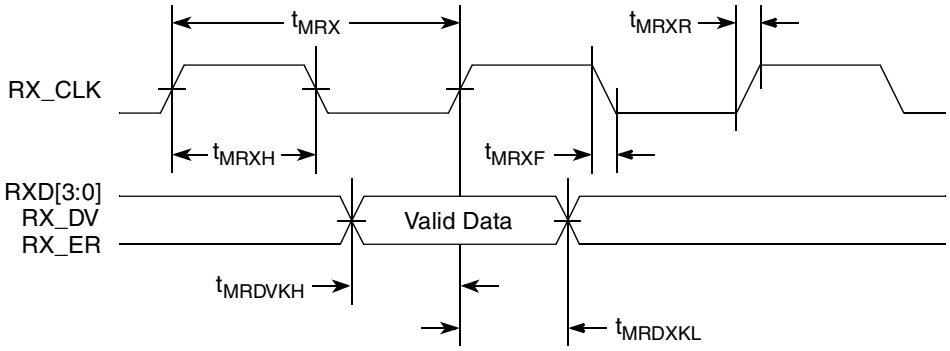

Figure 9. MII Receive AC Timing Diagram

8.2.2 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 28. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit	Note
Data to clock output skew (at transmitter)	t_{SKRGT}	–600	0	600	ps	—
Data to clock input skew (at receiver)	t_{SKRGT}	1.0	—	2.8	ns	2
Clock period	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 1000Base-T	t_{RGTH}/t_{RGT}	45	50	55	%	4
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns	—
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns	—
EC_GTX_CLK125 reference clock period	t_{G12}	—	8.0	—	ns	5
EC_GTX_CLK125 reference clock duty cycle measured at $0.5 \times LV_{DD1}$	t_{G125H}/t_{G125}	47	—	53	%	—

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between
5. This symbol represents the external EC_GTX_CLK125 and does not follow the original signal naming convention.

8.2.3 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.3.1 RMII Transmit AC Timing Specifications

This table shows the RMII transmit AC timing specifications.

Table 29. RMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMTH}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

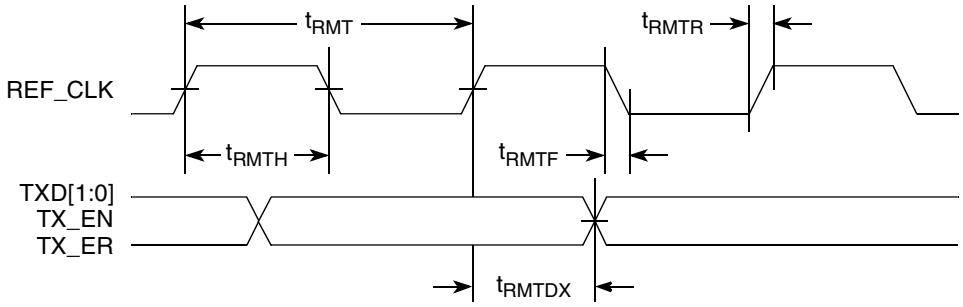

Figure 12. RMII Transmit AC Timing Diagram

8.2.3.2 RMII Receive AC Timing Specifications

This table shows the RMII receive AC timing specifications.

Table 30. RMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
Input low voltage at 3.3 LV_{DD}	V_{IL}	—	—	0.8	V
Input high voltage at 3.3 LV_{DD}	V_{IH}	2.0	—	—	V
REF_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMRH}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMRR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMRF}	1.0	—	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t_{RMRDV}	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t_{RMRDX}	2.0	—	—	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load for eTSEC.

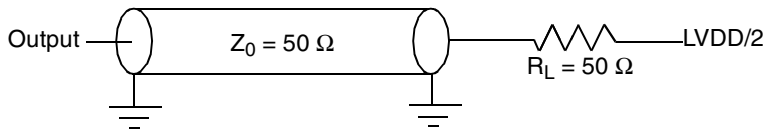

Figure 13. eTSEC AC Test Load

9.2 USB AC Electrical Specifications

This table describes the general timing parameters of the USB interface of the device.

Table 35. USB General Timing Parameters (ULPI Mode Only)

Parameter	Symbol [1]	Min	Max	Unit	Note
USB clock cycle time	t_{USCK}	15	—	ns	2, 3, 4, 5
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	2, 3, 4, 5
Input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	2, 3, 4, 5
USB clock to output valid—all outputs	t_{USKHOV}	—	7	ns	2, 3, 4, 5
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	2, 3, 4, 5

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H) with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to the USB clock, USBDR_CLK.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

These two figures provide the AC test load and signals for the USB, respectively.

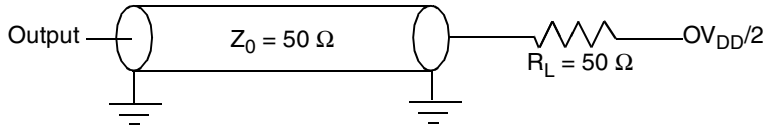

Figure 17. USB AC Test Load

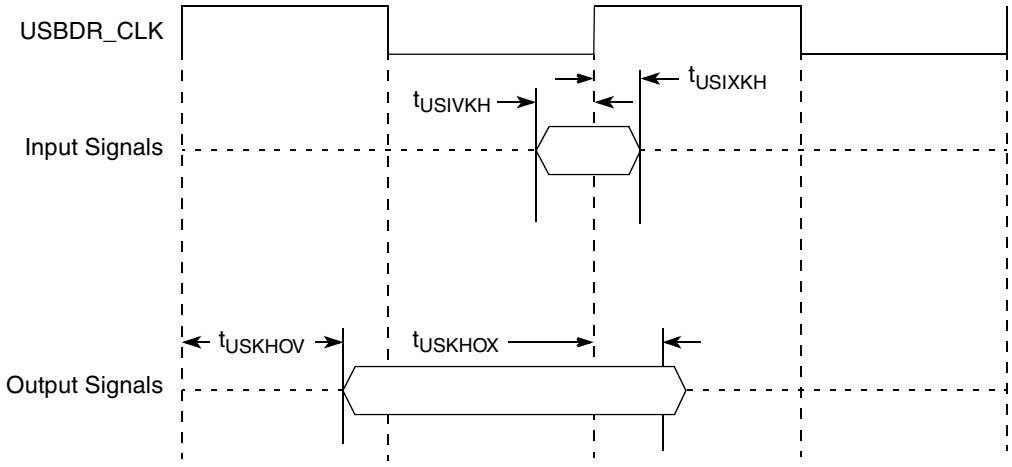

Figure 18. USB Interface Timing Diagram

This figures show the local bus signals.

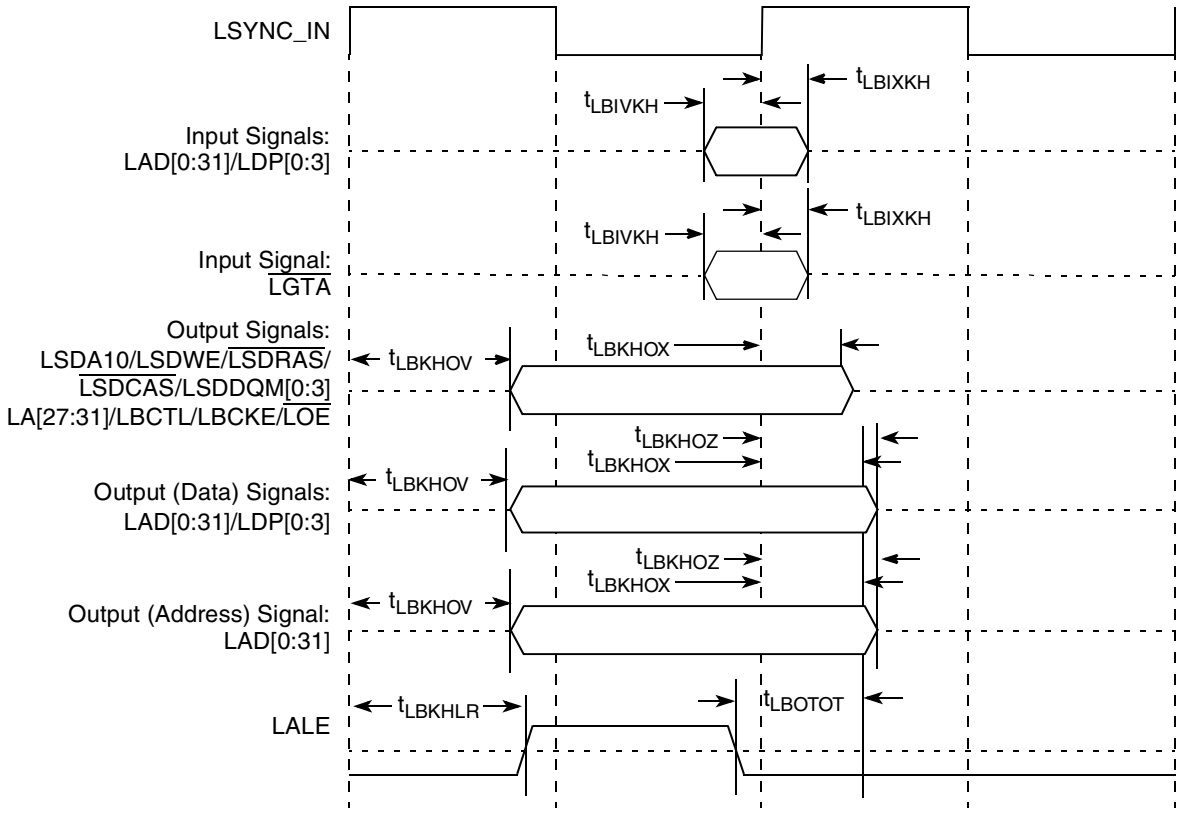

Figure 20. Local Bus Signals, Non-special Signals Only (PLL Enable Mode)

Table 42. eSDHC AC Timing Specifications for Full-Speed Mode (continued)

At recommended operating conditions OV_{DD} = 3.3 V ± 165 mV.

Parameter	Symbol[1]	Min	Max	Unit	Note
Input hold times: SD_CMD, SD_DAT*x*, SD_CD to SD_CLK	$t_{SFSIXKH}$	0	—	ns	2
SD_CLK delay within device	$t_{INT\_CLK\_DLY}$	1.5	—	ns	4
Output valid: SD_CLK to SD_CMD, SD_DAT*x* valid	$t_{SFSKHOV}$	—	4	ns	2
Output hold: SD_CLK to SD_CMD, SD_DAT*x* valid	$t_{SFSKHOX}$	0	—	—	—
SD card input setup	t_{ISU}	5	—	ns	3
SD card input hold	t_{IH}	5	—	ns	3
SD card output valid	t_{ODLY}	—	14	ns	3
SD card output hold	t_{OH}	0	—	ns	3

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{SFSIXKH}$ symbolizes eSDHC full mode speed device timing (SFS) input (I) to go invalid (X) with respect to the clock reference (K) going to high (H). Also $t_{SFSKHOV}$ symbolizes eSDHC full speed timing (SFS) for the clock reference (K) to go high (H), with respect to the output (O) going valid (V) or data output valid time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Measured at capacitive load of 40 pF.
3. For reference only, according to the SD card specifications.
4. Average, for reference only.

This figure provides the eSDHC clock input timing diagram.

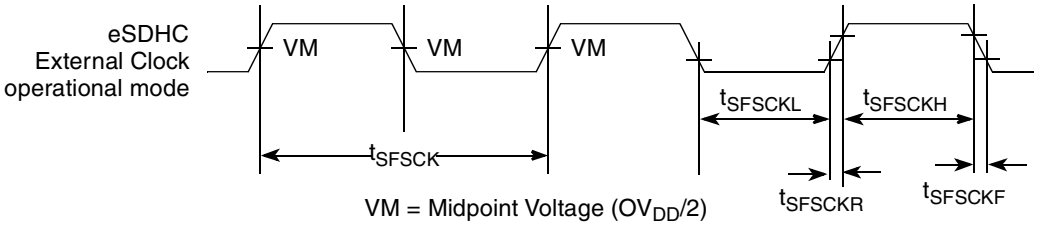

Figure 26. eSDHC Clock Input Timing Diagram

This figure provides the eSDHC clock input timing diagram.

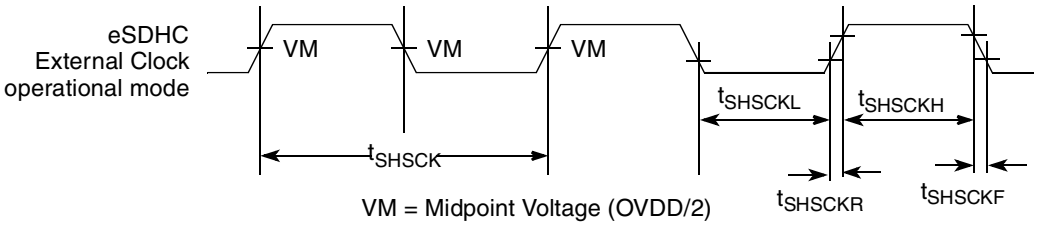

Figure 29. eSDHC Clock Input Timing Diagram

11.3.1 High-Speed Output Path (Write)

This figure provides the data and command output timing diagram.

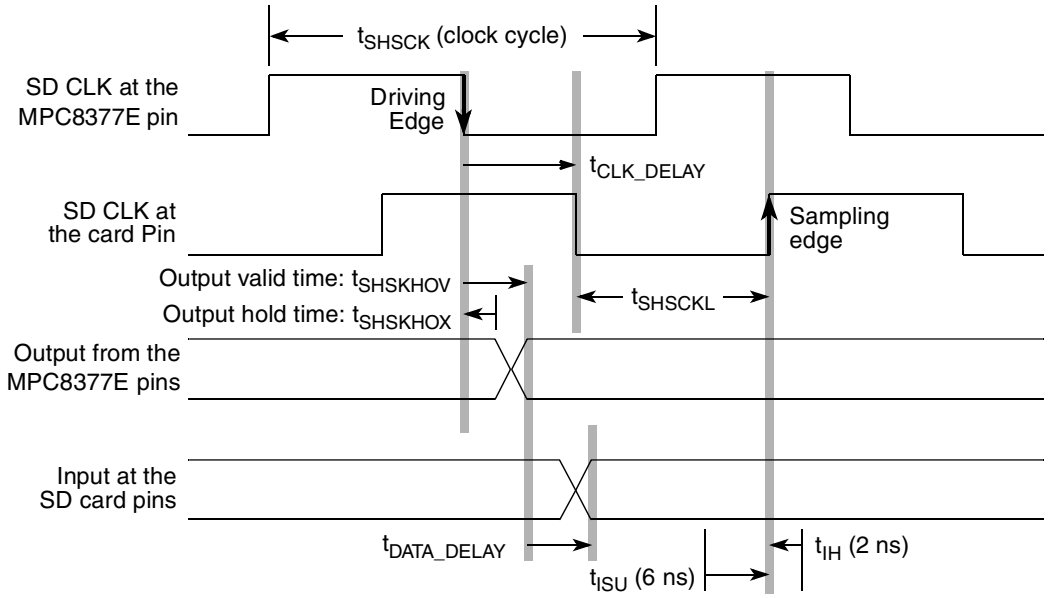

Figure 30. High Speed Output Path

11.3.1.1 High-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

Zero clock delay:

$$t_{SHSKHOV} + t_{DATA\_DELAY} + t_{ISU} < t_{SHSCKL} \quad \textit{Eqn. 10}$$

With clock delay:

$$t_{SHSKHOV} + t_{DATA\_DELAY} + t_{ISU} < t_{SHSCKL} + t_{CLK\_DELAY} \quad \textit{Eqn. 11}$$

$$t_{DATA\_DELAY} - t_{CLK\_DELAY} < t_{SHSCKL} - t_{ISU} - t_{SHSKHOV} \quad \textit{Eqn. 12}$$

This means that data delay should be equal or less than the clock delay in the ideal case where $t_{SHSCLKL}$ = 10 ns:

$$t_{DATA\_DELAY} - t_{CLK\_DELAY} < 10 - 6 - 4$$
$$t_{DATA\_DELAY} - t_{CLK\_DELAY} < 0$$

11.3.1.2 High-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK\_DELAY} < t_{SHSCKL} + t_{SHSKHOX} + t_{DATA\_DELAY} - t_{IH} \quad \textit{Eqn. 13}$$

$$t_{CLK\_DELAY} - t_{DATA\_DELAY} < t_{SHSCKL} + t_{SHSKHOX} - t_{IH} \quad \textit{Eqn. 14}$$

This means that clock can be delayed versus data up to 8 ns (external delay line) in ideal case of $t_{SHSCLKL}$ = 10 ns:

$$t_{CLK\_DELAY} - t_{DATA\_DELAY} < 10 + 0 - 2$$
$$t_{CLK\_DELAY} - t_{DATA\_DELAY} < 8$$

11.3.2 High-Speed Input Path (Read)

This figure provides the data and command input timing diagram.

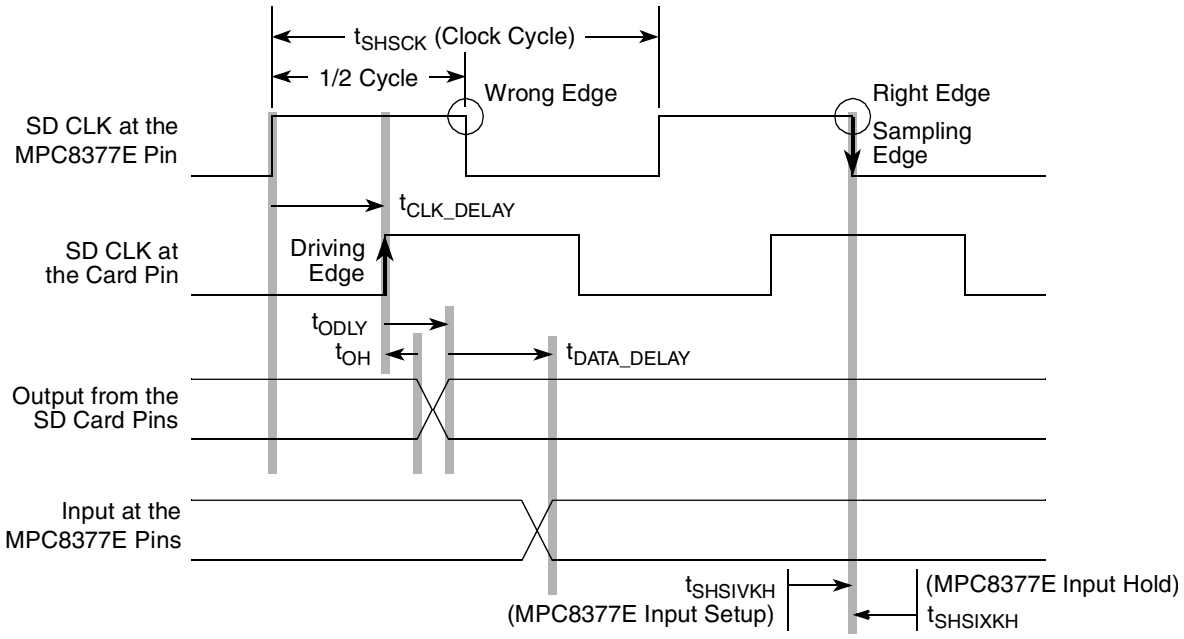

Figure 31. High-Speed Input Path

For the input path, the device eSDHC expects to sample the data 1.5 internal clock cycles after it was driven by the SD card. Since in this mode the SD card drives the data at the rising edge of the clock, a sufficient delay to the clock and the data must exist to ensure it will not be sampled at the wrong internal

This figure provides the boundary-scan timing diagram.

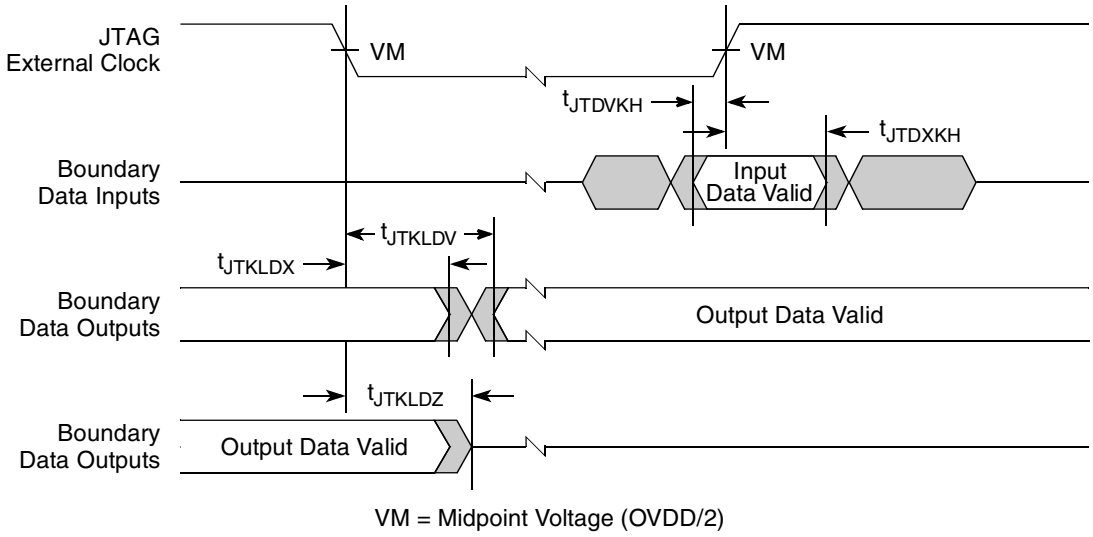

Figure 35. Boundary-Scan Timing Diagram

This figure provides the test access port timing diagram.

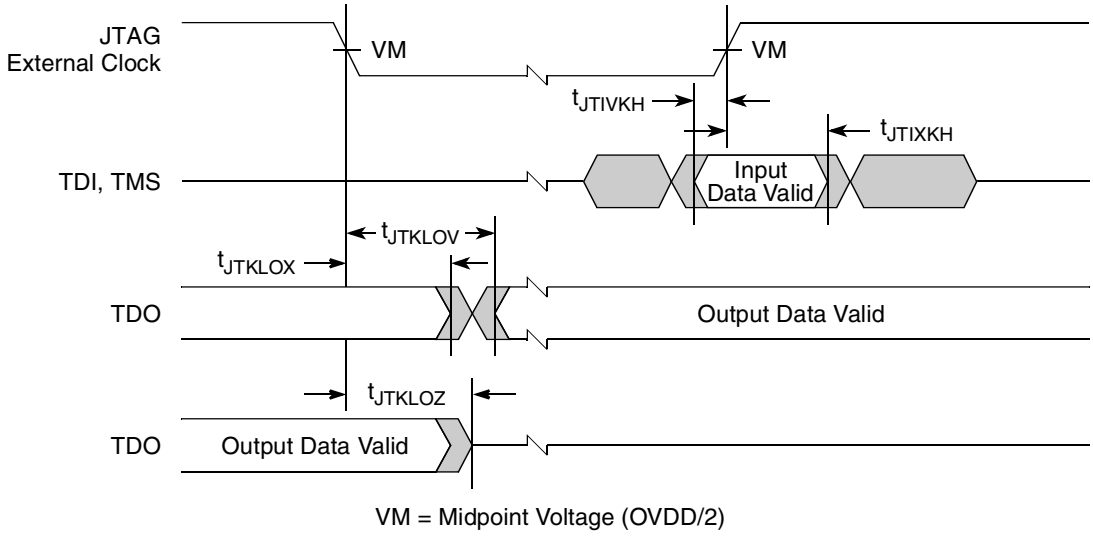

Figure 36. Test Access Port Timing Diagram

Table 49. PCI AC Timing Specifications at 66 MHz (continued)

PCI_SYNC_IN clock input levels are with next levels: VIL = $0.1 \times OV_{DD}$, VIH = $0.7 \times OV_{DD}$.

Parameter	Symbol[1]	Min	Max	Unit	Note
Input hold from cock	t_{PCIXKH}	0.25	—	ns	2, 4, 6
Output clock skew	t_{PCKOSK}	—	0.5	ns	5

Notes:

1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. PCI specifications allows 1 ns skew for 66 MHz but includes the total allowed skew, board, connectors, etc.
6. Value does not comply with the *PCI 2.3 Local Bus Specifications*.

This table shows the PCI AC timing specifications at 33 MHz.

Table 50. PCI AC Timing Specifications at 33 MHz

PCI_SYNC_IN clock input levels are with next levels: VIL = $0.1 \times OV_{DD}$, $V_{IH} = 0.7 \times OV_{DD}$.

Parameter	Symbol[1]	Min	Max	Unit	Note
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0.25	—	ns	2, 4, 6
Output clock skew	t_{PCKOSK}	—	0.5	ns	5

Notes:

1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. PCI specifications allows 2 ns skew for 33 MHz but includes the total allowed skew, board, connectors, etc.
6. Value does not comply with the *PCI 2.3 Local Bus Specifications*.

Table 53. Differential Receiver (Rx) Input Specifications (continued)

Parameter	Comments	Symbol	Min	Typical	Max	Units	Note
Unexpected Electrical Idle Enter Detect Threshold Integration Time	An unexpected electrical idle (Vrx-diffp-p < Vrx-idle-det-diffp-p) must be recognized no longer than Trx-idle-det-diff-entertime to signal an unexpected idle condition.	$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	—	—	10	ms	—
Total Skew	Skew across all lanes on a link. This includes variation in the length of SKP ordered set (e.g. COM and one to five SKP Symbols) at the Rx as well as any delay differences arising from the interconnect itself.	$L_{RX-SKEW}$	—	—	20	ns	—

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 44 should be used as the Rx device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 43). If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{Rx-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRx-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The receiver input impedance will result in a differential return loss greater than or equal to 10 dB with the D+ line biased to 300 mV and the D– line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 44). Note that the series capacitors, C_{Tx}, is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
6. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.
7. It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

15.5 Receiver Compliance Eye Diagrams

The Rx eye diagram in Figure 43 is specified using the passive compliance/test measurement load (see Figure 44) in place of any real PCI Express Rx component. In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 44) is larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics that cause the real PCI Express component to vary in impedance from the

compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. Rx component designer should provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 43) expected at the input receiver based on an adequate combination of system simulations and the return loss measured looking into the Rx package and silicon. The Rx eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI.

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a Vector Network Analyzer with 50 Ω probes—see Figure 44). Note that the series capacitors, $C_{PEACCTX}$, are optional for the return loss measurement.

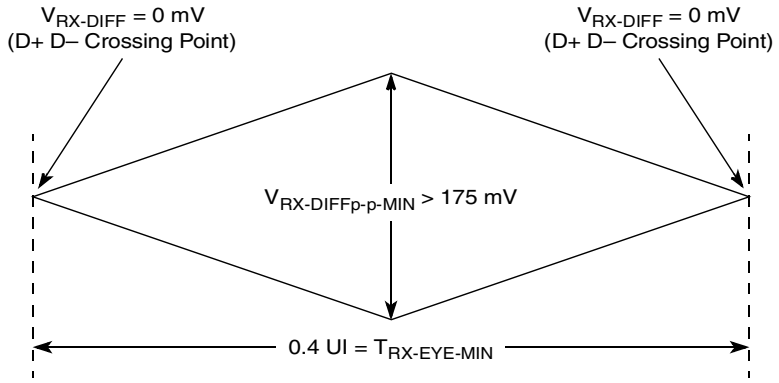

Figure 43. Minimum Receiver Eye Timing and Voltage Compliance Specification

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

- **Single-Ended Swing**

  The transmitter output signals and the receiver input signals SD*n*_TX, $\overline{\text{SD}n\text{\_TX}}$, SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

- **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**):

  The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SDn\_TX} - V_{\overline{SDn\_TX}}$. The V_{OD} value can be either positive or negative.

- **Differential Input Voltage, V_{ID}** (or **Differential Input Swing**):

  The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SDn\_RX} - V_{\overline{SDn\_RX}}$. The V_{ID} value can be either positive or negative.

- **Differential Peak Voltage**, V_{DIFFp}

  The peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

- **Differential Peak-to-Peak**, $V_{DIFFp-p}$

  Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.

- **Differential Waveform**

  The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD}n\text{\_TX}}$, for example) from the non-inverting signal (SD*n*_TX, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 60 as an example for differential waveform.

- **Common Mode Voltage, V_{cm}**

  The common mode voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SDn\_TX} + V_{\overline{SDn\_TX}}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.

greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

— For **external DC-coupled** connection, as described in Section 21.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 53 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

— For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDS*n*. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDS*n*). Figure 54 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

- **Single-ended Mode**

— The reference clock can also be single-ended. The SD _REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV_{p-p} (from V_{min} to V_{max}) with $\overline{SDn\_REF\_CLK}$ either left unconnected or tied to ground.

— The SD*n*_REF_CLK input average voltage must be between 200 mV and 400 mV. Figure 55 shows the SerDes reference clock input requirement for single-ended signaling mode.

— To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{SDn\_REF\_CLK}$) through the same source impedance as the clock input (SD*n*_REF_CLK) in use.

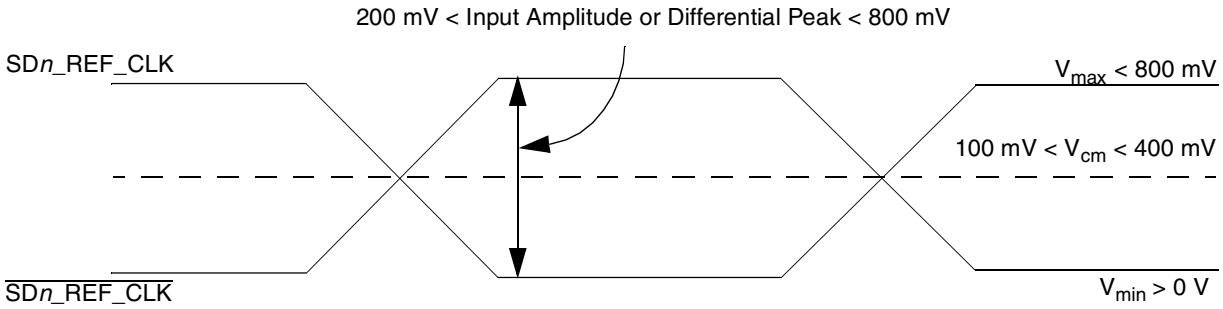

Figure 53. Differential Reference Clock Input DC Requirements (External DC-Coupled)

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MDQ35	AE1	I/O	GVDD	11
MDQ36	V6	I/O	GVDD	11
MDQ37	Y5	I/O	GVDD	11
MDQ38	AA4	I/O	GVDD	11
MDQ39	AB6	I/O	GVDD	11
MDQ40	AD3	I/O	GVDD	11
MDQ41	AC4	I/O	GVDD	11
MDQ42	AD4	I/O	GVDD	11
MDQ43	AF1	I/O	GVDD	11
MDQ44	AE4	I/O	GVDD	11
MDQ45	AC5	I/O	GVDD	11
MDQ46	AE2	I/O	GVDD	11
MDQ47	AE3	I/O	GVDD	11
MDQ48	AG1	I/O	GVDD	11
MDQ49	AG2	I/O	GVDD	11
MDQ50	AG3	I/O	GVDD	11
MDQ51	AF5	I/O	GVDD	11
MDQ52	AE5	I/O	GVDD	11
MDQ53	AD7	I/O	GVDD	11
MDQ54	AH2	I/O	GVDD	11
MDQ55	AG4	I/O	GVDD	11
MDQ56	AH3	I/O	GVDD	11
MDQ57	AG5	I/O	GVDD	11
MDQ58	AF8	I/O	GVDD	11
MDQ59	AJ5	I/O	GVDD	11
MDQ60	AF6	I/O	GVDD	11
MDQ61	AF7	I/O	GVDD	11
MDQ62	AH6	I/O	GVDD	11
MDQ63	AH7	I/O	GVDD	11
MDQS0	C8	I/O	GVDD	11
MDQS1	C4	I/O	GVDD	11
MDQS2	E3	I/O	GVDD	11
MDQS3	G2	I/O	GVDD	11

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
LA25/LAD30	D29	I/O	LBVDD	—
LA26/LAD31	E20	I/O	LBVDD	—
LA27	H26	O	LBVDD	—
LA28	C29	O	LBVDD	—
LA29	E28	O	LBVDD	—
LA30	B26	O	LBVDD	—
LA31	J25	O	LBVDD	—
LA10/LALE	H29	O	LBVDD	—
LBCTL	A22	O	LBVDD	—
LCLK0	B22	O	LBVDD	—
LCLK1	C23	O	LBVDD	—
LCLK2	B23	O	LBVDD	—
LCS_B0	D25	O	LBVDD	—
LCS_B1	F19	O	LBVDD	—
LCS_B2	C27	O	LBVDD	—
LCS_B3	D24	O	LBVDD	—
LCS_B4/LDP0	C24	I/O	LBVDD	—
LCS_B5/LDP1	B29	I/O	LBVDD	—
LA7/LCS_B6/LDP2	E29	I/O	LBVDD	—
LA8/LCS_B7/LDP3	F29	I/O	LBVDD	—
LFCLE/LGPL0	D21	O	LBVDD	—
LFALE/LGPL1	A26	O	LBVDD	—
LFRE_B/LGPL2/LOE_B	F22	O	LBVDD	—
LFWP_B/LGPL3	C21	O	LBVDD	—
LGPL4/LFRB_B/LGTA_B/ LUPWAIT/LPBSE	J29	I/O	LBVDD	16
LA9/LGPL5	G29	O	LBVDD	—
LSYNC_IN	A21	I	LBVDD	—
LSYNC_OUT	D23	O	LBVDD	—
LWE_B0/LFWE0/LBS_B0	E22	O	LBVDD	—
LWE_B1/LFWE1/LBS_B1	B25	O	LBVDD	—
LWE_B2/LFWE2/LBS_B2	E27	O	LBVDD	—
LWE_B3/LFWE3/LBS_B3	F28	O	LBVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
Programmable Interrupt Controller (PIC) Interface				
MCP_OUT_B	AD14	O	OVDD	2
IRQ_B0/MCP_IN_B/GPIO2[12]	F9	I/O	OVDD	—
IRQ_B1/GPIO2[13]	E9	I/O	OVDD	—
IRQ_B2/GPIO2[14]	F10	I/O	OVDD	—
IRQ_B3/GPIO2[15]	D9	I/O	OVDD	—
IRQ_B4/GPIO2[16]/SD_WP	C9	I/O	OVDD	—
IRQ_B5/GPIO2[17]/ USBDR_PWRFAULT	AE10	I/O	OVDD	—
IRQ_B6/GPIO2[18]	AD10	I/O	OVDD	—
IRQ_B7/GPIO2[19]	AD9	I/O	OVDD	—
PMC Interface				
QUIESCE_B	D13	O	OVDD	—
SerDes1 Interface				
L1_SD_IMP_CAL_RX	AJ14	I	L1_XPADVDD	—
L1_SD_IMP_CAL_TX	AG19	I	L1_XPADVDD	—
L1_SD_REF_CLK	AJ17	I	L1_XPADVDD	—
L1_SD_REF_CLK_B	AH17	I	L1_XPADVDD	—
L1_SD_RXA_N	AJ15	I	L1_XPADVDD	—
L1_SD_RXA_P	AH15	I	L1_XPADVDD	—
L1_SD_RXE_N	AJ19	I	L1_XPADVDD	—
L1_SD_RXE_P	AH19	I	L1_XPADVDD	—
L1_SD_TXA_N	AF15	O	L1_XPADVDD	—
L1_SD_TXA_P	AE15	O	L1_XPADVDD	—
L1_SD_TXE_N	AF18	O	L1_XPADVDD	—
L1_SD_TXE_P	AE18	O	L1_XPADVDD	—
L1_SDAVDD_0	AJ18	SerDes PLL Power (1.0 or 1.05 V)	—	—
L1_SDAVSS_0	AG17	SerDes PLL GND	—	—
L1_XCOREVDD	AH14, AJ16, AF17, AH20, AJ20	SerDes Core Power (1.0 or 1.05 V)	—	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
SPIMISO/SD_DAT0	AD11	I/O	OVDD	—
SPIMOSI/SD_CMD	AJ9	I/O	OVDD	—
SPISEL_B/SD_CD	AE11	I	OVDD	—
System Control Interface				
SRESET_B	AD12	I/O	OVDD	2
HRESET_B	AE12	I/O	OVDD	1
PORESET_B	AE14	I	OVDD	—
Test Interface				
TEST	E10	I	OVDD	10
TEST_SEL0	D10	I	OVDD	13
TEST_SEL1	D12	I	OVDD	13
Thermal Management				
Reserved	F15	I	—	14
Power Supply Signals				
LVDD1	AC21, AG21, AH23	Power for eTSEC 1 I/O (2.5 V, 3.3 V)	LVDD1	—
LVDD2	AG24, AH27, AH29	Power for eTSEC 2 I/O (2.5 V, 3.3 V)	LVDD2	—
LBVDD	G20, D22, A24, G26, D27, A28	Power for eLBC (3.3, 2.5, or 1.8 V)	LBVDD	—
VDD	K10, L10, M10, N10, P10, R10, T10, U10, V10, W10, Y10, K11, R11, Y11, K12, Y12, K13, Y13, K14, Y14, K15, L15, W15, Y15, K16, Y16, K17, Y17, K18, Y18, K19, R19, Y19, K20, L20, M20, N20, P20, R20, T20, U20, V20, W20, Y20	Power for Core (1.0 V or 1.5 V)	VDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
Pull Down	B16, AH18	—	—	7

Notes:
1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OVDD.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OVDD.
3. This output is actively driven during reset rather than being released to high impedance during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI Specification recommendation and see AN3665, “MPC837xE Design Checklist,” for more details.
6. These are On Die Termination pins, used to control DDR2 memories internal termination resistance.
7. This pin must always be tied to GND using a 0 Ω resistor.
8. This pin must always be left not connected.
9. For DDR2 operation, it is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor.
10. This pin must always be tied low. If it is left floating it may cause the device to malfunction.
11. See AN3665, “MPC837xE Design Checklist,” for proper DDR termination.
12. This pin must not be pulled down during PORESET.
13. This pin must always be tied to OVDD.
14. Open or tie to GND.
15. Voltage settings are dependent on the frequency used; see Table 3.
16. See AN3665, “MPC837xE Design Checklist,” for proper termination.