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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300c4s
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 125°C (TA)
Security Features	-
Package / Case	689-BBGA Exposed Pad
Supplier Device Package	689-TEPBGA II (31x31)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8377vralg

1.10 PCI Express Controller

The PCI Express controller includes the following features:

- PCI Express 1.0a compatible
- Two ×1 links or one ×2 link width
- Auto-detection of number of connected lanes
- Selectable operation as root complex or endpoint
- Both 32- and 64-bit addressing
- 128-byte maximum payload size
- Support for MSI and INTx interrupt messages
- Virtual channel 0 only
- Selectable Traffic Class
- Full 64-bit decode with 32-bit wide windows
- Dedicated four channel descriptor-based DMA engine per interface

1.11 Serial ATA (SATA) Controllers

The serial ATA (SATA) controllers have the following features:

- Supports *Serial ATA Rev 2.5 Specification*
- Spread spectrum clocking on receive
- Asynchronous notification
- Hot Plug including asynchronous signal recovery
- Link power management
- Native command queuing
- Staggered spin-up and port multiplier support
- Port multiplier support
- SATA 1.5 and 3.0 Gb/s operation
- Interrupt driven
- Power management support
- Error handling and diagnostic features
  - — Far end/near end loopback
  - — Failed CRC error reporting
  - — Increased ALIGN insertion rates
- Scrambling and CONT override

6.2.2 DDR1 and DDR2 SDRAM Output AC Timing Specifications

This table shows the DDR1 and DDR2 SDRAM output AC timing specifications.

Table 21. DDR1 and DDR2 SDRAM Output AC Timing Specifications

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK*n* cycle time, MCK*n*/$\overline{\text{MCK}n}$ crossing	t_{MCK}	5	10	ns	2
ADDR/CMD output setup with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHAS}	 1.95 2.40 3.15 4.20	 — — — —	ns	3, 7
ADDR/CMD output hold with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHAX}	 1.95 2.40 3.15 4.20	 — — — —	ns	3, 7
$\overline{\text{MCS}n}$ output setup with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHCS}	 1.95 2.40 3.15 4.20	 — — — —	ns	3
$\overline{\text{MCS}n}$ output hold with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHCX}	 1.95 2.40 3.15 4.20	 — — — —	ns	3
MCK to MDQS skew	t_{DDKHMH}	–0.6	0.6	ns	4, 8
MDQ//MDM output setup with respect to MDQS 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHDS}, t_{DDKLDS}	 550 800 1100 1200	 — — — —	ps	5, 8
MDQ//MDM output hold with respect to MDQS 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHDX}, t_{DDKLDX}	 700 800 1100 1200	 — — — —	ps	5, 8
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6, 8

This figure shows the MII management AC timing diagram.

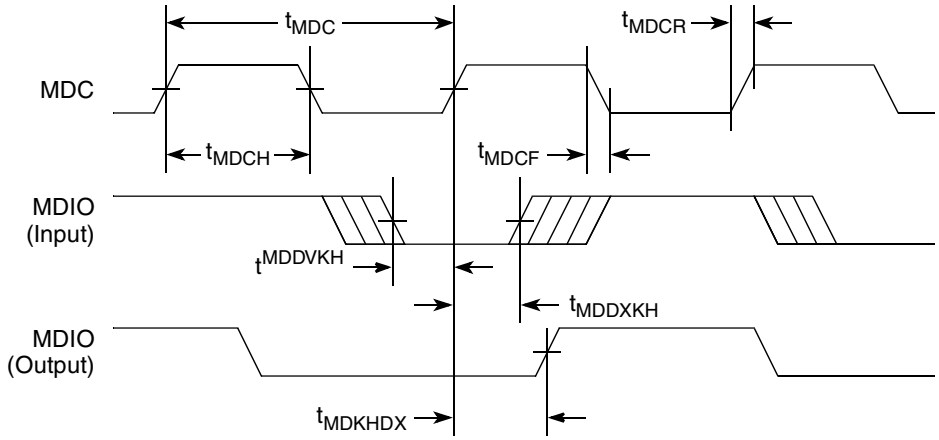


Figure 16. MII Management Interface Timing Diagram

9 USB

This section provides the AC and DC electrical characteristics for the USB dual-role controllers.

9.1 USB DC Electrical Characteristics

This table provides the DC electrical characteristics for the ULPI interface at recommended OV_{DD} = 3.3 V ± 165 mV.

Table 34. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V	1
Low-level input voltage	V_{IL}	–0.3	0.8	V	1
Input current	I_{IN}	—	±30	μA	2
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V	—
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V	—

Notes:
1. The minimum V_{IL} and maximum V_{IH} values are based on the respective minimum and maximum OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply and is referenced in Table 3.

9.2 USB AC Electrical Specifications

This table describes the general timing parameters of the USB interface of the device.

Table 35. USB General Timing Parameters (ULPI Mode Only)

Parameter	Symbol [1]	Min	Max	Unit	Note
USB clock cycle time	t_{USCK}	15	—	ns	2, 3, 4, 5
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	2, 3, 4, 5
Input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	2, 3, 4, 5
USB clock to output valid—all outputs	t_{USKHOV}	—	7	ns	2, 3, 4, 5
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	2, 3, 4, 5

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H) with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to the USB clock, USBDR_CLK.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

These two figures provide the AC test load and signals for the USB, respectively.

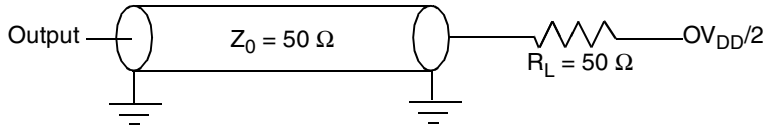


Figure 17. USB AC Test Load

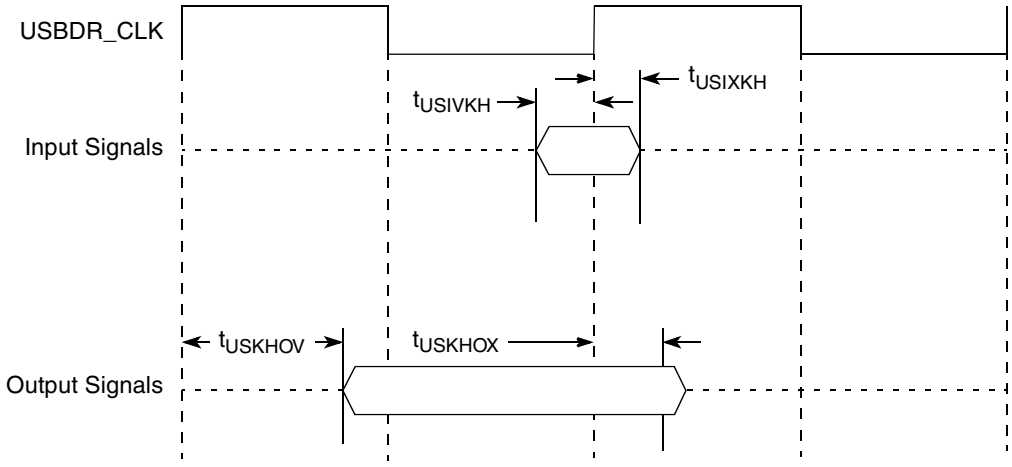


Figure 18. USB Interface Timing Diagram

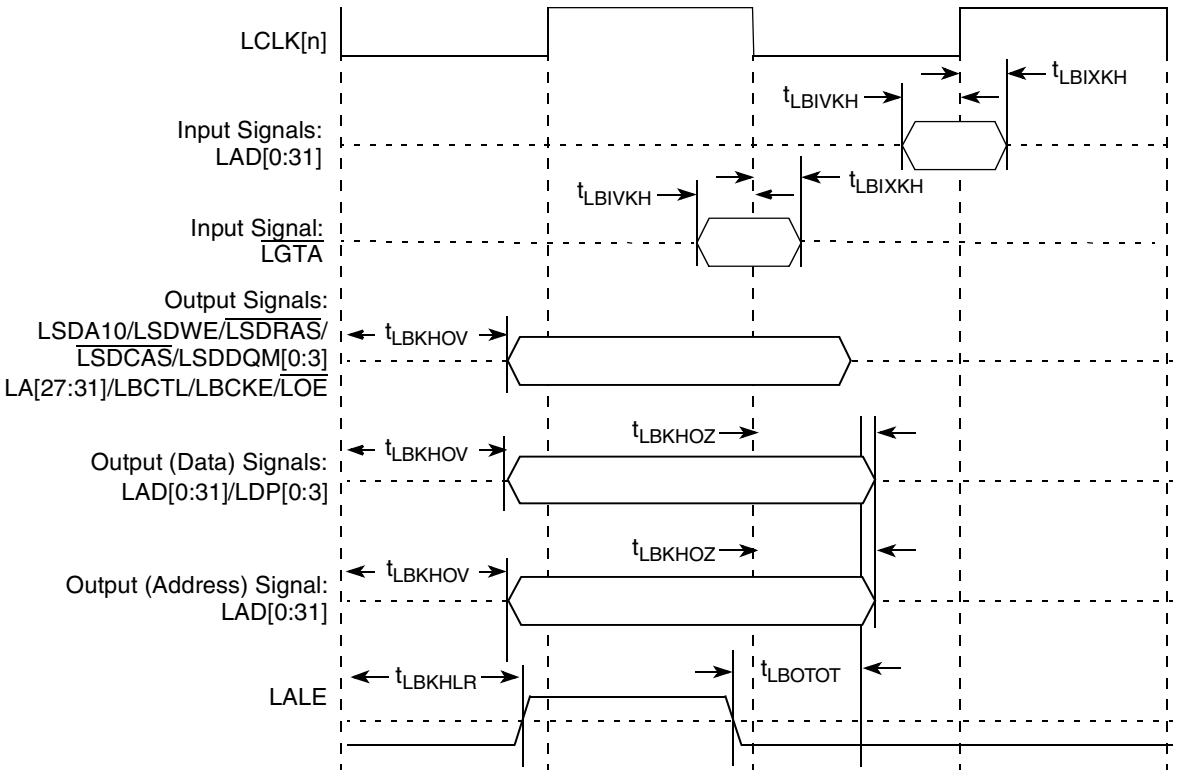


Figure 21. Local Bus Signals, Non-special Signals Only (PLL Bypass Mode)

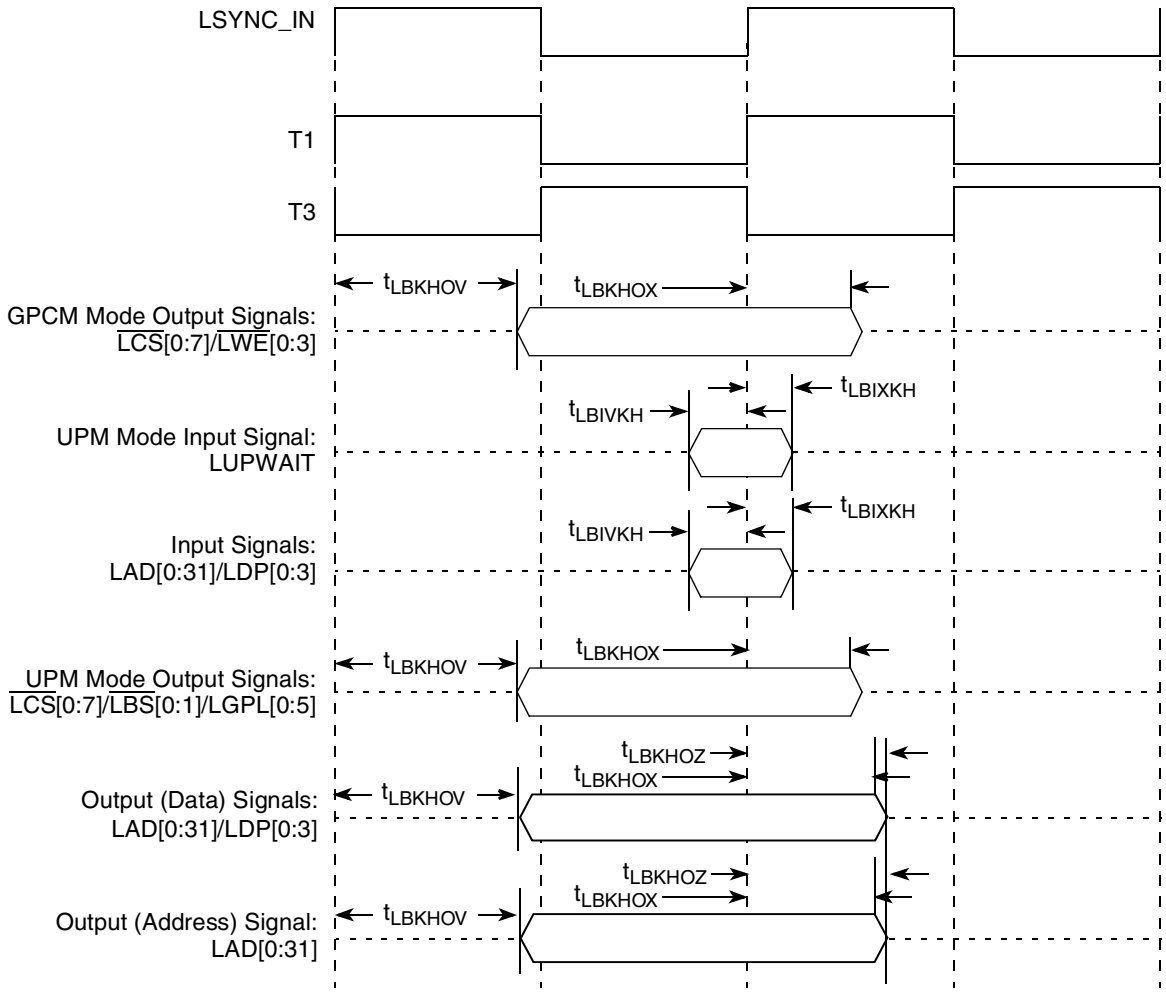


Figure 22. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (PLL Enable Mode)

11.2.1 Full-Speed Output Path (Write)

This figure provides the data and command output timing diagram.

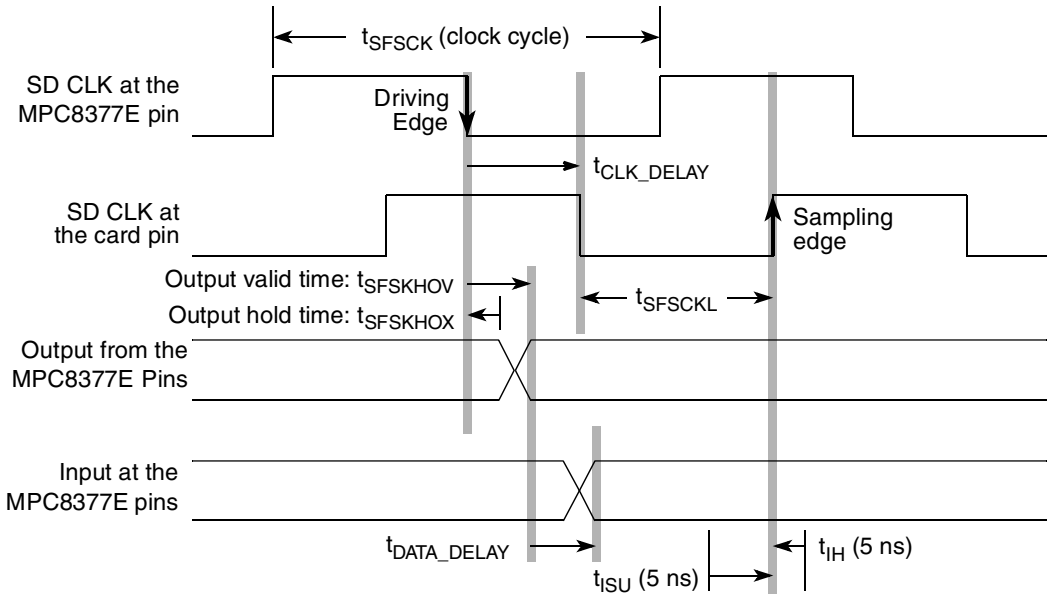


Figure 27. Full Speed Output Path

11.2.1.1 Full-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

No clock delay:

$$t_{SFSKHOV} + t_{DATA\_DELAY} + t_{ISU} < t_{SFSCKL} \quad \textit{Eqn. 1}$$

With clock delay:

$$t_{SFSKHOV} + t_{DATA\_DELAY} + t_{ISU} < t_{SFSCKL} + t_{CLK\_DELAY} \quad \textit{Eqn. 2}$$

$$t_{DATA\_DELAY} + t_{SFSCKL} < t_{SFSCK} + t_{CLK\_DELAY} - t_{ISU} - t_{SFSKHOV} \quad \textit{Eqn. 3}$$

This means that data can be delayed versus clock up to 11 ns in ideal case of t_{SFSCKL} = 20 ns:

$t_{DATA\_DELAY} + 20 < 40 + t_{CLK\_DELAY} - 5 - 4$

$t_{DATA\_DELAY} < 11 + t_{CLK\_DELAY}$

11.2.1.2 Full-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK\_DELAY} < t_{SFSCKL} + t_{SFSKHOX} + t_{DATA\_DELAY} - t_{IH} \quad \textit{Eqn. 4}$$

$$t_{CLK\_DELAY} + t_{IH} - t_{SFSKHOX} < t_{SFSCKL} + t_{DATA\_DELAY} \quad \text{Eqn. 5}$$

This means that clock can be delayed versus data up to 15 ns (external delay line) in ideal case of $t_{SFSCLKL}$ = 20 ns:

$t_{CLK\_DELAY} + 5 - 0 < 20 + t_{DATA\_DELAY}$

$t_{CLK\_DELAY} < 15 + t_{DATA\_DELAY}$

11.2.1.3 Full-Speed Write Combined Formula

The following equation is the combined formula to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK\_DELAY} + t_{IH} - t_{SFSKHOX} < t_{SFSCKL} + t_{DATA\_DELAY} < t_{SFSCK} + t_{CLK\_DELAY} - t_{ISU} - t_{SFSKHOV} \quad \text{Eqn. 6}$$

11.2.2 Full-Speed Input Path (Read)

This figure provides the data and command input timing diagram.

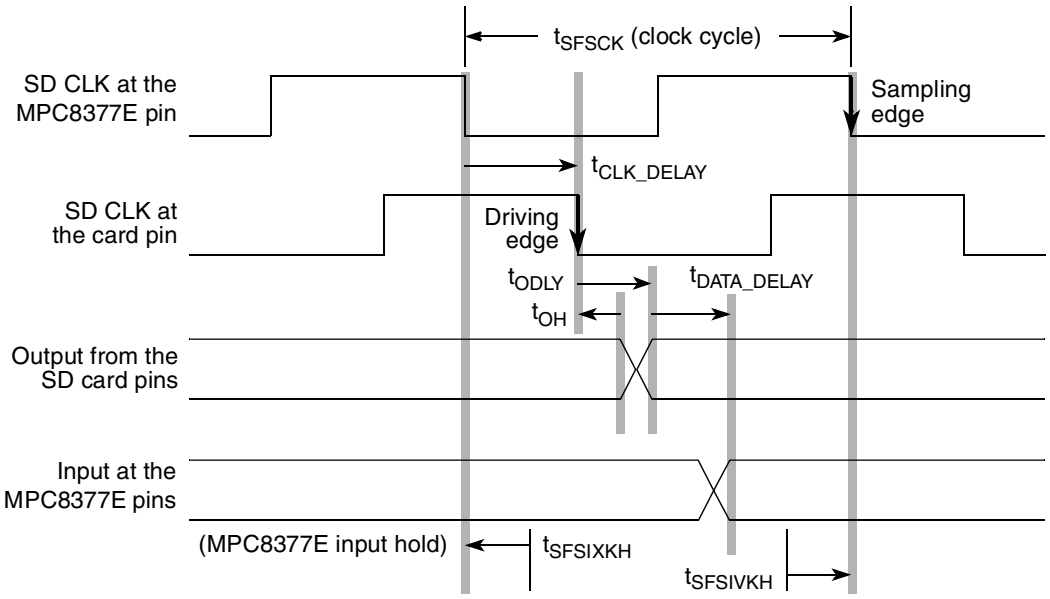


Figure 28. Full Speed Input Path

11.2.2.1 Full-Speed Read Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} + t_{ODLY} + t_{SFSIVKH} < t_{SFSCK} \quad \text{Eqn. 7}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < t_{SFSCK} - t_{ODLY} - t_{SFSIVKH} - t_{INT\_CLK\_DLY} \quad \text{Eqn. 8}$$

This figure provides the eSDHC clock input timing diagram.

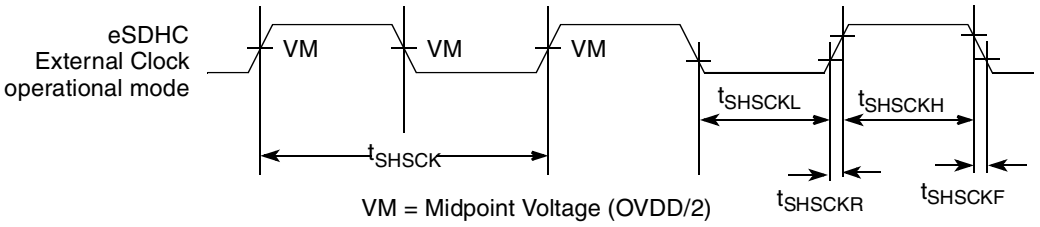


Figure 29. eSDHC Clock Input Timing Diagram

11.3.1 High-Speed Output Path (Write)

This figure provides the data and command output timing diagram.

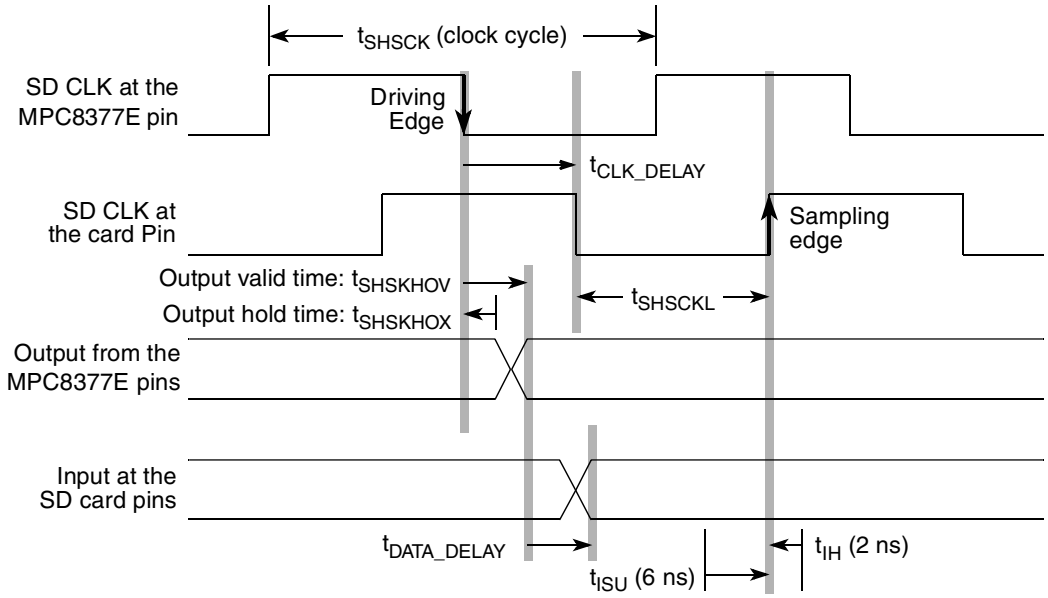


Figure 30. High Speed Output Path

11.3.1.1 High-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

Zero clock delay:

$$t_{SHSKHOV} + t_{DATA\_DELAY} + t_{ISU} < t_{SHSCKL} \quad \textit{Eqn. 10}$$

With clock delay:

$$t_{SHSKHOV} + t_{DATA\_DELAY} + t_{ISU} < t_{SHSCKL} + t_{CLK\_DELAY} \quad \textit{Eqn. 11}$$

$$t_{DATA\_DELAY} - t_{CLK\_DELAY} < t_{SHSCKL} - t_{ISU} - t_{SHSKHOV} \quad \textit{Eqn. 12}$$

12.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE 1149.1 (JTAG) interface of the chip.

Table 44. JTAG interface DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.5	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±30	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

12.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the device. This table provides the JTAG AC timing specifications as defined in Figure 33 through Figure 36.

Table 45. JTAG AC Timing Specifications (Independent of CLKIN) [1]

Parameter	Symbol[2]	Min	Max	Unit	Note
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	—
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	—

Table 45. JTAG AC Timing Specifications (Independent of CLKIN) [1] (continued)

Parameter	Symbol[2]	Min	Max	Unit	Note
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	5

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 Ω load (see Figure 17). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.

This figure provides the AC test load for TDO and the boundary-scan outputs of the device.

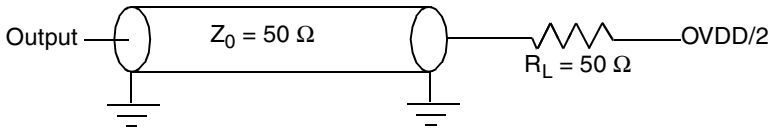


Figure 32. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

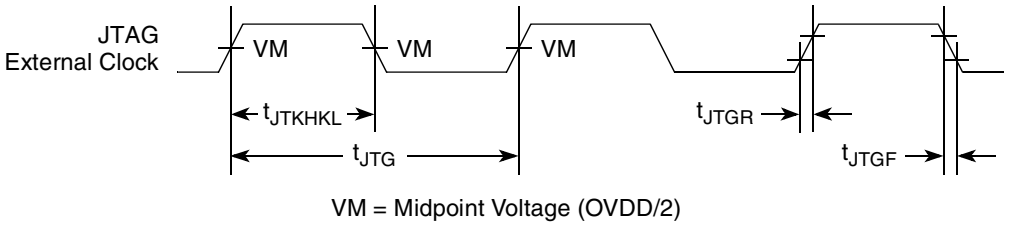


Figure 33. JTAG Clock Input Timing Diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.

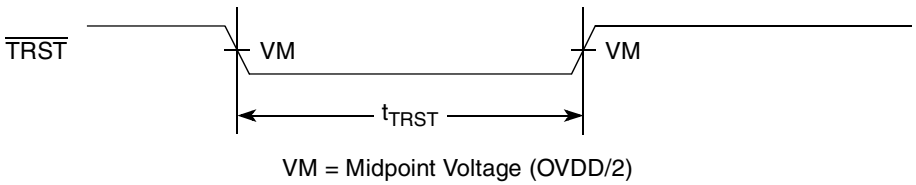


Figure 34. $\overline{\text{TRST}}$ Timing Diagram

This figure provides the AC test load for PCI.

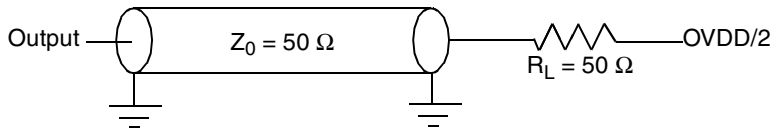


Figure 39. PCI AC Test Load

This figure shows the PCI input AC timing conditions.

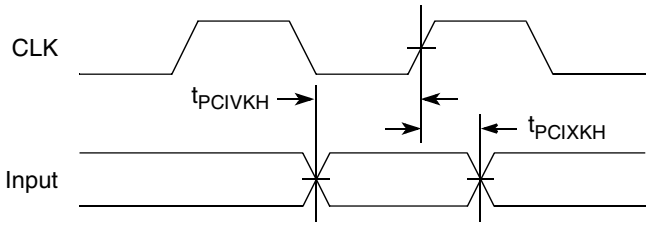


Figure 40. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.

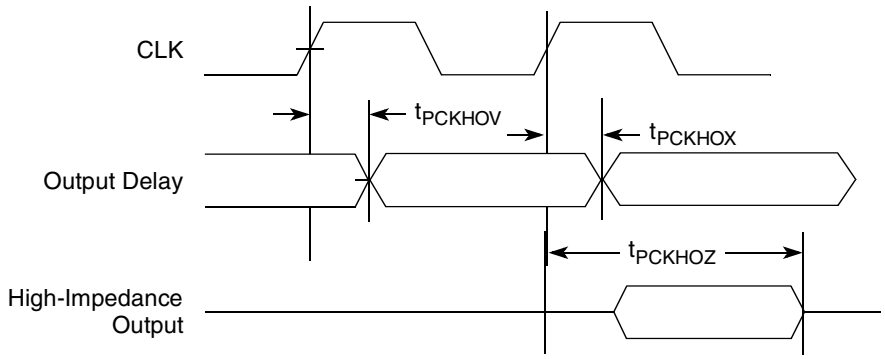


Figure 41. PCI Output AC Timing Measurement Condition

15 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus.

15.1 DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK

For more information see Section 21, “High-Speed Serial Interfaces (HSSI).”

compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. Rx component designer should provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 43) expected at the input receiver based on an adequate combination of system simulations and the return loss measured looking into the Rx package and silicon. The Rx eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI.

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a Vector Network Analyzer with 50 Ω probes—see Figure 44). Note that the series capacitors, $C_{PEACCTX}$, are optional for the return loss measurement.

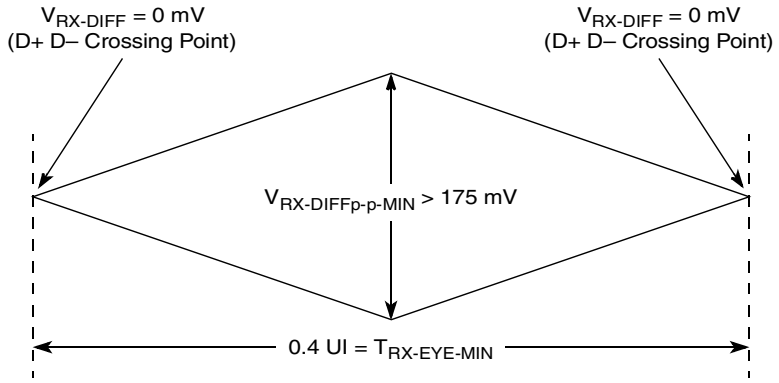


Figure 43. Minimum Receiver Eye Timing and Voltage Compliance Specification

19.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins of the chip.

Table 67. IPIC DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.0	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.8	V
Input current	—	I_{IN}	—	±30	μA
Output low voltage	I_{OL} = 6.0 mA	V_{OL}	—	0.5	V
Output low voltage	I_{OL} = 3.2 mA	V_{OL}	—	0.4	V

Note:
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, $\overline{\text{MCP\_OUT}}$.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

19.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

Table 68. IPIC Input AC Timing Specifications

Parameter	Symbol	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Note:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

20 SPI

This section describes the DC and AC electrical specifications for the SPI of the chip.

20.1 SPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the device SPI.

Table 69. SPI DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.0	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.8	V
Input current	—	I_{IN}	—	± 30	μA
Output high voltage	I_{OH} = –8.0 mA	V_{OH}	2.4	—	V

Table 69. SPI DC Electrical Characteristics (continued)

Parameter	Condition	Symbol	Min	Max	Unit
Output low voltage	I_{OL} = 8.0 mA	V_{OL}	—	0.5	V
Output low voltage	I_{OL} = 3.2 mA	V_{OL}	—	0.4	V

20.2 SPI AC Timing Specifications

This table provides the SPI input and output AC timing specifications.

Table 70. SPI AC Timing Specifications

Parameter	Symbol[1]	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOV}	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	4	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin. The maximum SPICLK input frequency is 66.666 MHz.

This figure provides the AC test load for the SPI.

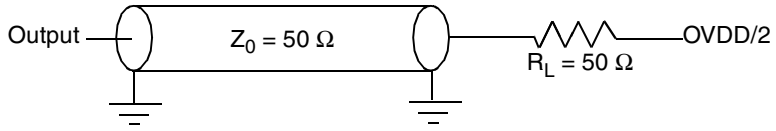


Figure 48. SPI AC Test Load

These figures represent the AC timing from Table 70. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters for PCI Express .

Table 71. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with XV_{DD_SRDS} or XV_{DD_SRDS} = 1.0 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	200	—	mV	2
Differential Input Low Voltage	V_{IL}	—	–200	mV	2
Rising edge rate (SD*n*_REF_CLK) to falling edge rate ($\overline{\text{SD}n\text{\_REF\_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Notes:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus $\overline{\text{SD}n\text{\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 60.
4. Matching applies to rising edge rate for SD*n*_REF_CLK and falling edge rate for $\overline{\text{SD}n\text{\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets $\overline{\text{SD}n\text{\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SD*n*_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SD}n\text{\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 61.

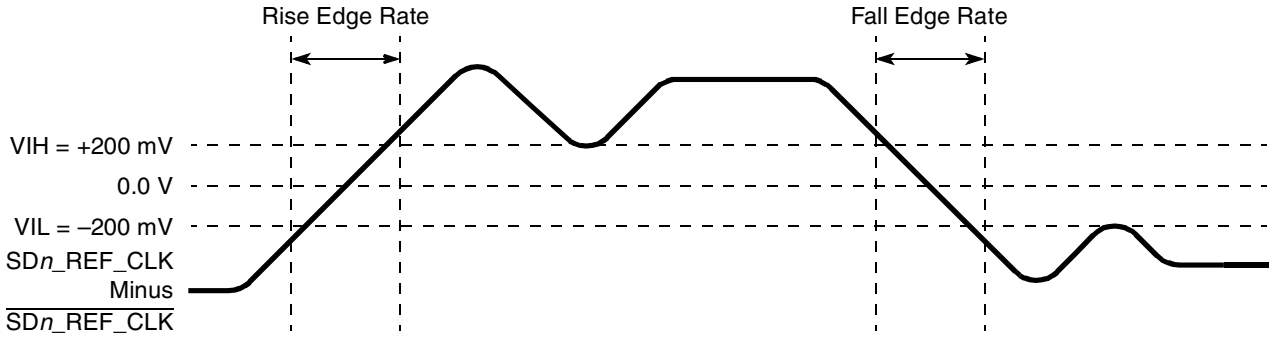


Figure 60. Differential Measurement Points for Rise and Fall Time

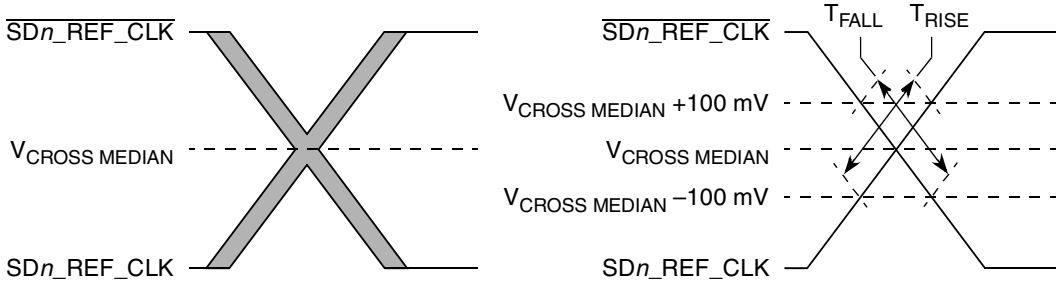


Figure 61. Single-Ended Measurement Points for Rise and Fall Time Matching

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
UART_RTS_B[2]	L29	O	OVDD	—
Enhanced Local Bus Controller (eLBC) Interface				
LAD0	E24	I/O	LBVDD	—
LAD1	G28	I/O	LBVDD	—
LAD2	H25	I/O	LBVDD	—
LAD3	F26	I/O	LBVDD	—
LAD4	C26	I/O	LBVDD	—
LAD5	J28	I/O	LBVDD	—
LAD6	F21	I/O	LBVDD	—
LAD7	F23	I/O	LBVDD	—
LAD8	E25	I/O	LBVDD	—
LAD9	E26	I/O	LBVDD	—
LAD10	A23	I/O	LBVDD	—
LAD11	F24	I/O	LBVDD	—
LAD12	G24	I/O	LBVDD	—
LAD13	F25	I/O	LBVDD	—
LAD14	H28	I/O	LBVDD	—
LAD15	G25	I/O	LBVDD	—
LA11/LAD16	F27	I/O	LBVDD	—
LA12/LAD17	B21	I/O	LBVDD	—
LA13/LAD18	A25	I/O	LBVDD	—
LA14/LAD19	C28	I/O	LBVDD	—
LA15/LAD20	H24	I/O	LBVDD	—
LA16/LAD21	E23	I/O	LBVDD	—
LA17/LAD22	B28	I/O	LBVDD	—
LA18/LAD23	D28	I/O	LBVDD	—
LA19/LAD24	A27	I/O	LBVDD	—
LA20/LAD25	C25	I/O	LBVDD	—
LA21/LAD26	B27	I/O	LBVDD	—
LA22/LAD27	H27	I/O	LBVDD	—
LA23/LAD28	E21	I/O	LBVDD	—
LA24/LAD29	F20	I/O	LBVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
L1_XCOREVSS	AG14, AG15, AG16, AH16, AG18, AG20	SerDes Core GND	—	—
L1_XPADVDD	AE16, AF16, AD18, AE19, AF19	SerDes I/O Power (1.0 or 1.05 V)	—	—
L1_XPADVSS	AF14, AE17, AF20	SerDes I/O GND	—	—
SerDes2 Interface				
L2_SD_IMP_CAL_RX	C19	I	L2_XPADVDD	—
L2_SD_IMP_CAL_TX	C15	I	L2_XPADVDD	—
L2_SD_REF_CLK	B17	I	L2_XPADVDD	—
L2_SD_REF_CLK_B	A17	I	L2_XPADVDD	—
L2_SD_RXA_N	A19	I	L2_XPADVDD	—
L2_SD_RXA_P	B19	I	L2_XPADVDD	—
L2_SD_RXE_N	A15	I	L2_XPADVDD	—
L2_SD_RXE_P	B15	I	L2_XPADVDD	—
L2_SD_TXA_N	D18	O	L2_XPADVDD	—
L2_SD_TXA_P	E18	O	L2_XPADVDD	—
L2_SD_TXE_N	D15	O	L2_XPADVDD	—
L2_SD_TXE_P	E15	O	L2_XPADVDD	—
L2_SDAVDD_0	A16	SerDes PLL Power (1.0 or 1.05 V)	—	—
L2_SDAVSS_0	C17	SerDes PLL GND	—	—
L2_XCOREVDD	A14, B14, D17, B18, B20	SerDes Core Power (1.0 or 1.05 V)	—	—
L2_XCOREVSS	C14, C16, A18, C18, A20, C20	SerDes Core GND	—	—
L2_XPADVDD	D14, E16, F18, D19, E19	SerDes I/O Power (1.0 or 1.05 V)	—	—
L2_XPADVSS	D16, E17, D20	SerDes I/O GND	—	—
SPI Interface				
SPICLK/SD_CLK	AH9	I/O	OVDD	—

This table shows the heat sink thermal resistance for TePBGA II package with heat sinks, simulated in a standard JEDEC environment, per JESD 51-6.

Table 82. Thermal Resistance with Heat Sink in Open Flow (TePBGA II)

Heat Sink Assuming Thermal Grease	Air Flow	Thermal Resistance (°/W)
AAVID 30 × 30 × 9.4 mm Pin Fin	Natural Convection	13.1
	0.5 m/s	10.6
	1 m/s	9.3
	2 m/s	8.2
	4 m/s	7.5
AAVID 31 × 35 × 23 mm Pin Fin	Natural Convection	11.1
	0.5 m/s	8.5
	1 m/s	7.7
	2 m/s	7.2
	4 m/s	6.8
AAVID 43× 41× 16.5mm Pin Fin	Natural Convection	11.3
	0.5 m/s	9.0
	1 m/s	7.8
	2 m/s	7.0
	4 m/s	6.5
Wakefield, 53 × 53 × 25 mm Pin Fin	Natural Convection	9.7
	0.5 m/s	7.7
	1 m/s	6.8
	2 m/s	6.4
	4 m/s	6.1

Heat sink vendors include the following:

Aavid Thermalloy
www.aavidthermalloy.com

Alpha Novatech
www.alphanovatech.com

International Electronic Research Corporation (IERC)
www.ctscorp.com

Millennium Electronics (MEI)
www.mei-thermal.com

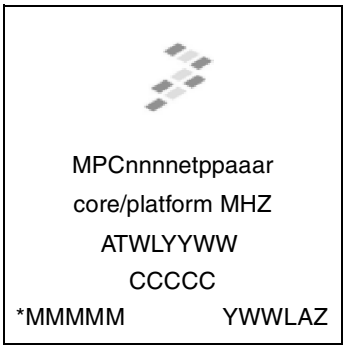
This table shows the SVR and PVR settings by device.

Table 86. SVR and PVR Settings by Product Revision

Device	Package	SVR		PVR	
		Rev 1.0	Rev. 2.1	Rev. 1.0	Rev. 2.1
MPC8377	TePBGA II	0x80C7_0010	0x80C7_0021	0x8086_1010	0x8086_1011
MPC8377E		0x80C6_0010	0x80C6_0021		
MPC8378		0x80C5_0010	0x80C5_0021		
MPC8378E		0x80C4_0010	0x80C4_0021		
MPC8379		0x80C3_0010	0x80C3_0021		
MPC8379E		0x80C2_0010	0x80C2_0021		

26.2 Part Marking

Parts are marked as in the example as shown in this figure.



TePBGA II

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 67. Freescale Part Marking for TePBGA II Devices

27 Document Revision History

This table provides a revision history for this document.

Table 87. Document Revision History

Revision	Date	Substantive Change(s)
8	05/2012	In Table 15, “DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V,” updated Output leakage current (I_{OZ}) min and max values.
7	10/2011	• In Table 84, “Part Numbering Nomenclature,” updated “Revision Level description”and added footnote 4.In Section 21.2.4, “AC Requirements for SerDes Reference Clocks,” modified the introductory sentence for Table 71, “SerDes Reference Clock Common AC Parameters.”