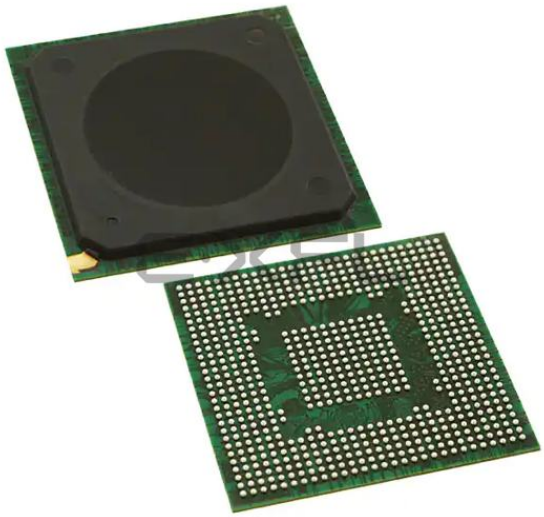

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c4s
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 125°C (TA)
Security Features	-
Package / Case	689-BBGA Exposed Pad
Supplier Device Package	689-TEPBGA II (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8377vralga

In addition to the security engine, new high-speed interfaces, such as PCI Express and SATA are included. This table compares the differences between MPC837xE derivatives and provides the number of ports available for each interface.

Table 1. High-Speed Interfaces on the MPC8377E, MPC8378E, and MPC8379E

Descriptions	MPC8377E	MPC8378E	MPC8379E
SGMII	0	2	0
PCI Express®	2	2	0
SATA	2	0	4

1.1 DDR Memory Controller

The DDR1/DDR2 memory controller includes the following features:

- Single 32- or 64-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 400-MHz data rate
- Support up to 4 chip selects
- 64-Mbit to 2-Gbit (for DDR1) and to 4-Gbit (for DDR2) devices with ×8/×16/×32 data ports (no direct ×4 support)
- Support for up to 32 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O

1.2 USB Dual-Role Controller

The USB controller includes the following features:

- Supports USB on-the-go mode, including both device and host functionality, when using an external ULPI (UTMI + low-pin interface) PHY
- Complies with *USB Specification, Rev. 2.0*
- Supports operation as a stand-alone USB device
  - Supports one upstream facing port
  - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - Supports USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation; low-speed operation is supported only in host mode
- Supports UTMI + low pin interface (ULPI)

8.1.1 MII, RMII, RGMII, and RTBI DC Electrical Characteristics

MII and RMII drivers and receivers comply with the DC parametric attributes specified in Table 24 and Table 25. The RGMII and RTBI signals in Table 25 are based on a 2.5 V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 24. MII and RMII DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage 3.3 V	LV_{DD1} LV_{DD2}	3.13	3.47	V	1
Output high voltage (LV_{DD1}/LV_{DD2} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.40	LV_{DD1}/LV_{DD2} + 0.3	V	—
Output low voltage (LV_{DD1}/LV_{DD2} = Min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.50	V	—
Input high voltage	V_{IH}	2.0	LV_{DD1}/LV_{DD2} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.90	V	—
Input high current (V_{IN} = LV_{DD1}, V_{IN} = LV_{DD2})	I_{IH}	—	30	µA	1
Input low current (V_{IN} = GND)	I_{IL}	–600	—	µA	—

Notes:
1. LV_{DD1} supports eTSEC 1. LV_{DD2} supports eTSEC 2.

Table 25. RGMII and RTBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage 2.5 V	LV_{DD1} LV_{DD2}	2.37	2.63	V	1
Output high voltage (LV_{DD1}/LV_{DD2} = Min, IOH = –1.0 mA)	V_{OH}	2.00	LV_{DD1}/LV_{DD2} + 0.3	V	—
Output low voltage (LV_{DD1}/LV_{DD2} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—
Input high voltage	V_{IH}	1.7	LV_{DD1}/LV_{DD2} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.70	V	—
Input high current (V_{IN} = LV_{DD1}, V_{IN} = LV_{DD2})	I_{IH}	—	–20	µA	1
Input low current (V_{IN} = GND)	I_{IL}	–20	—	µA	—

Notes:
1. LV_{DD1} supports eTSEC 1. LV_{DD2} supports eTSEC 2.

This figure shows the MII receive AC timing diagram.

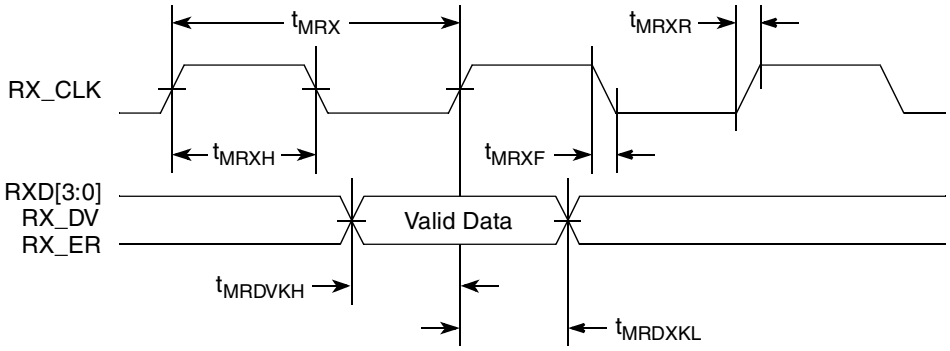

Figure 9. MII Receive AC Timing Diagram

8.2.2 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 28. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit	Note
Data to clock output skew (at transmitter)	t_{SKRGT}	–600	0	600	ps	—
Data to clock input skew (at receiver)	t_{SKRGT}	1.0	—	2.8	ns	2
Clock period	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 1000Base-T	t_{RGTH}/t_{RGT}	45	50	55	%	4
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns	—
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns	—
EC_GTX_CLK125 reference clock period	t_{G12}	—	8.0	—	ns	5
EC_GTX_CLK125 reference clock duty cycle measured at $0.5 \times LV_{DD1}$	t_{G125H}/t_{G125}	47	—	53	%	—

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between
5. This symbol represents the external EC_GTX_CLK125 and does not follow the original signal naming convention.

Table 42. eSDHC AC Timing Specifications for Full-Speed Mode (continued)

At recommended operating conditions OV_{DD} = 3.3 V ± 165 mV.

Parameter	Symbol[1]	Min	Max	Unit	Note
Input hold times: SD_CMD, SD_DAT*x*, SD_CD to SD_CLK	$t_{SFSIXKH}$	0	—	ns	2
SD_CLK delay within device	$t_{INT\_CLK\_DLY}$	1.5	—	ns	4
Output valid: SD_CLK to SD_CMD, SD_DAT*x* valid	$t_{SFSKHOV}$	—	4	ns	2
Output hold: SD_CLK to SD_CMD, SD_DAT*x* valid	$t_{SFSKHOX}$	0	—	—	—
SD card input setup	t_{ISU}	5	—	ns	3
SD card input hold	t_{IH}	5	—	ns	3
SD card output valid	t_{ODLY}	—	14	ns	3
SD card output hold	t_{OH}	0	—	ns	3

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{SFSIXKH}$ symbolizes eSDHC full mode speed device timing (SFS) input (I) to go invalid (X) with respect to the clock reference (K) going to high (H). Also $t_{SFSKHOV}$ symbolizes eSDHC full speed timing (SFS) for the clock reference (K) to go high (H), with respect to the output (O) going valid (V) or data output valid time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Measured at capacitive load of 40 pF.
3. For reference only, according to the SD card specifications.
4. Average, for reference only.

This figure provides the eSDHC clock input timing diagram.

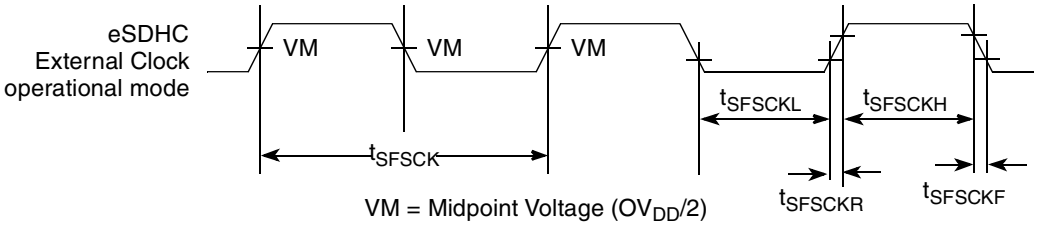

Figure 26. eSDHC Clock Input Timing Diagram

11.2.1 Full-Speed Output Path (Write)

This figure provides the data and command output timing diagram.

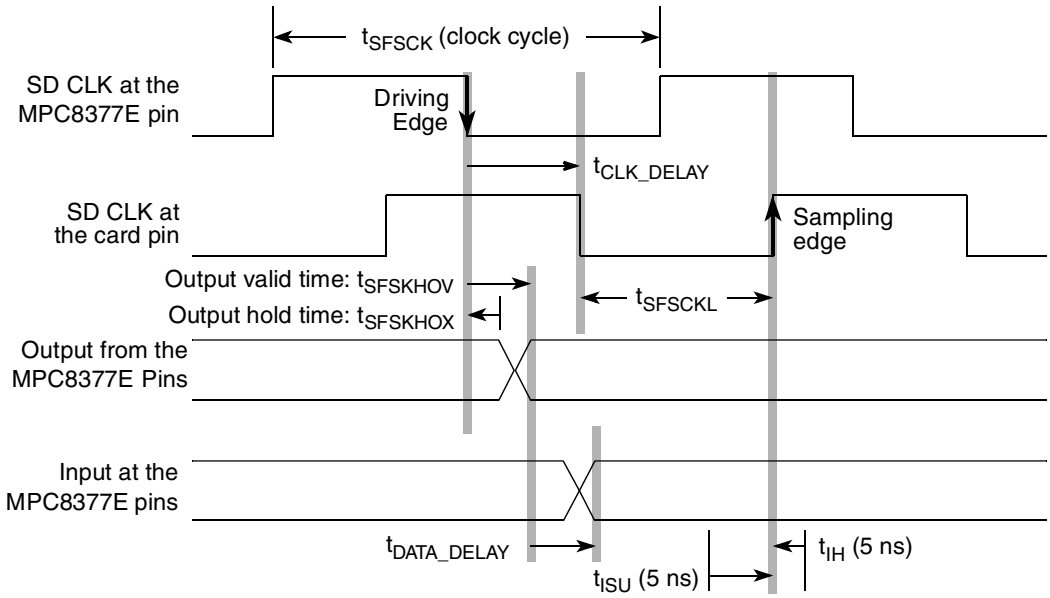

Figure 27. Full Speed Output Path

11.2.1.1 Full-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

No clock delay:

$$t_{SFSKHOV} + t_{DATA\_DELAY} + t_{ISU} < t_{SFSCKL} \quad \textit{Eqn. 1}$$

With clock delay:

$$t_{SFSKHOV} + t_{DATA\_DELAY} + t_{ISU} < t_{SFSCKL} + t_{CLK\_DELAY} \quad \textit{Eqn. 2}$$

$$t_{DATA\_DELAY} + t_{SFSCKL} < t_{SFSCK} + t_{CLK\_DELAY} - t_{ISU} - t_{SFSKHOV} \quad \textit{Eqn. 3}$$

This means that data can be delayed versus clock up to 11 ns in ideal case of t_{SFSCKL} = 20 ns:

$t_{DATA\_DELAY} + 20 < 40 + t_{CLK\_DELAY} - 5 - 4$

$t_{DATA\_DELAY} < 11 + t_{CLK\_DELAY}$

11.2.1.2 Full-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK\_DELAY} < t_{SFSCKL} + t_{SFSKHOX} + t_{DATA\_DELAY} - t_{IH} \quad \textit{Eqn. 4}$$

Table 45. JTAG AC Timing Specifications (Independent of CLKIN) [1] (continued)

Parameter	Symbol[2]	Min	Max	Unit	Note
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	5

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 Ω load (see Figure 17). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.

This figure provides the AC test load for TDO and the boundary-scan outputs of the device.

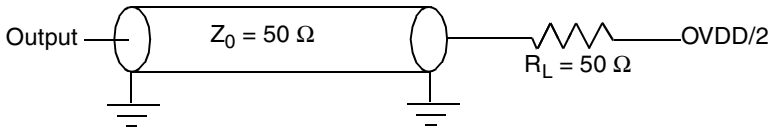

Figure 32. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

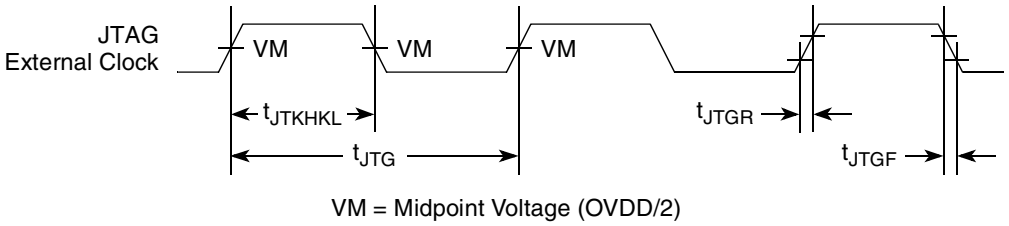

Figure 33. JTAG Clock Input Timing Diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.

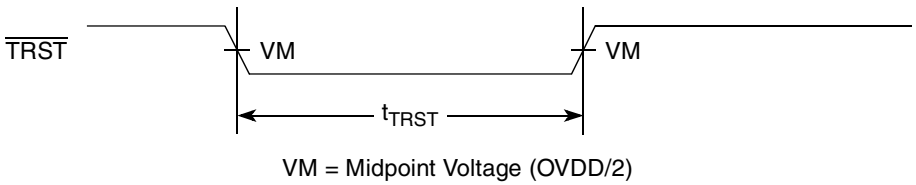

Figure 34. $\overline{\text{TRST}}$ Timing Diagram

14 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the chip.

14.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface of the device. The DC characteristics of the PORESET signal, which can be used as PCI RST in applications where the device is a PCI agent, deviates from the standard PCI levels.

Table 48. PCI DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
High-level input voltage	$V_{OUT} \geq V_{OH}$ (min) or	V_{IH}	2.0	OV_{DD} + 0.5	V
Low-level input voltage	$V_{OUT} \leq V_{OL}$ (max)	V_{IL}	–0.5	$0.3 \times OV_{DD}$	V
High-level output voltage	I_{OH} = –500 µA	V_{OH}	$0.9 \times OV_{DD}$	—	V
Low-level output voltage	I_{OL} = 1500 µA	V_{OL}	—	$0.1 \times OV_{DD}$	V
Input current	$0 V \leq V_{IN} \leq OV_{DD}$	I_{IN}	—	± 30	µA

Note:
- The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2.

14.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the device. Note that the PCI_CLK/PCI_SYNC_IN or CLKIN signal is used as the PCI input clock depending on whether the chip is configured as a host or agent device. CLKIN is used when the device is in host mode.

This table shows the PCI AC timing specifications at 66 MHz.

Table 49. PCI AC Timing Specifications at 66 MHz

PCI_SYNC_IN clock input levels are with next levels: VIL = $0.1 \times OV_{DD}$, VIH = $0.7 \times OV_{DD}$.

Parameter	Symbol[1]	Min	Max	Unit	Note
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from clock	t_{PCKHOX}	1	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4

15.2 AC Requirements for PCI Express SerDes Clocks

This table lists the PCI Express SerDes clock AC requirements.

Table 51. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements

Parameter	Symbol	Min	Typical	Max	Unit	Note
REFCLK cycle time	t_{REF}	—	10	—	ns	—
REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	t_{REFCJ}	—	—	100	ps	—
REFCLK phase jitter peak-to-peak. Deviation in edge location with respect to mean edge location.	t_{REFPJ}	–50	—	+50	ps	—
SD_REF_CLK/_B cycle to cycle clock jitter (period jitter)	t_{CKCJ}	—	—	100	ps	—
SD_REF_CLK/_B phase jitter peak-to-peak. Deviation in edge location with respect to mean edge location.	t_{CKPJ}	–50	—	+50	ps	2, 3

Notes:
1. All options provide serial interface bit rate of 1.5 and 3.0 Gbps.
2. In a frequency band from 150 kHz to 15 MHz, at BER of 10^{-12}.
3. Total peak-to-peak Deterministic Jitter "J_D" should be less than or equal to 50 ps.

15.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

15.4 Physical Layer Specifications

Following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer, use the *PCI Express Base Specification*, Rev. 1.0a.

NOTE

The voltage levels of the transmitter and the receiver depend on the SerDes control registers which should be programmed at the recommended values for PCI Express protocol (that is, L1_nV$_{DD}$ = 1.0 V).

Table 52. Differential Transmitter (Tx) Output Specifications (continued)

Parameter	Conditions	Symbol	Min	Typical	Max	Units	Note
Absolute delta of DC common mode between D+ and D–	$\lvert V_{TX\text{-}CM\text{-}DC\text{-}D+} - V_{TX\text{-}CM\text{-}DC\text{-}D-} \rvert \leq 25$ mV $V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D+} \rvert$ $V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D-} \rvert$	$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	0	—	25	mV	2
Electrical idle differential peak output voltage	$V_{PEEIDPTX} = \lvert V_{TX\text{-}IDLE\text{-}D+} - V_{TX\text{-}IDLE\text{-}D-} \rvert \leq 20$ mV	$V_{TX\text{-}IDLE\text{-}DIFFp}$	0	—	20	mV	2
Amount of voltage change allowed during receiver detection	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present.	$V_{TX\text{-}RCV\text{-}DETECT}$	—	$XPADV_{DD}/2$	600	mV	6
Tx DC common mode voltage	The allowed DC common mode voltage under any conditions.	$V_{TX\text{-}DC\text{-}CM}$	0	$XPADV_{DD}/2$	—	V	6
Tx short circuit current limit	The total current the transmitter can provide when shorted to its ground	$I_{TX\text{-}SHORT}$	—	—	90	mA	—
Minimum time spent in electrical idle	Minimum time a transmitter must be in electrical idle. Utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set.	$T_{TX\text{-}IDLE\text{-}MIN}$	50	—	—	UI	—
Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from LO.	$T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$	—	—	20	UI	—
Maximum time to transition to valid Tx specifications after leaving an electrical idle condition	Maximum time to meet all Tx specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the Tx to meet all Tx specifications after leaving electrical idle	$T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$	—	—	20	UI	—
Differential return loss	Measured over 50 MHz to 1.25 GHz.	$RL_{TX\text{-}DIFF}$	12	—	—	dB	4

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen1i or 1.5 Gbits/s transmission.

Table 56. Gen1i/1.5G Transmitter AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Channel speed	t_{CH_SPEED}	—	1.5	—	Gbps	—
Unit interval	T_{UI}	666.4333	666.667	670.2333	ps	—
Total jitter, data-data 5 UI	$U_{SATA\_TXTJ5UI}$	—	—	0.355	UI_{p-p}	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	—	—	0.47	UI_{p-p}	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	—	—	0.175	UI_{p-p}	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ250UI}$	—	—	0.22	UI_{p-p}	1

Note:
1. Measured at Tx output pins peak to peak phase variation, random data pattern.

16.2.2 Gen2i/3G Transmitter Specifications

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission.

Table 57. Gen 2i/3G Transmitter DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Tx differential output voltage	V_{SATA_TXDIFF}	400	550	700	mV_{p-p}	1
Tx differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	—

Note:
1. Terminated by 50 Ω load.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission.

Table 58. Gen 2i/3G Transmitter AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Channel speed	t_{CH_SPEED}	—	3.0	—	Gbps	—
Unit interval	T_{UI}	333.2	333.33	335.11	ps	—
Total jitter $f_{C3dB}=f_{BAUD}/10$	$U_{SATA\_TXTJfB/10}$	—	—	0.3	UI_{p-p}	1
Total jitter $f_{C3dB} = f_{BAUD}/500$	$U_{SATA\_TXTJfB/500}$	—	—	0.37	UI_{p-p}	1

Table 58. Gen 2i/3G Transmitter AC Specifications (continued)

Parameter	Symbol	Min	Typical	Max	Units	Note
Total jitter $f_{C3dB} = f_{BAUD}/1667$	$U_{SATA\_TXTJfB/1667}$	—	—	0.55	UI_{p-p}	1
Deterministic jitter $f_{C3dB} = f_{BAUD}/10$	$U_{SATA\_TXDJfB/10}$	—	—	0.17	UI_{p-p}	1
Deterministic jitter $f_{C3dB} = f_{BAUD}/500$	$U_{SATA\_TXDJfB/500}$	—	—	0.19	UI_{p-p}	1
Deterministic jitter $f_{C3dB} = f_{BAUD}/1667$	$U_{SATA\_TXDJfB/1667}$	—	—	0.35	UI_{p-p}	1

Note:
1. Measured at Tx output pins peak to peak phase variation, random data pattern.

16.3 Differential Receiver (Rx) Input Characteristics

This section discusses the Gen1i/1.5G and Gen2i/3G differential receiver input AC characteristics.

16.3.1 Gen1i/1.5G Receiver Specifications

This table provides the Gen1i or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 59. Gen1i/1.5G Receiver Input DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Differential input voltage	V_{SATA_RXDIFF}	240	500	600	mV_{p-p}	1
Differential Rx input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	—

Note:
1. Voltage relative to common of either signal comprising a differential pair.

This table provides the Gen1i or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface.

Table 60. Gen 1i/1.5G Receiver AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Unit interval	T_{UI}	666.4333	666.667	670.2333	ps	—
Total jitter, data-data 5 UI	$U_{SATA\_TXTJ5UI}$	—	—	0.43	UI_{p-p}	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	—	—	0.60	UI_{p-p}	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	—	—	0.25	UI_{p-p}	1

— The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.

- The maximum average current requirement that also determines the common mode voltage range
  — When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  — This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND_SRDS*n* (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  — If the device driving the SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ inputs cannot drive 50 Ω to SGND_SRDS*n* (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  — This requirement is described in detail in the following sections.

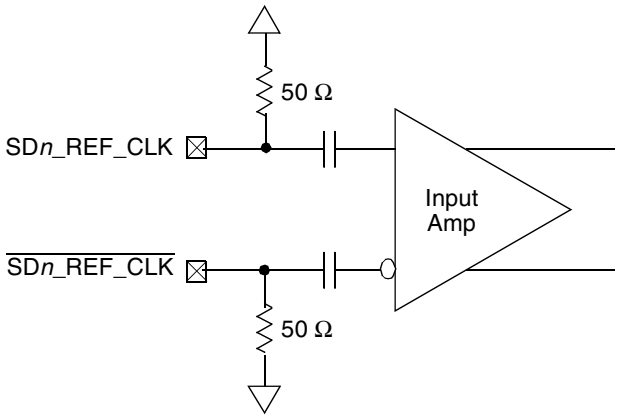

Figure 52. Receiver of SerDes Reference Clocks

21.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the device SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  — The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and

output driver features a 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

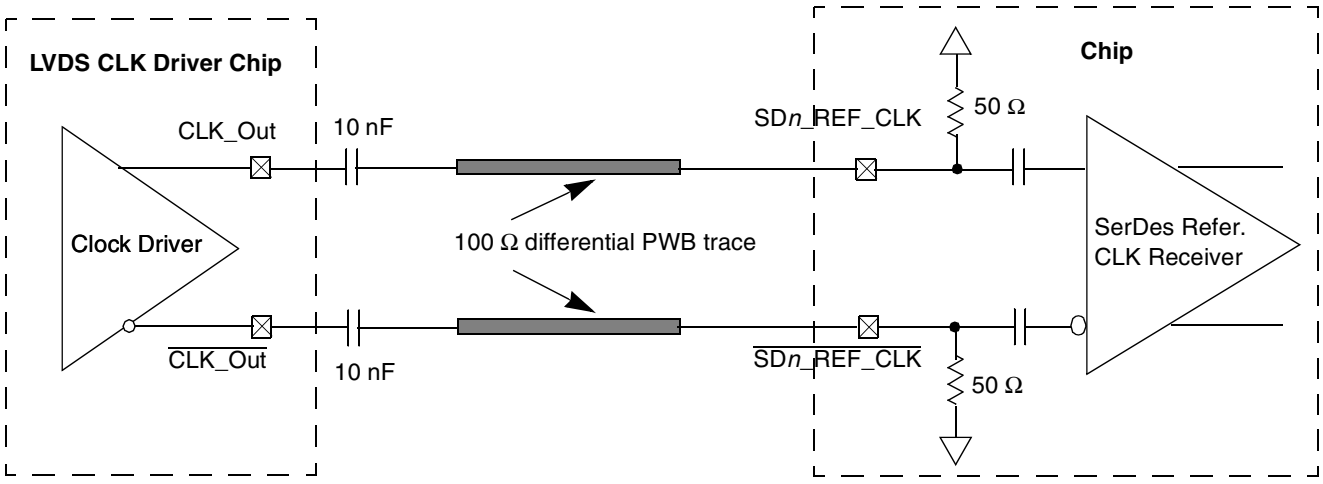

Figure 57. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 58 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with device SerDes reference clock input's DC requirement, AC-coupling has to be used. Figure 58 assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 Ω to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50 Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the device SerDes reference clock's differential input amplitude requirement (between 200 mV and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Consult clock

driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

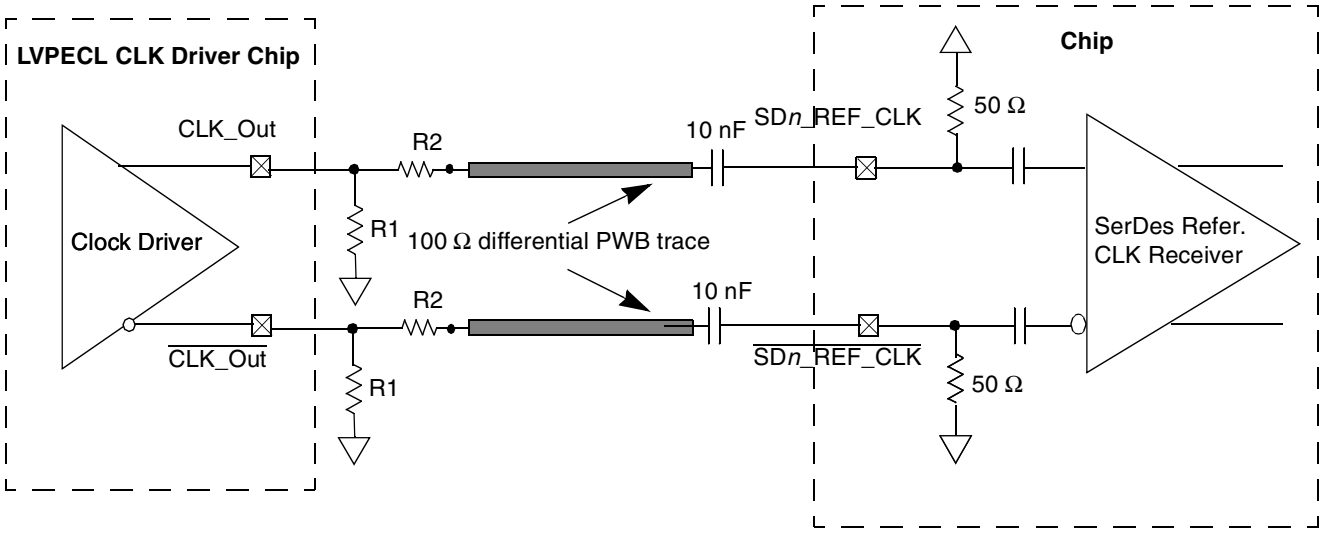

Figure 58. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with device SerDes reference clock input's DC requirement.

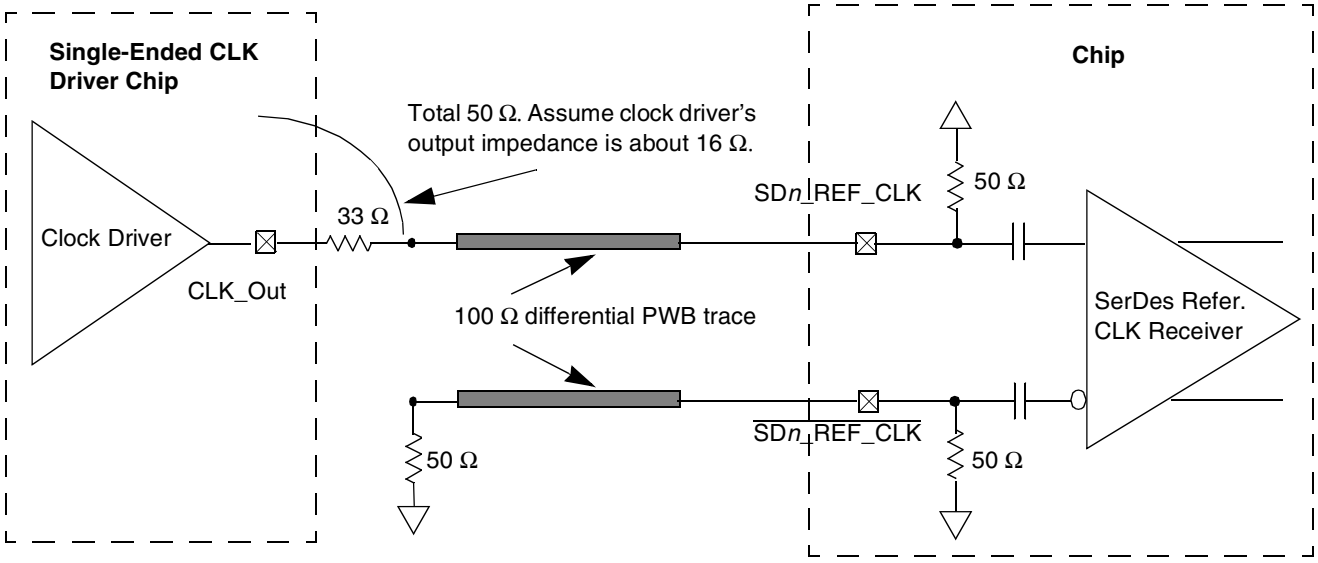

Figure 59. Single-Ended Connection (Reference Only)

21.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 KHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MBA2	M3	O	GVDD	—
MCAS_B	W5	O	GVDD	—
MCK_B0	H1	O	GVDD	—
MCK_B1	K1	O	GVDD	—
MCK_B2	V1	O	GVDD	—
MCK_B3	W2	O	GVDD	—
MCK_B4	AA1	O	GVDD	—
MCK_B5	AB2	O	GVDD	—
MCK0	J1	O	GVDD	—
MCK1	L1	O	GVDD	—
MCK2	V2	O	GVDD	—
MCK3	W1	O	GVDD	—
MCK4	Y1	O	GVDD	—
MCK5	AB1	O	GVDD	—
MCKE0	M4	O	GVDD	3
MCKE1	R5	O	GVDD	3
MCS_B0	W3	O	GVDD	—
MCS_B1	P3	O	GVDD	—
MCS_B2	T4	O	GVDD	—
MCS_B3	R4	O	GVDD	—
MDIC0	AH8	I/O	GVDD	9
MDIC1	AJ8	I/O	GVDD	9
MDM0	B6	O	GVDD	—
MDM1	B2	O	GVDD	—
MDM2	E2	O	GVDD	—
MDM3	E1	O	GVDD	—
MDM4	Y6	O	GVDD	—
MDM5	AC6	O	GVDD	—
MDM6	AE6	O	GVDD	—
MDM7	AJ4	O	GVDD	—
MDM8	L6	O	GVDD	—
MDQ0	A8	I/O	GVDD	11
MDQ1	A6	I/O	GVDD	11

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
UART_RTS_B[2]	L29	O	OVDD	—
Enhanced Local Bus Controller (eLBC) Interface				
LAD0	E24	I/O	LBVDD	—
LAD1	G28	I/O	LBVDD	—
LAD2	H25	I/O	LBVDD	—
LAD3	F26	I/O	LBVDD	—
LAD4	C26	I/O	LBVDD	—
LAD5	J28	I/O	LBVDD	—
LAD6	F21	I/O	LBVDD	—
LAD7	F23	I/O	LBVDD	—
LAD8	E25	I/O	LBVDD	—
LAD9	E26	I/O	LBVDD	—
LAD10	A23	I/O	LBVDD	—
LAD11	F24	I/O	LBVDD	—
LAD12	G24	I/O	LBVDD	—
LAD13	F25	I/O	LBVDD	—
LAD14	H28	I/O	LBVDD	—
LAD15	G25	I/O	LBVDD	—
LA11/LAD16	F27	I/O	LBVDD	—
LA12/LAD17	B21	I/O	LBVDD	—
LA13/LAD18	A25	I/O	LBVDD	—
LA14/LAD19	C28	I/O	LBVDD	—
LA15/LAD20	H24	I/O	LBVDD	—
LA16/LAD21	E23	I/O	LBVDD	—
LA17/LAD22	B28	I/O	LBVDD	—
LA18/LAD23	D28	I/O	LBVDD	—
LA19/LAD24	A27	I/O	LBVDD	—
LA20/LAD25	C25	I/O	LBVDD	—
LA21/LAD26	B27	I/O	LBVDD	—
LA22/LAD27	H27	I/O	LBVDD	—
LA23/LAD28	E21	I/O	LBVDD	—
LA24/LAD29	F20	I/O	LBVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
LA25/LAD30	D29	I/O	LBVDD	—
LA26/LAD31	E20	I/O	LBVDD	—
LA27	H26	O	LBVDD	—
LA28	C29	O	LBVDD	—
LA29	E28	O	LBVDD	—
LA30	B26	O	LBVDD	—
LA31	J25	O	LBVDD	—
LA10/LALE	H29	O	LBVDD	—
LBCTL	A22	O	LBVDD	—
LCLK0	B22	O	LBVDD	—
LCLK1	C23	O	LBVDD	—
LCLK2	B23	O	LBVDD	—
LCS_B0	D25	O	LBVDD	—
LCS_B1	F19	O	LBVDD	—
LCS_B2	C27	O	LBVDD	—
LCS_B3	D24	O	LBVDD	—
LCS_B4/LDP0	C24	I/O	LBVDD	—
LCS_B5/LDP1	B29	I/O	LBVDD	—
LA7/LCS_B6/LDP2	E29	I/O	LBVDD	—
LA8/LCS_B7/LDP3	F29	I/O	LBVDD	—
LFCLE/LGPL0	D21	O	LBVDD	—
LFALE/LGPL1	A26	O	LBVDD	—
LFRE_B/LGPL2/LOE_B	F22	O	LBVDD	—
LFWP_B/LGPL3	C21	O	LBVDD	—
LGPL4/LFRB_B/LGTA_B/ LUPWAIT/LPBSE	J29	I/O	LBVDD	16
LA9/LGPL5	G29	O	LBVDD	—
LSYNC_IN	A21	I	LBVDD	—
LSYNC_OUT	D23	O	LBVDD	—
LWE_B0/LFWE0/LBS_B0	E22	O	LBVDD	—
LWE_B1/LFWE1/LBS_B1	B25	O	LBVDD	—
LWE_B2/LFWE2/LBS_B2	E27	O	LBVDD	—
LWE_B3/LFWE3/LBS_B3	F28	O	LBVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
GND (VSS)	A1, AJ1, H2, N2, AA2, AD2, D3, R3, AF3, A4, F4, J4, L4, V4, Y4, AB4, B5, E5, P5, AH5, K6, T6, AA6, AD6, AG6, F7, J7, Y7, AJ7, B8, AE8, AG8, G9, AC9,B11, D11, F11, L11, M11, N11, P11, T11, U11, V11, W11,L12, M12, N12, P12, R12, T12, U12, V12, W12, E12, E13, L13, M13, N13, P13, R13, T13, U13, V13, W13, AE13, AJ13, F14, L14, M14, N14, P14, R14, T14, U14, V14, W14, M15, N15, P15, R15, T15, U15, V15, L16, M16, N16, P16, R16, T16, U16, V16, W16, L17, M17, N17, P17, R17, T17, U17, V17, W17, L18, M18, N18, P18, R18, T18, U18, V18, W18, L19, M19, N19, P19, T19, U19, V19, W19, AC20, G21, AF21, C22, J23, AA23, AJ23, B24, W24, AF24, K25, R25, AD25, D26, G27, M27, T27, Y27, AB27, AG27, A29, AJ29	—	—	—
AVDD_C	AD13	Power for e300 core PLL (1.0 V or 1.05 V)	—	15
AVDD_L	F13	Power for eLBC PLL (1.0 V or 1.05 V)	—	15
AVDD_P	F12	Power for system PLL (1.0 V or 1.05 V)	—	15
GVDD	A2, D2, R2, U2, AC2, AF2, AJ2, F3, H3, L3, N3, Y3, AB3, B4, P4, AF4, AH4, C5, F5, K5, V5, AA5, AD5, N6, R6, AJ6, B7, E7, K7, AA7, AE7, AG7, AD8	Power for DDR SDRAM I/O Voltage (2.5 or 1.8 V)	GVDD	—
OVDD	AC10, AF12, AJ12, K23, Y23, R24, AD24, L25, W25, AB26, U27, M28, Y28, G10, A11, C11	PCI, USB, and other Standard (3.3 V)	OVDD	—
No Connect				
NC	F16, F17, AD16, AD17	—	—	8
Pull Down				

Tyco Electronics
Chip Coolers™
www.chipcoolers.com

Wakefield Engineering
www.wakefield.com

Interface material vendors include the following:

Chomerics, Inc.
www.chomerics.com

Dow-Corning Corporation
Dow-Corning Electronic Materials
www.dowcorning.com

Shin-Etsu MicroSi, Inc.
www.microsi.com

The Bergquist Company
www.bergquistcompany.com

24.3 Heat Sink Attachment

The device requires the use of heat sinks. When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum compressive force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

24.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction to case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_J = junction temperature (°C)

T_C = case temperature of the package (°C)

Table 87. Document Revision History (continued)

Revision	Date	Substantive Change(s)
2	10/2009	• In Table 3, “Recommended Operating Conditions,” added “Operating temperature range” values. • In Table 5, “Power Dissipation [1],” corrected maximal application for 800/400 MHz to 4.3 W. • In Table 5, “Power Dissipation [1],” added a column for “Typical Application at T_j = 65°C (W)”. • In Table 5, “Power Dissipation [1],” added a column for “Sleep Power at T_j = 65°C (W)”. • In Table 11, removed overbar from CFG_CLKIN_DIV. • In Table 17, “Current Draw Characteristics for MV_{REF},” updated I_{MVREF} maximum value for both DDR1 and DDR2 to 600 and 400 µA, respectively. Also, updated Note 1 and added Note 2. • In Table 20, “DDR1 and DDR2 SDRAM Input AC Timing Specifications,” column headings renamed to “Min” and “Max”. Footnote 2 updated to state “T is the MCK clock period”. • In Table 20, “DDR1 and DDR2 SDRAM Input AC Timing Specifications,” and Table 21, “DDR1 and DDR2 SDRAM Output AC Timing Specifications,” clarified that the frequency parameters are data rates. • In Table 29, “RMII Transmit AC Timing Specifications,” updated t_{RMTDX}I to 2.0 ns. • In Table 60, Gen 1i/1.5G Transmitter AC Specifications,” and Table 62, Gen 2i/3G Transmitter AC Specifications,” corrected titles from “Transmitter” to “Receiver”. • In Table 72, “TePBGA II Pinout Listing,” removed pin THERM0; it is now Reserved. Also added 1.05 V to VDD pin. • In Table 74, “Operating Frequencies for TePBGA II,” corrected “DDR2 memory bus frequency (MCK)” range to 125–200. • In Table 79, “e300 Core PLL Configuration,” added 3.5:1 and 4:1 core_clk: csb_clk ratio options. • In Table 80, “Example Clock Frequency Combinations,” updated column heading to “DDR data rate” . • In Section 20.2, “SPI AC Timing Specifications,” corrected t_{NIKHOX} and t_{NEKHOX} to t_{NIKHOV} and t_{NEKHOV}, respectively.
1	02/2009	• In Table 3, “Recommended Operating Conditions,” added two new rows for 800 MHz, and created two rows for SerDes. In addition, changed 666 to 667 MHz. • In Table 5, “Power Dissipation [1],” added Notes 4 and 5. In addition, changed 666 to 667 MHz. • In Table 13, “DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V,” Table 21, “DDR1 and DDR2 SDRAM Output AC Timing Specifications,” and Table 72, “TePBGA II Pinout Listing,” added footnote to references to MVREF, MDQ, and MDQS, referencing AN3665, *MPC837xE Design Checklist*. • In Table 21, updated t_{DDKHCX} minimum value for 333 MHz to 2.40. • In Table 72, “TePBGA II Pinout Listing,” added footnote to USBDR_STP_SUSPEND and modified footnote 10 and added footnote 14. • In Table 74, “Operating Frequencies for TePBGA II,” changed 667 to 800 MHz for *core_clk*. • In Table 80, “Example Clock Frequency Combinations,” added 800 MHz cells for e300 core. • Updated part numbering information in AF column in Table 84, “Part Numbering Nomenclature.” In addition, modified extended temperature information in notes 1 and 4. • In Table 85, “Available Parts (Core/DDR Data Rate),” added new row for 800/400 MHz.
0	12/2008	Initial public release.