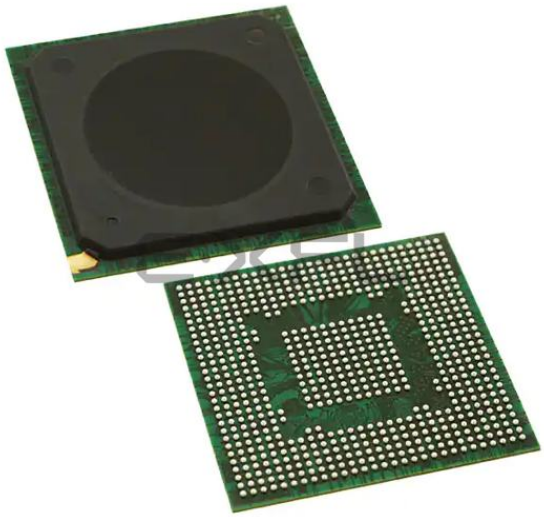

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c4s
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 125°C (TA)
Security Features	-
Package / Case	689-BBGA Exposed Pad
Supplier Device Package	689-TEPBGA II (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8377vrang

1.3 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The eTSECs include the following features:

- Two enhanced Ethernet interfaces can be used for RGMII/MII/RMII/RTBI
- Two controllers conform to IEEE Std 802.3®, IEEE 802.3u, IEEE 802.3x, IEEE 802.3z, IEEE 802.3au, IEEE 802.3ab, and IEEE Std 1588™ standards
- Support for Wake-on-Magic Packet™, a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status

1.4 Integrated Programmable Interrupt Controller (IPIC)

The integrated programmable interrupt controller (IPIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The IPIC programming model is compatible with the MPC8260 interrupt controller, and it supports 8 external and 34 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

1.5 Power Management Controller (PMC)

The power management controller includes the following features:

- Provides power management when the device is used in both host and agent modes
- Supports PCI Power Management 1.2 D0, D1, D2, and D3hot states
- Support for PME generation in PCI agent mode, PME detection in PCI host mode
- Supports Wake-on-LAN (Magic Packet), USB, GPIO, and PCI (PME input as host)
- Supports MPC8349E backward-compatibility mode

1.6 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) allows the device to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit.

1.7 DMA Controller, Dual I^2C, DUART, Enhanced Local Bus Controller (eLBC), and Timers

The device provides an integrated four-channel DMA controller with the following features:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors (accessible by local masters)
- Supports misaligned transfers

1.12 Enhanced Secured Digital Host Controller (eSDHC)

The enhanced SD host controller (eSDHC) has the following features:

- Conforms to *SD Host Controller Standard Specification, Rev 2.0* with Test Event register support.
- Compatible with the *MMC System Specification, Rev 4.0*
- Compatible with the *SD Memory Card Specification, Rev 2.0*, and supports High Capacity SD memory cards
- Compatible with the *SDIO Card Specification Rev, 1.2*
- Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC*plus*, MMC 4x, and RS-MMC cards
- SD bus clock frequency up to 50 MHz
- Supports 1-/4-bit SD and SDIO modes, 1-/4-bit MMC modes
- Supports internal DMA capabilities

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the chip. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Characteristic	Symbol	Max Value	Unit	Note
Core supply voltage	V_{DD}	–0.3 to 1.1	V	—
PLL supply voltage (e300 core, eLBC, and system)	AV_{DD}	–0.3 to 1.1	V	—
DDR1 and DDR2 DRAM I/O voltage	GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
Three-speed Ethernet I/O, MII management voltage	LV_{DD}[1,2]	–0.3 to 3.63	V	—
PCI, DUART, system control and power management, I^2C, and JTAG I/O voltage	OV_{DD}	–0.3 to 3.63	V	—
Local bus	LBV_{DD}	–0.3 to 3.63	V	—
SerDes	L[1,2]_nV_{DD}	–0.3 to 1.1	V	6

Table 5. Power Dissipation [1] (continued)

Core Frequency (MHz)	CSB/DDR Frequency (MHz)	Sleep Power at T_j = 65°C (W) [2]	Typical Application at T_j = 65°C (W) [2]	Typical Application at T_j = 125°C (W) [3]	Max Application at T_j = 125°C (W) [4]
600	400	1.45	2.1	3.4	4.1
	300	1.45	2.0	3.3	4.0
667	333	1.45	2.1	3.3	4.1
	266	1.45	2.0	3.3	3.9
800	400	1.45	2.5	3.8	4.3

Notes:
1. The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 6.
2. Typical power is based on a voltage of V_{DD} = 1.0 V for core frequencies ≤ 667 MHz or V_{DD} = 1.05 V for core frequencies of 800 MHz, and running a Dhrystone benchmark application.
3. Typical power is based on a voltage of V_{DD} = 1.0 V for core frequencies ≤ 667 MHz or V_{DD} = 1.05 V for core frequencies of 800 MHz, and running a Dhrystone benchmark application.
4. Maximum power is based on a voltage of V_{DD} = 1.0 V for core frequencies ≤ 667 MHz or V_{DD} = 1.05 V for core frequencies of 800 MHz, worst case process, and running an artificial smoke test.

This table shows the estimated typical I/O power dissipation for the device.

Table 6. Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD}/LBV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	L[1,2]_$n$$V_{DD}$ (1.0 V)	Unit	Comments
DDR I/O 65% utilization 2 pair of clocks	200 MHz data rate, 32-bit	0.28	0.35	—	—	—	—	W	—
	200 MHz data rate, 64-bit	0.41	0.49	—	—	—	—	W	
	266 MHz data rate, 32-bit	0.31	0.4	—	—	—	—	W	
	266 MHz data rate, 64-bit	0.46	0.56	—	—	—	—	W	
	300 MHz data rate, 32-bit	0.33	0.43	—	—	—	—	W	
	300 MHz data rate, 64-bit	0.48	0.6	—	—	—	—	W	
	333 MHz data rate, 32-bit	0.35	0.45	—	—	—	—	W	
	333 MHz data rate, 64-bit	0.51	0.64	—	—	—	—	W	
	400 MHz data rate, 32-bit	0.38	—	—	—	—	—	W	
	400 MHz data rate, 64-bit	0.56	—	—	—	—	—	W	

4.1 DC Electrical Characteristics

This table provides the clock input (CLKIN/PCI_CLK) DC timing specifications for the device.

Table 7. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit	Note
Input high voltage	—	V_{IH}	2.7	OV_{DD} + 0.3	V	1
Input low voltage	—	V_{IL}	–0.3	0.4	V	1
CLKIN Input current	0 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	± 10	μA	—
PCI_CLK Input current	0 V ≤ V_{IN} ≤ 0.5 V or OV_{DD} – 0.5 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	± 30	μA	—

Note:
1. In PCI agent mode, this specification does not comply with *PCI 2.3 Specification*.

4.2 AC Electrical Characteristics

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

Table 8. CLKIN AC Timing Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Note
CLKIN/PCI_CLK frequency	f_{CLKIN}	25	—	66.666	MHz	1, 6
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	40	ns	—
CLKIN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	± 150	ps	4, 5

Notes:
1. **Caution:** The system, core and security block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter-short term and long term-and is guaranteed by design.
5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be < 500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.
6. Spread spectrum is allowed up to 1% down-spread on CLKIN/PCI_CLK up to 60 KHz.

5.2 RESET AC Electrical Characteristics

This table provides the reset initialization AC timing specifications of the device.

Table 11. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of $\overline{\text{HRESET}}$ to activate reset flow	32	—	$t_{PCI\_SYNC\_IN}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the device is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_CLK when the device is in PCI agent mode	32	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ negation to negation (output)	16	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR config signals (CFG_RESET_SOURCE[0:3], CFG_CLKIN_DIV, and CFG_LBMUX) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR config signals (CFG_RESET_SOURCE[0:3], CFG_CLKIN_DIV, and CFG_LBMUX) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the device to turn off POR config signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the device to start driving functional output signals multiplexed with the POR configuration signals with respect to the negation of HRESET	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8379E Integrated Host Processor Reference Manual* for more details.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the device is in PCI host mode. See the *MPC8379E Integrated Host Processor Reference Manual* for more details.
3. POR config signals consists of CFG_RESET_SOURCE[0:3], CFG_LBMUX, and CFG_CLKIN_DIV.

Table 12 provides the PLL lock times.

Table 12. PLL Lock Times

Parameter	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

Note:

- The device guarantees the PLL lock if the clock settings are within spec range. The core clock also depends on the core PLL ratio. See Section 23, “Clocking,” for more information.

6 DDR1 and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the chip. Note that DDR1 SDRAM is GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

Table 22. DUART DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current, (0 V ≤V_{IN} ≤ OV_{DD})	I_{IN}	—	±30	µA

Note: The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2.

7.2 DUART AC Electrical Specifications

this table provides the AC timing parameters for the DUART interface of the device.

Table 23. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	256	baud	—
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate will be limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RGMII/RTBI/RMII DC Electrical Characteristics

The electrical characteristics specified here apply to media independent interface (MII), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), reduced media independent interface (RMII) signals, management data input/output (MDIO) and management data clock (MDC).

The MII and RMII interfaces are defined for 3.3 V, while the RGMII and RTBI interfaces can be operated at 2.5 V. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3*. The RMII interface follows the *RMII Consortium RMII Specification Version 1.2*.

8.2.3 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.3.1 RMII Transmit AC Timing Specifications

This table shows the RMII transmit AC timing specifications.

Table 29. RMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMTH}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

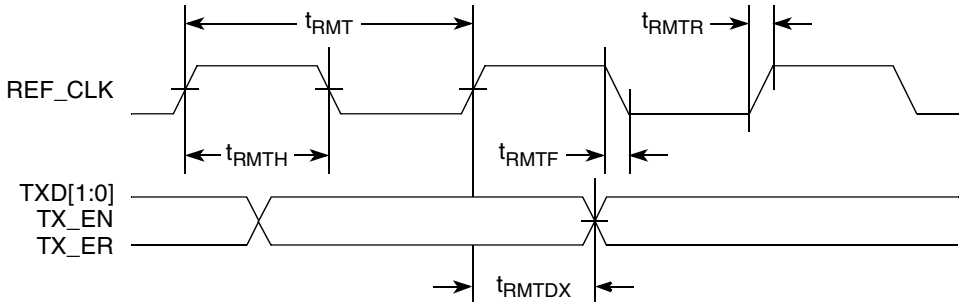


Figure 12. RMII Transmit AC Timing Diagram

9.2 USB AC Electrical Specifications

This table describes the general timing parameters of the USB interface of the device.

Table 35. USB General Timing Parameters (ULPI Mode Only)

Parameter	Symbol [1]	Min	Max	Unit	Note
USB clock cycle time	t_{USCK}	15	—	ns	2, 3, 4, 5
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	2, 3, 4, 5
Input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	2, 3, 4, 5
USB clock to output valid—all outputs	t_{USKHOV}	—	7	ns	2, 3, 4, 5
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	2, 3, 4, 5

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H) with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to the USB clock, USBDR_CLK.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

These two figures provide the AC test load and signals for the USB, respectively.

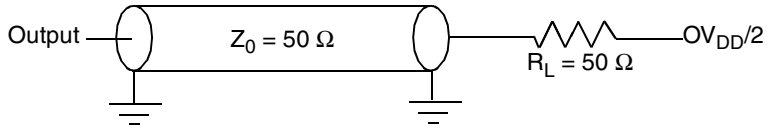


Figure 17. USB AC Test Load

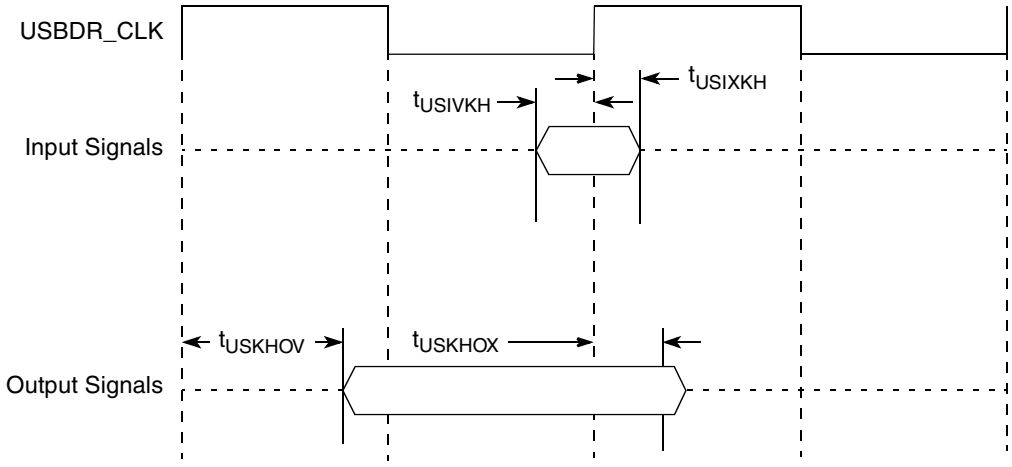


Figure 18. USB Interface Timing Diagram

11.2.1 Full-Speed Output Path (Write)

This figure provides the data and command output timing diagram.

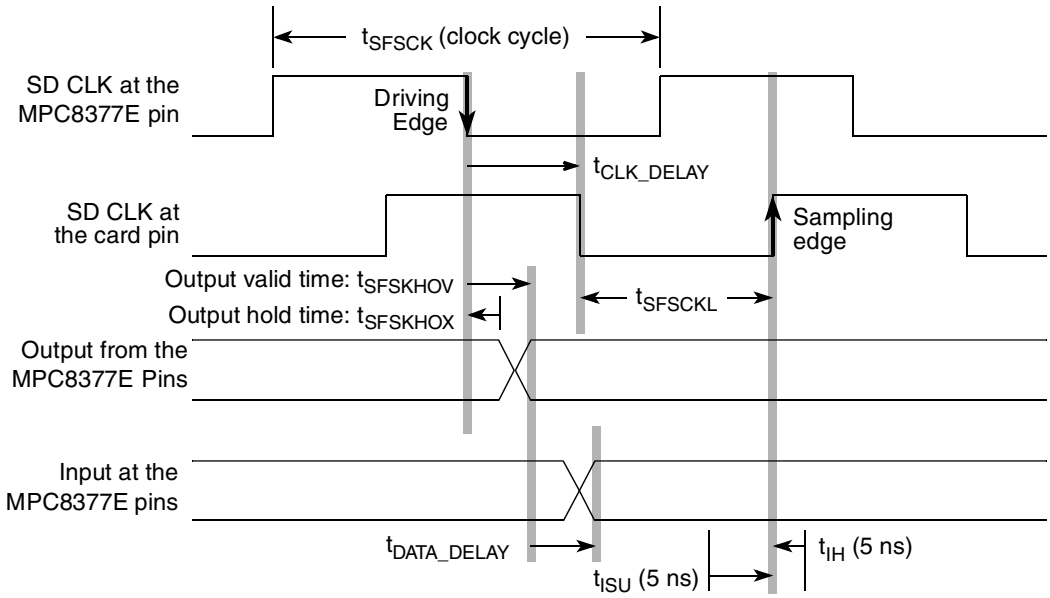


Figure 27. Full Speed Output Path

11.2.1.1 Full-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

No clock delay:

$$t_{SFSKHOV} + t_{DATA\_DELAY} + t_{ISU} < t_{SFSCKL} \quad \textit{Eqn. 1}$$

With clock delay:

$$t_{SFSKHOV} + t_{DATA\_DELAY} + t_{ISU} < t_{SFSCKL} + t_{CLK\_DELAY} \quad \textit{Eqn. 2}$$

$$t_{DATA\_DELAY} + t_{SFSCKL} < t_{SFSCK} + t_{CLK\_DELAY} - t_{ISU} - t_{SFSKHOV} \quad \textit{Eqn. 3}$$

This means that data can be delayed versus clock up to 11 ns in ideal case of t_{SFSCKL} = 20 ns:

$t_{DATA\_DELAY} + 20 < 40 + t_{CLK\_DELAY} - 5 - 4$

$t_{DATA\_DELAY} < 11 + t_{CLK\_DELAY}$

11.2.1.2 Full-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK\_DELAY} < t_{SFSCKL} + t_{SFSKHOX} + t_{DATA\_DELAY} - t_{IH} \quad \textit{Eqn. 4}$$

This means that data delay should be equal or less than the clock delay in the ideal case where $t_{SHSCLKL}$ = 10 ns:

$$t_{DATA\_DELAY} - t_{CLK\_DELAY} < 10 - 6 - 4$$
$$t_{DATA\_DELAY} - t_{CLK\_DELAY} < 0$$

11.3.1.2 High-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK\_DELAY} < t_{SHSCKL} + t_{SHSKHOX} + t_{DATA\_DELAY} - t_{IH} \quad \textit{Eqn. 13}$$

$$t_{CLK\_DELAY} - t_{DATA\_DELAY} < t_{SHSCKL} + t_{SHSKHOX} - t_{IH} \quad \textit{Eqn. 14}$$

This means that clock can be delayed versus data up to 8 ns (external delay line) in ideal case of $t_{SHSCLKL}$ = 10 ns:

$$t_{CLK\_DELAY} - t_{DATA\_DELAY} < 10 + 0 - 2$$
$$t_{CLK\_DELAY} - t_{DATA\_DELAY} < 8$$

11.3.2 High-Speed Input Path (Read)

This figure provides the data and command input timing diagram.

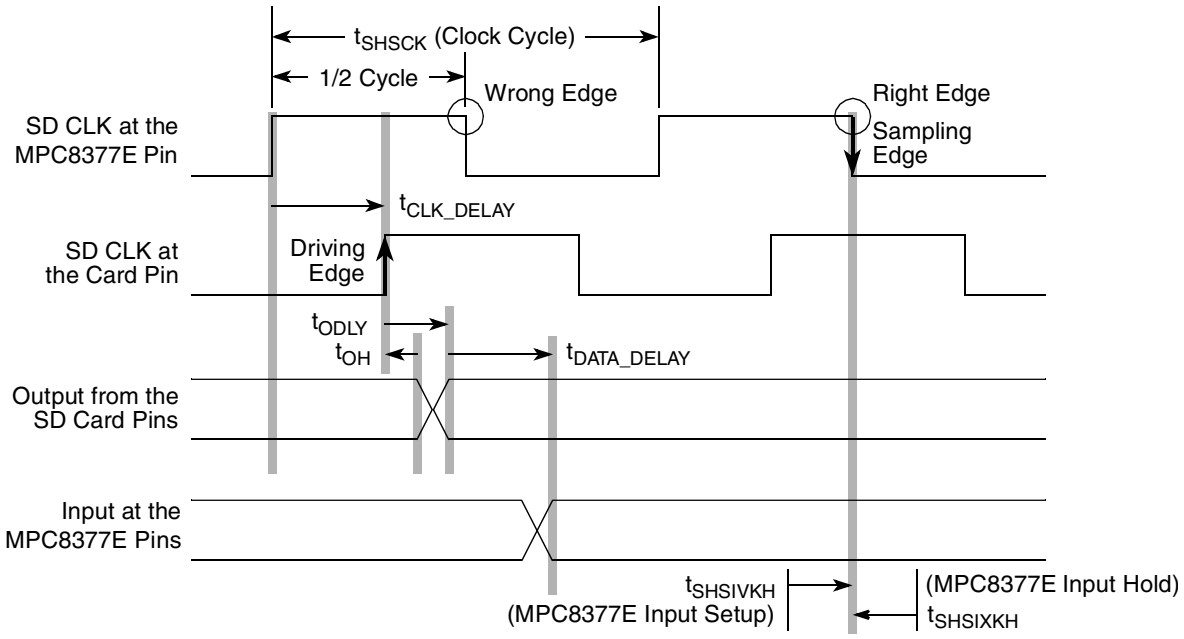


Figure 31. High-Speed Input Path

For the input path, the device eSDHC expects to sample the data 1.5 internal clock cycles after it was driven by the SD card. Since in this mode the SD card drives the data at the rising edge of the clock, a sufficient delay to the clock and the data must exist to ensure it will not be sampled at the wrong internal

13 I^2C

This section describes the DC and AC electrical characteristics for the I^2C interface of the chip.

13.1 I^2C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I^2C interface of the chip.

Table 46. I^2C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 165 mV.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current ($0 V \le V_{IN} \le OV_{DD}$)	I_{IN}	—	± 30	µA	4

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8379E PowerQUICC II Pro Integrated Host Processor Reference Manual* for information on the digital filter used.
4. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

13.2 I^2C AC Electrical Specifications

This table provides the AC timing parameters for the I^2C interface of the device.

Table 47. I^2C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 46).

Parameter	Symbol[1]	Min	Max	Unit	Note
SCL clock frequency	f_{I2C}	0	400	kHz	—
Low period of the SCL clock	t_{I2CL}	1.3	—	µs	—
High period of the SCL clock	t_{I2CH}	0.6	—	µs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	µs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	µs	—
Data setup time	t_{I2DVKH}	100	—	ns	—

14 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the chip.

14.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface of the device. The DC characteristics of the PORESET signal, which can be used as PCI RST in applications where the device is a PCI agent, deviates from the standard PCI levels.

Table 48. PCI DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
High-level input voltage	$V_{OUT} \geq V_{OH}$ (min) or	V_{IH}	2.0	OV_{DD} + 0.5	V
Low-level input voltage	$V_{OUT} \leq V_{OL}$ (max)	V_{IL}	–0.5	$0.3 \times OV_{DD}$	V
High-level output voltage	I_{OH} = –500 µA	V_{OH}	$0.9 \times OV_{DD}$	—	V
Low-level output voltage	I_{OL} = 1500 µA	V_{OL}	—	$0.1 \times OV_{DD}$	V
Input current	$0 V \leq V_{IN} \leq OV_{DD}$	I_{IN}	—	± 30	µA

Note:
- The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2.

14.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the device. Note that the PCI_CLK/PCI_SYNC_IN or CLKIN signal is used as the PCI input clock depending on whether the chip is configured as a host or agent device. CLKIN is used when the device is in host mode.

This table shows the PCI AC timing specifications at 66 MHz.

Table 49. PCI AC Timing Specifications at 66 MHz

PCI_SYNC_IN clock input levels are with next levels: VIL = $0.1 \times OV_{DD}$, VIH = $0.7 \times OV_{DD}$.

Parameter	Symbol[1]	Min	Max	Unit	Note
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from clock	t_{PCKHOX}	1	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4

Table 53. Differential Receiver (Rx) Input Specifications (continued)

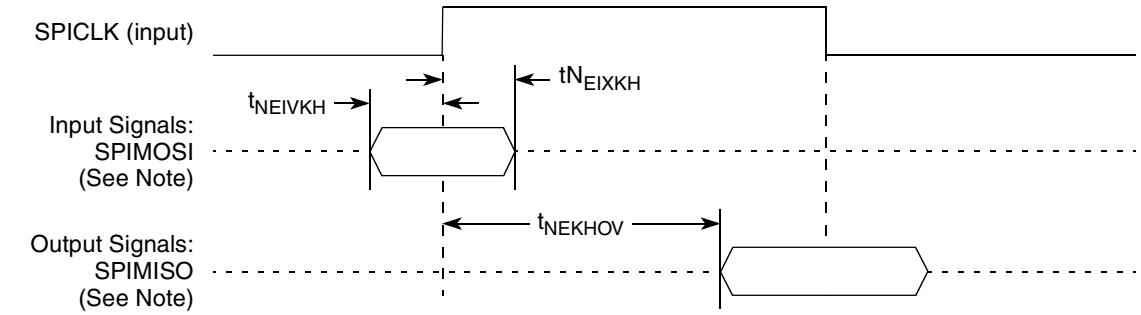
Parameter	Comments	Symbol	Min	Typical	Max	Units	Note
Unexpected Electrical Idle Enter Detect Threshold Integration Time	An unexpected electrical idle (Vrx-diffp-p < Vrx-idle-det-diffp-p) must be recognized no longer than Trx-idle-det-diff-entertime to signal an unexpected idle condition.	$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	—	—	10	ms	—
Total Skew	Skew across all lanes on a link. This includes variation in the length of SKP ordered set (e.g. COM and one to five SKP Symbols) at the Rx as well as any delay differences arising from the interconnect itself.	$L_{RX-SKEW}$	—	—	20	ns	—

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 44 should be used as the Rx device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 43). If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{Rx-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRx-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The receiver input impedance will result in a differential return loss greater than or equal to 10 dB with the D+ line biased to 300 mV and the D– line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 44). Note that the series capacitors, C_{Tx}, is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
6. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.
7. It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

15.5 Receiver Compliance Eye Diagrams

The Rx eye diagram in Figure 43 is specified using the passive compliance/test measurement load (see Figure 44) in place of any real PCI Express Rx component. In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 44) is larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics that cause the real PCI Express component to vary in impedance from the

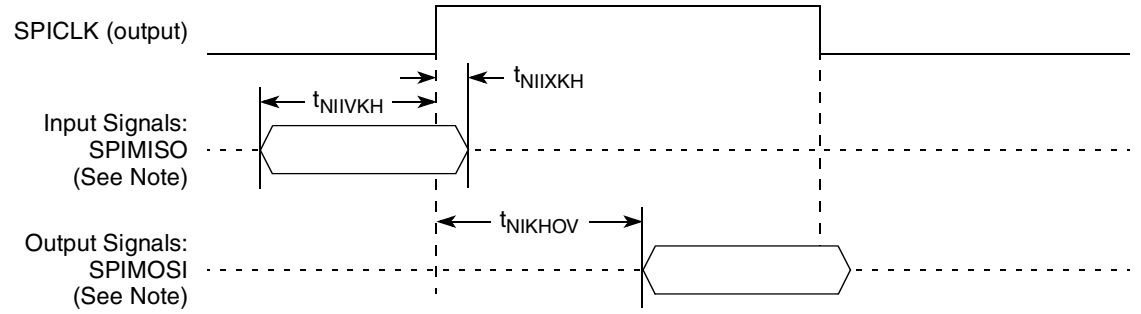
This figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 49. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 50. SPI AC Timing in Master Mode (Internal Clock) Diagram

21 High-Speed Serial Interfaces (HSSI)

This chip features two serializer/deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. See Table 1 for the interfaces supported.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

21.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 51 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{\_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$). Each signal swings between A volts and B volts where A > B.

driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

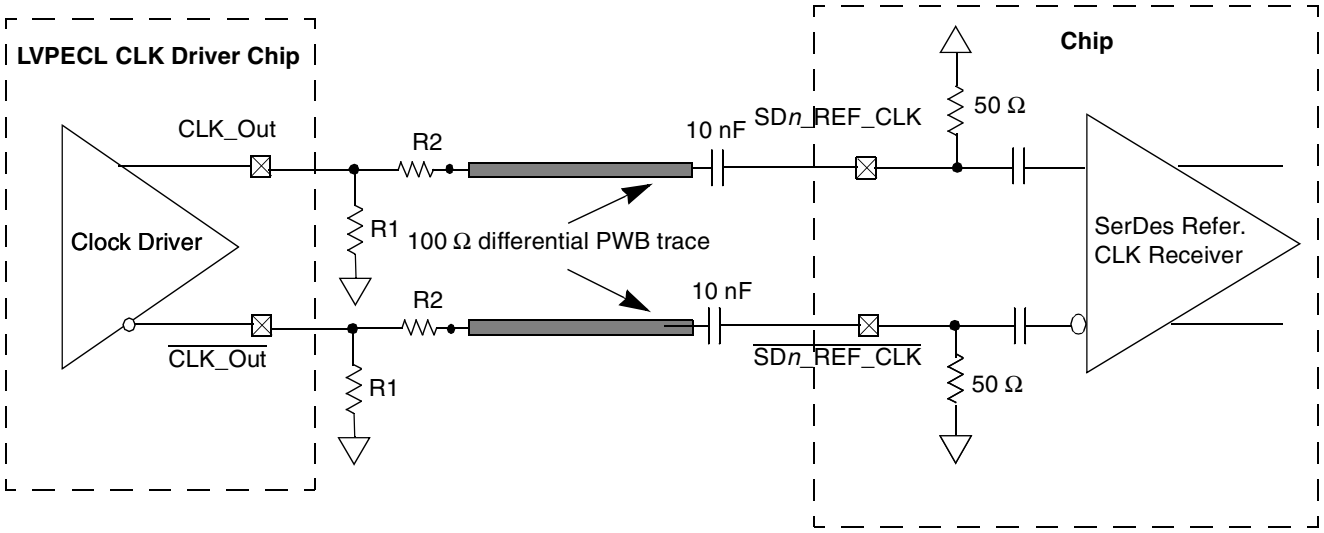


Figure 58. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with device SerDes reference clock input's DC requirement.

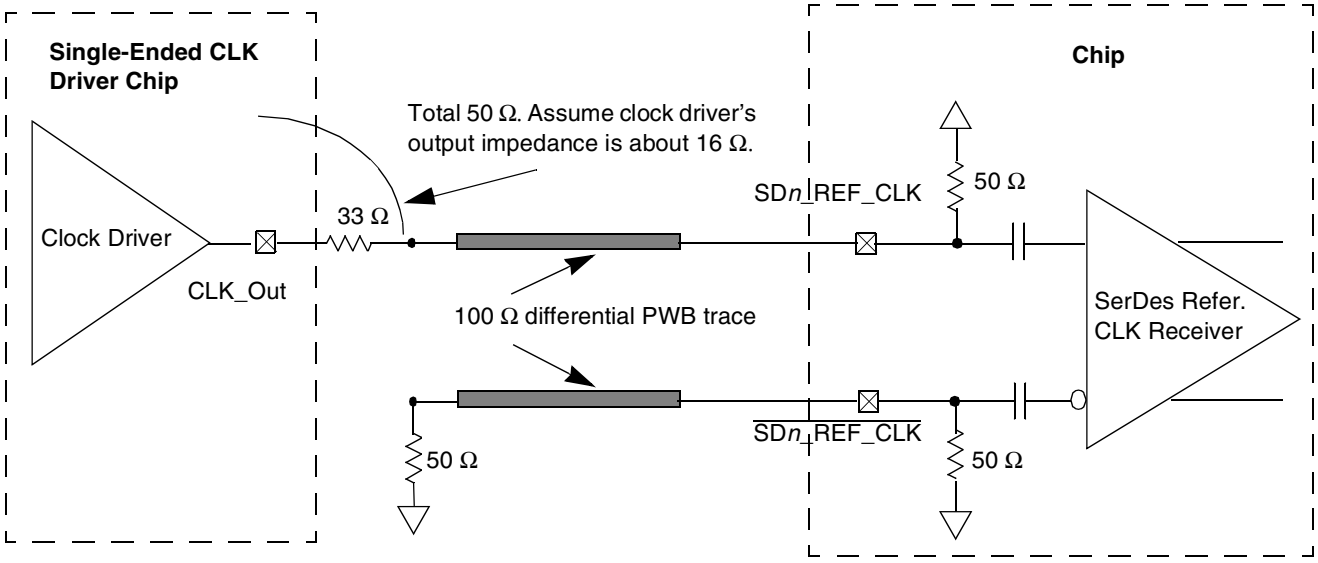


Figure 59. Single-Ended Connection (Reference Only)

21.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 KHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise

[5] Parallelism measurement should exclude any effect of mark on top surface of package.

22.2 Pinout Listings

This table provides the pinout listing for the TePBGA II package.

Table 72. TePBGA II Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Note
Clock Signals				
CLKIN	K24	I	OVDD	—
PCI_CLK/PCI_SYNC_IN	C10	I	OVDD	—
PCI_SYNC_OUT	N24	O	OVDD	3
PCI_CLK0	L24	O	OVDD	—
PCI_CLK1	M24	O	OVDD	—
PCI_CLK2	M25	O	OVDD	—
PCI_CLK3	M26	O	OVDD	—
PCI_CLK4	L26	O	OVDD	—
RTC/PIT_CLOCK	AF11	I	OVDD	—
DDR SDRAM Memory Interface				
MA0	U3	O	GVDD	—
MA1	U1	O	GVDD	—
MA2	T5	O	GVDD	—
MA3	T3	O	GVDD	—
MA4	T2	O	GVDD	—
MA5	T1	O	GVDD	—
MA6	R1	O	GVDD	—
MA7	P2	O	GVDD	—
MA8	P1	O	GVDD	—
MA9	N4	O	GVDD	—
MA10	V3	O	GVDD	—
MA11	M5	O	GVDD	—
MA12	N1	O	GVDD	—
MA13	M2	O	GVDD	—
MA14	M1	O	GVDD	—
MBA0	U5	O	GVDD	—
MBA1	U4	O	GVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MDQ2	C7	I/O	GVDD	11
MDQ3	D8	I/O	GVDD	11
MDQ4	A7	I/O	GVDD	11
MDQ5	A5	I/O	GVDD	11
MDQ6	A3	I/O	GVDD	11
MDQ7	C6	I/O	GVDD	11
MDQ8	D7	I/O	GVDD	11
MDQ9	E8	I/O	GVDD	11
MDQ10	B1	I/O	GVDD	11
MDQ11	D5	I/O	GVDD	11
MDQ12	B3	I/O	GVDD	11
MDQ13	D6	I/O	GVDD	11
MDQ14	C3	I/O	GVDD	11
MDQ15	C2	I/O	GVDD	11
MDQ16	D4	I/O	GVDD	11
MDQ17	E6	I/O	GVDD	11
MDQ18	F6	I/O	GVDD	11
MDQ19	G4	I/O	GVDD	11
MDQ20	F8	I/O	GVDD	11
MDQ21	E4	I/O	GVDD	11
MDQ22	C1	I/O	GVDD	11
MDQ23	G6	I/O	GVDD	11
MDQ24	F2	I/O	GVDD	11
MDQ25	G5	I/O	GVDD	11
MDQ26	H6	I/O	GVDD	11
MDQ27	H4	I/O	GVDD	11
MDQ28	D1	I/O	GVDD	11
MDQ29	G3	I/O	GVDD	11
MDQ30	H5	I/O	GVDD	11
MDQ31	F1	I/O	GVDD	11
MDQ32	W6	I/O	GVDD	11
MDQ33	AC1	I/O	GVDD	11
MDQ34	AC3	I/O	GVDD	11

This table shows the heat sink thermal resistance for TePBGA II package with heat sinks, simulated in a standard JEDEC environment, per JESD 51-6.

Table 82. Thermal Resistance with Heat Sink in Open Flow (TePBGA II)

Heat Sink Assuming Thermal Grease	Air Flow	Thermal Resistance (°/W)
AAVID 30 × 30 × 9.4 mm Pin Fin	Natural Convection	13.1
	0.5 m/s	10.6
	1 m/s	9.3
	2 m/s	8.2
	4 m/s	7.5
AAVID 31 × 35 × 23 mm Pin Fin	Natural Convection	11.1
	0.5 m/s	8.5
	1 m/s	7.7
	2 m/s	7.2
	4 m/s	6.8
AAVID 43× 41× 16.5mm Pin Fin	Natural Convection	11.3
	0.5 m/s	9.0
	1 m/s	7.8
	2 m/s	7.0
	4 m/s	6.5
Wakefield, 53 × 53 × 25 mm Pin Fin	Natural Convection	9.7
	0.5 m/s	7.7
	1 m/s	6.8
	2 m/s	6.4
	4 m/s	6.1

Heat sink vendors include the following:

Aavid Thermalloy
www.aavidthermalloy.com

Alpha Novatech
www.alphanovatech.com

International Electronic Research Corporation (IERC)
www.ctscorp.com

Millennium Electronics (MEI)
www.mei-thermal.com

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the VDD, OVDD, GVDD, and LVDD planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

25.3 Connection Recommendations

To ensure reliable operation, it is highly recommended that unused inputs be connected to an appropriate signal level. Unused active low inputs should be tied to OVDD, GVDD, or LVDD as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external VDD, GVDD, LVDD, OVDD, and GND pins of the device.

25.4 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OVDD or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 66). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

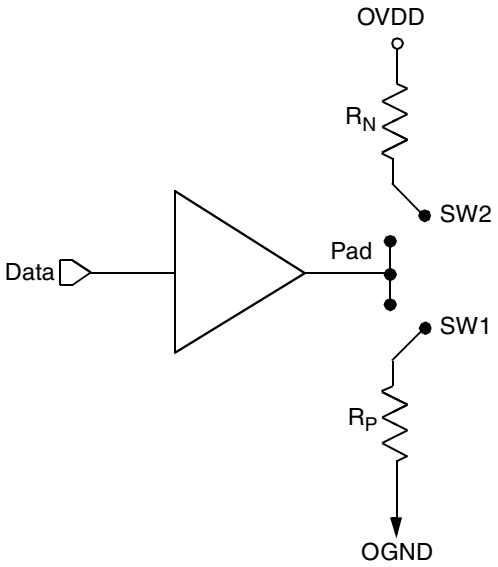


Figure 66. Driver Impedance Measurement

Table 87. Document Revision History (continued)

Revision	Date	Substantive Change(s)
6	07/2011	In Section 2.2, "Power Sequencing," updated power down sequencing information.
5	07/2011	• In Table 2, "Absolute Maximum Ratings[1]," removed footnote 5 from LB_{IN} to OV_{IN}. Also, corrected footnote 5. • In Table 3, "Recommended Operating Conditions," added footnote 2 to AV_{DD}. • In Figure 2, "Overshoot/Undershoot Voltage for $GV_{DD}/LV_{DD}/OV_{DD}/LBV_{DD}$," added LBV_{DD}. • In Table 13, "DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V," updated I_{OZ} min/max to –50/50. • In Figure 11, "RGMII and RTBI AC Timing and Multiplexing Diagrams," added distinction between t_{SKRGT_RX} and t_{SKRGT_TX} signals. • In Table 33, "MII Management AC Timing Specifications," updated MDC frequency—removed Min and Max values, added Typical value. Also, updated footnote 2 and removed footnote 3. • In Table 48, "PCI DC Electrical Characteristics," updated V_{IH} min value to 2.0. • In Table 72, "TePBGA II Pinout Listing," added Note to LGPL4/LFRB_B/LGTA_B/LUPWAIT/LPBSE (to be consistent with AN3665, "MPC837xE Design Checklist." • In Table 74, "Operating Frequencies for TePBGA II," added Minimum Operating Frequency for eTSEC, and corrected DDR2 Minimum and Maximum Operating Frequency values.
4	11/2010	• In Table 25, "RGMII and RTBI DC Electrical Characteristics," updated V_{IH} min value to 1.7. • In Table 40, "Local Bus General Timing Parameters—PLL Bypass Mode," added row for t_{LBKHLR}. • In Section 10.2, "Local Bus AC Electrical Specifications," and in Section 23, "Clocking," updated LCCR to LCRR. • In Table 72, "TePBGA II Pinout Listing," added SD_WP to pin C9. Also clarified TEST_SEL0 and TEST_SEL1 pins—no change in functionality.
3	03/2010	• Added Section 4.3, "eTSEC Gigabit Reference Clock Timing." • In Table 34, "USB DC Electrical Characteristics," and Table 35, "USB General Timing Parameters (ULPI Mode Only)," added table footnotes . • In Table 39, "Local Bus General Timing Parameters—PLL Enable Mode," and Table 40, "Local Bus General Timing Parameters—PLL Bypass Mode," corrected footnotes for $t_{LBOTOT1}$, $t_{LBOTOT2}$, $t_{LBOTOT3}$. • In Figure 22, "Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (PLL Enable Mode)," and Figure 24, "Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (PLL Enable Mode)," shifted "Input Signals: LAD[0:31]/LDP[0:3]" from the falling edge to the rising edge of LSYNC_IN. • In Figure 63, "Mechanical Dimensions and Bottom Surface Nomenclature of the TEPBGA II," added heat spreader. • In Section 25.6, "Pull-Up Resistor Requirements," removed "Ethernet Management MDIO pin" from list of open drain type pins. • In Table 72, "TePBGA II Pinout Listing," updated the Pin Type column for AVDD_C, AVDD_L, and AVDD_P pins. • in Table 72, "TePBGA II Pinout Listing," added Note 16 to eTSEC pins. • In Table 77, "CSB Frequency Options for Host Mode," and Table 78, "CSB Frequency Options for Agent Mode," updated *csb_clk* frequencies available. • In Table 84, "Part Numbering Nomenclature," removed footnote to "e300 core Frequency."