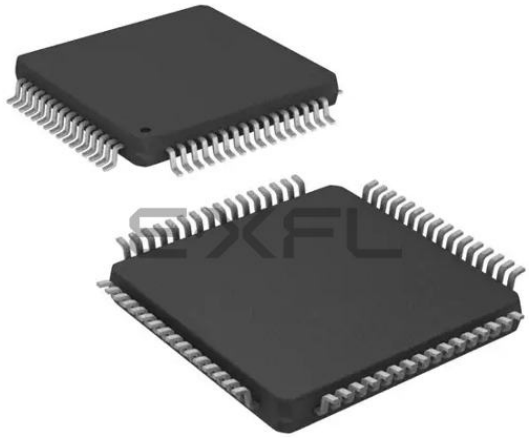

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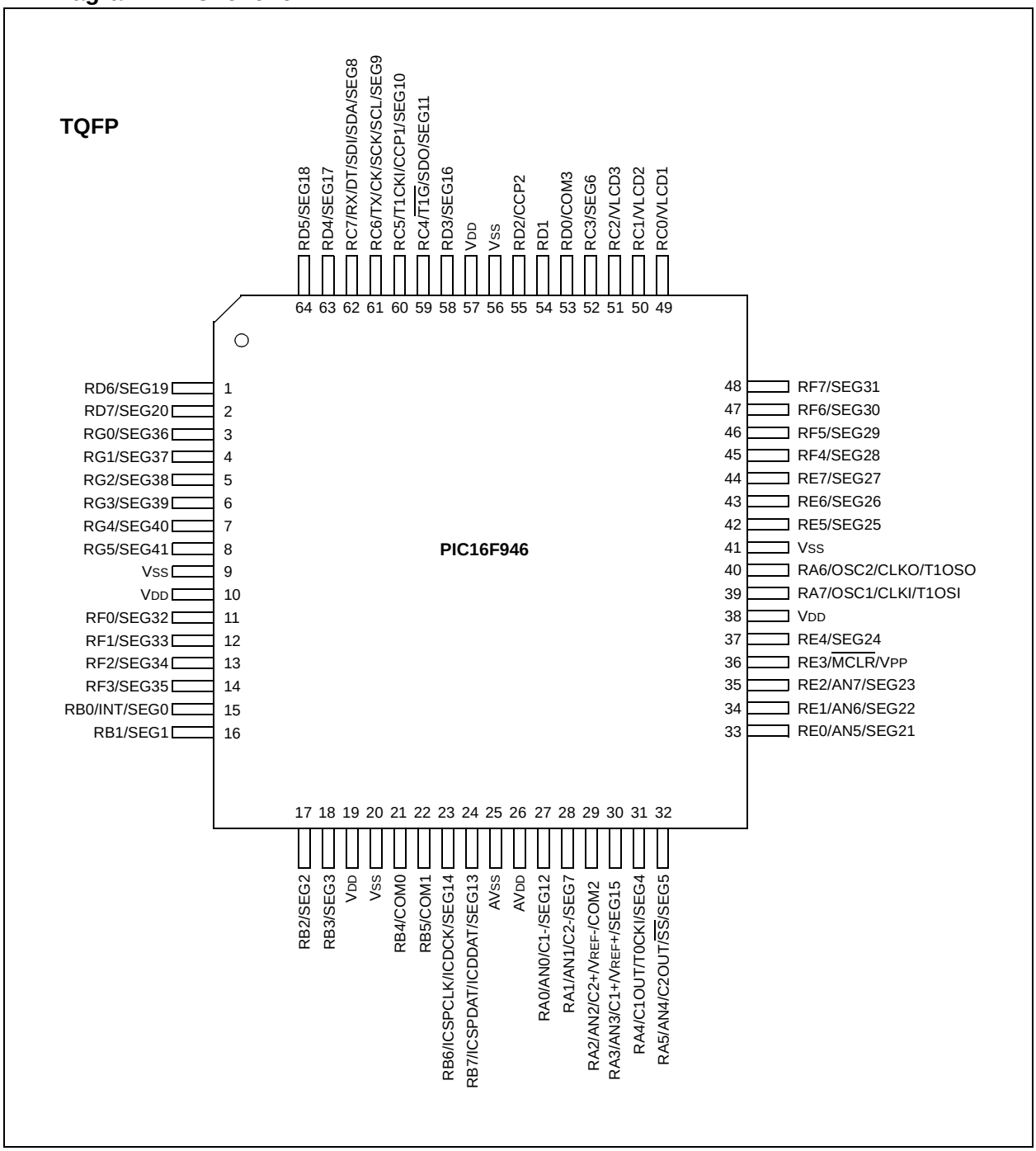
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	336 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f946-i-pt

Device	Program Memory	Data Memory		I/O	10-bit A/D (ch)	LCD (segment drivers)	CCP	Timers 8/16-bit
	Flash (words)	SRAM (bytes)	EEPROM (bytes)					
PIC16F946	8K	336	256	53	8	42	2	2/1

Pin Diagram – PIC16F946



2.5 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

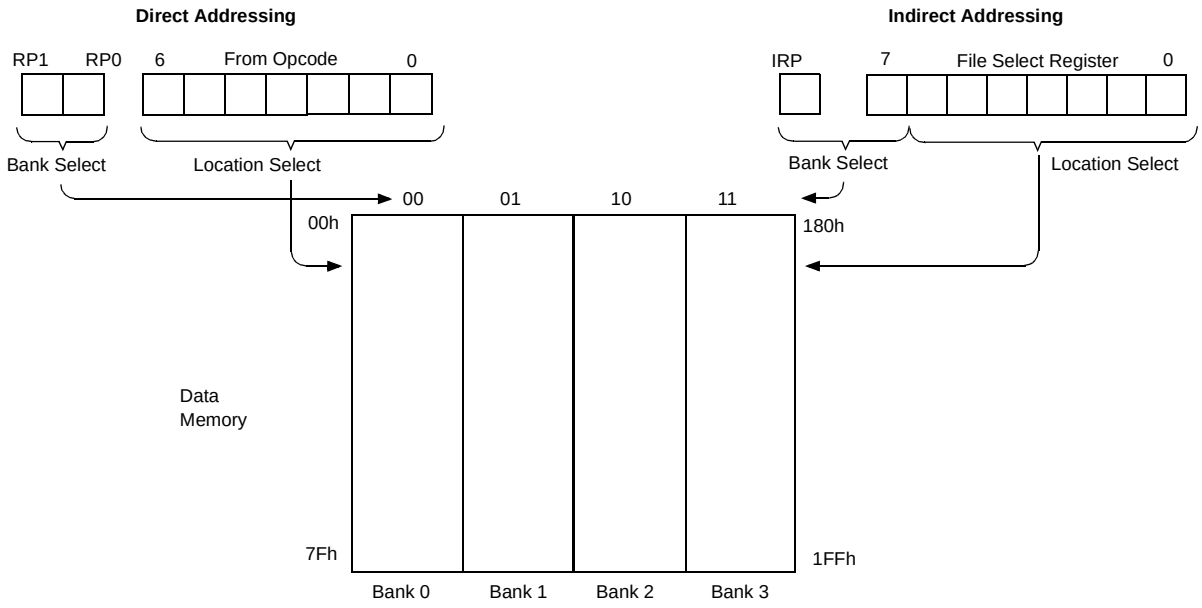
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 2-4.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 2-2.

EXAMPLE 2-2: INDIRECT ADDRESSING

```
    MOVLW   0x20    ;initialize pointer
    MOVWF   FSR     ;to RAM
NEXTCLRF    INDF    ;clear INDF register
    INCF    FSR     ;inc pointer
    BTFSS   FSR,4   ;all done?
    GOTO    NEXT    ;no clear next
CONTINUE            ;yes continue
```

FIGURE 2-4: DIRECT/INDIRECT ADDRESSING PIC16F946



Note: For memory map detail, see Figure 2-1.

3.0 I/O PORTS

This device includes four 8-bit port registers along with their corresponding TRIS registers and one four bit port:

- PORTA and TRISA
- PORTB and TRISB
- PORTC and TRISC
- PORTD and TRISD
- PORTE and TRISE
- PORTF and TRISF
- PORTG and TRISG

3.1 PORTA and TRISA Registers

PORTA is a 8-bit wide, bidirectional port. The corresponding data direction register is TRISA (Register 3-2). Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a High-impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin). Example 3-1 shows how to initialize PORTA.

Five of the pins of PORTA can be configured as analog inputs. These pins, RA5 and RA<3:0>, are configured as analog inputs on device power-up and must be reconfigured by the user to be used as I/O's. This is done by writing the appropriate values to the CMCON0 and ANSEL registers (see Example 3-1).

Reading the PORTA register (Register 3-1) reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the port data latch.

The TRISA register controls the direction of the PORTA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

Note 1:	The CMCON0 (9Ch) register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.
2:	Analog lines that carry LCD signals (i.e., SEGx, COMy, where x and y are segment and common identifiers) are shown as direct connections to the device pins. The signals are outputs from the LCD module and may be tri-stated, depending on the configuration of the LCD module.

EXAMPLE 3-1: INITIALIZING PORTA

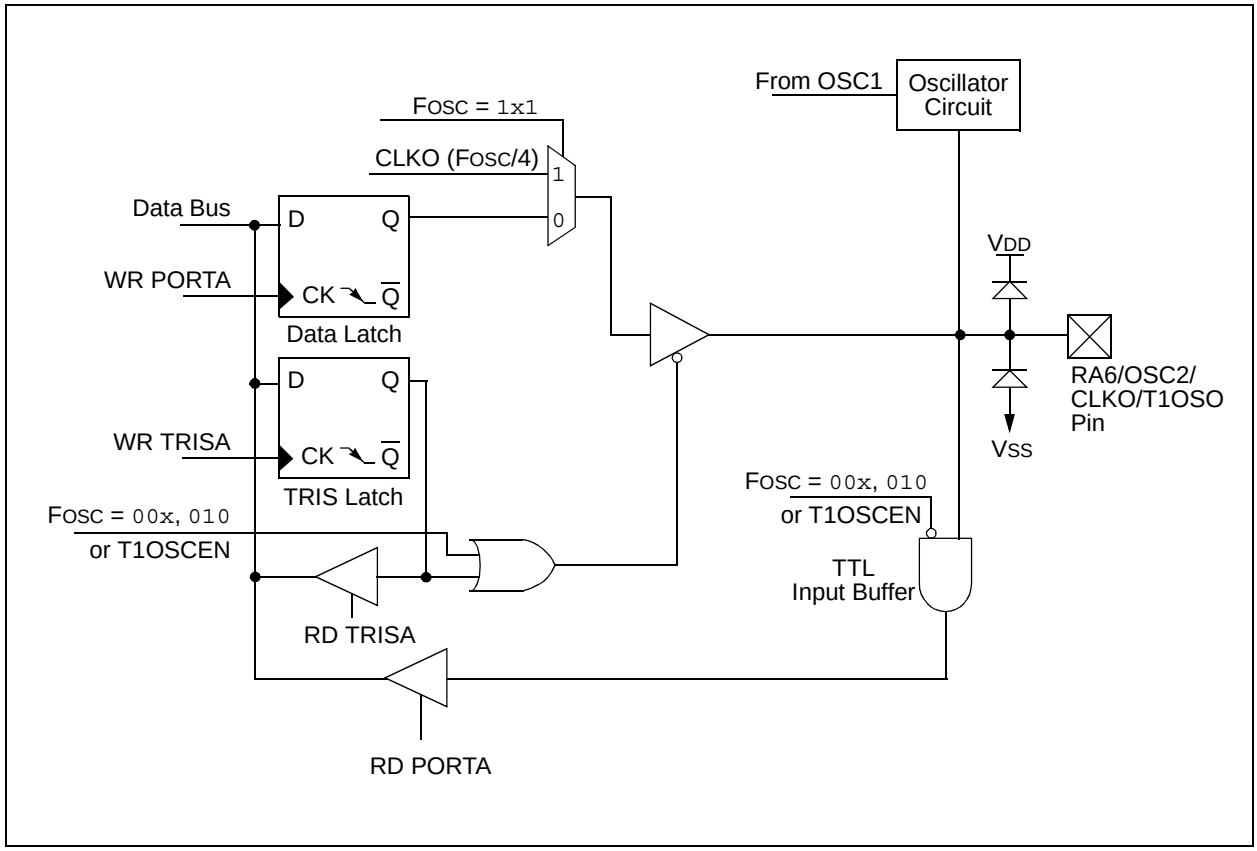
```
BCF     STATUS,RP0      ;Bank 0
BCF     STATUS,RP1      ;
CLRF    PORTA           ;Init PORTA
BSF     STATUS,RP0      ;Bank 1
BCF     STATUS,RP1      ;
MOVLW   07h             ;Set RA<2:0> to
MOVWF   CMCON0          ;digital I/O
CLF     ANSEL           ;Make all PORTA I/O
MOVLW   F0h             ;Set RA<7:4> as inputs
MOVWF   TRISA           ;and set RA<3:0>
                        ; as outputs
BCF     STATUS,RP0      ;Bank 0
BCF     STATUS,RP1      ;
```

3.1.1.7 RA6/OSC2/CLKO/T1OSO

Figure 3-7 shows the diagram for this pin. The RA6/OSC2/CLKO/T1OSO pin is configurable to function as one of the following:

- a general purpose I/O
- a crystal/resonator connection
- a clock output
- a TMR1 oscillator connection

FIGURE 3-7: BLOCK DIAGRAM OF RA6/OSC2/CLKO/T1OSO

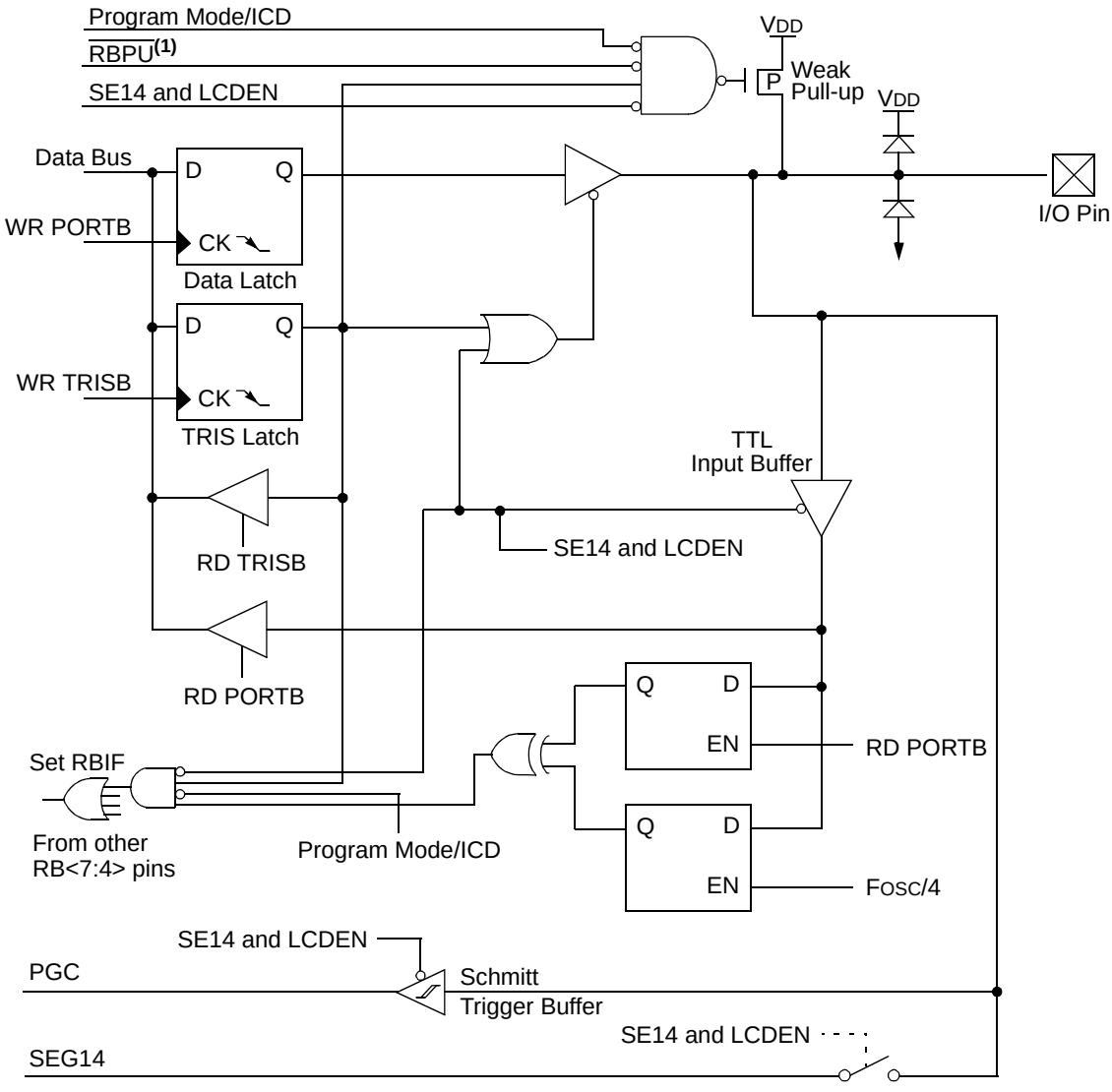


3.3.3.7 RB6/ICSPCLK/ICDCK/SEG14

Figure 3-12 shows the diagram for this pin. The RB6/ICSPCLK/ICDCK/SEG14 pin is configurable to function as one of the following:

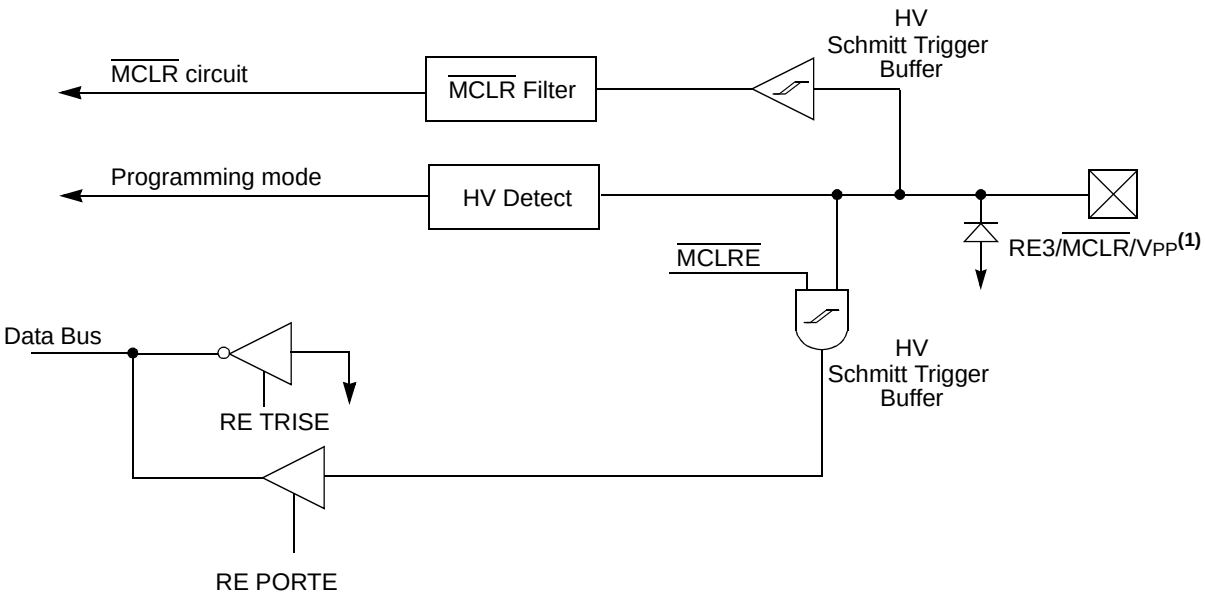
- a general purpose I/O
- an In-Circuit Serial Programming™ clock
- an ICD clock I/O
- an analog output for the LCD

FIGURE 3-12: BLOCK DIAGRAM OF RB6/ICSPCLK/ICDCK/SEG14



Note 1: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the $\overline{\text{RBPU}}$ bit.

FIGURE 3-27: BLOCK DIAGRAM OF RE3/$\overline{MCLR}$/VPP



Note 1: RE3 will read '0' when pin is $\overline{MCLR}$.

TABLE 3-5: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
09h	PORTE	RE7	R6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADFM	VCFG1	VCFG0	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	ADON	0000 0000	0000 0000
89h	TRISE	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3(2)	TRISE2	TRISE1	TRISE0	1111 1111	1111 1111
91h	ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
107h	LCDCON	LCDEN	SLPEN	WERR	VLCDEN	CS1	CS0	LMUX1	LMUX0	0001 0011	0001 0011
11Eh	LCDSE2(1)	SE23	SE22	SE21	SE20	SE19	SE18	SE17	SE16	0000 0000	uuuu uuuu
19Ch	LCDSE3(1)	SE31	SE30	SE29	SE28	SE27	SE26	SE25	SE24	0000 0000	uuuu uuuu

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTE.
Note 1: This register is only initialized by a POR or BOR and is unchanged by other Resets.
2: Bit is read-only; TRISE = 1 always.

4.4.3 LFINTOSC

The Low-Frequency Internal Oscillator (LFINTOSC) is an uncalibrated (approximate) 31 kHz internal clock source.

The output of the LFINTOSC connects to a postscaler and multiplexer (see Figure 4-1). 31 kHz can be selected via software using the IRCF bits (see **Section 4.4.4 "Frequency Select Bits (IRCF)"**). The LFINTOSC is also the frequency for the Power-up Timer (PWRT), Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The LFINTOSC is enabled by selecting 31 kHz (IRCF = 000) as the System Clock Source (SCS = 1), or when any of the following are enabled:

- Two-Speed Start-up (IESO = 1 and IRCF = 000)
- Power-up Timer (PWRT)
- Watchdog Timer (WDT)
- Fail-Safe Clock Monitor (FSCM)
- Selected as LCD module clock source

The LF Internal Oscillator (LTS) bit (OSCCON<1>) indicates whether the LFINTOSC is stable or not.

4.4.4 FREQUENCY SELECT BITS (IRCF)

The output of the 8 MHz HFINTOSC and 31 kHz LFINTOSC connect to a postscaler and multiplexer (see Figure 4-1). The Internal Oscillator Frequency select bits, IRCF<2:0> (OSCCON<6:4>), select the frequency output of the internal oscillators. One of eight frequencies can be selected via software:

- 8 MHz
- 4 MHz (Default after Reset)
- 2 MHz
- 1 MHz
- 500 kHz
- 250 kHz
- 125 kHz
- 31 kHz

Note:	Following any Reset, the IRCF bits are set to '110' and the frequency selection is set to 4 MHz. The user can modify the IRCF bits to select a different frequency.

4.4.5 HF AND LF INTOSC CLOCK SWITCH TIMING

When switching between the LFINTOSC and the HFINTOSC, the new oscillator may already be shut down to save power. If this is the case, there is a 10 µs delay after the IRCF bits are modified before the frequency selection takes place. The LTS/HTS bits will reflect the current active status of the LFINTOSC and the HFINTOSC oscillators. The timing of a frequency selection is as follows:

1. IRCF bits are modified.
2. If the new clock is shut down, a 10 µs clock start-up delay is started.
3. Clock switch circuitry waits for a falling edge of the current clock.
4. CLKO is held low and the clock switch circuitry waits for a rising edge in the new clock.
5. CLKO is now connected with the new clock. HTS/LTS bits are updated as required.
6. Clock switch is complete.

If the internal oscillator speed selected is between 8 MHz and 125 kHz, there is no start-up delay before the new frequency is selected. This is because the old and the new frequencies are derived from the HFINTOSC via the postscaler and multiplexer.

4.5 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS) bit.

4.5.1 SYSTEM CLOCK SELECT (SCS) BIT

The System Clock Select (SCS) bit (OSCCON<0>) selects the system clock source that is used for the CPU and peripherals.

- When SCS = 0, the system clock source is determined by configuration of the FOSC<2:0> bits in the Configuration Word register (CONFIG).
- When SCS = 1, the system clock source is chosen by the internal oscillator frequency selected by the IRCF bits. After a Reset, SCS is always cleared.

Note:	Any automatic clock switch, which may occur from Two-Speed Start-up or Fail-Safe Clock Monitor, does not update the SCS bit. The user can monitor the OSTS (OSCCON<3>) to determine the current system clock source.

REGISTER 8-2: CMCON1 – COMPARATOR CONFIGURATION REGISTER (ADDRESS: 97h)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0
—	—	—	—	—	—	T1GSS	C2SYNC
bit 7							bit 0

bit 7-2: **Unimplemented**: Read as '0'

bit 1 **T1GSS:** Timer1 Gate Source Select bit

1 = Timer1 gate source is $\overline{T1G}$ pin (RC4 must be configured as digital input)
0 = Timer1 gate source is Comparator 2 Output

bit 0 **C2SYNC:** Comparator 2 Synchronize bit

1 = C2 output synchronized with falling edge of Timer1 clock
0 = C2 output not synchronized with Timer1 clock

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

8.4 Comparator Outputs

The comparator outputs are read through the CMCON0 register. These bits are read-only. The comparator outputs may also be directly output to the RA4 and RA5 I/O pins. When enabled, multiplexers in the output path of the RA4 and RA5 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 8-4 and Figure 8-5 show the output block diagram for Comparator 1 and 2.

The TRIS bits will still function as an output enable/disable for the RA4 and RA5 pins while in this mode.

The polarity of the comparator outputs can be changed using the C1INV and C2INV bits (CMCON0<5:4>).

Timer1 gate source can be configured to use the $\overline{T1G}$ pin or Comparator 2 output as selected by the T1GSS bit (CMCON1<1>). This feature can be used to time the duration or interval of analog events. The output of Comparator 2 can also be synchronized with Timer1 by setting the C2SYNC bit (CMCON1<0>). When enabled, the output of Comparator 2 is latched on the falling edge of Timer1 clock source. If a prescaler is used with Timer1, Comparator 2 is latched after the prescaler. To prevent a race condition, the Comparator 2 output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See (Figure 8-5), Comparator 2 Block Diagram and (Figure 5-1), Timer1 Block Diagram for more information.

It is recommended to synchronize Comparator 2 with Timer1 by setting the C2SYNC bit when Comparator 2 is used as the Timer1 gate source. This ensures Timer1 does not miss an increment if Comparator 2 changes during an increment.

8.5 Comparator Interrupts

The comparator interrupt flags are set whenever there is a change in the output value of its respective comparator. Software will need to maintain information about the status of the output bits, as read from CMCON0<7:6>, to determine the actual change that has occurred. The CxIF bits, PIR2<6:5>, are the Comparator Interrupt flags. This bit must be reset in software by clearing it to '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CxIE bits (PIE2<6:5>) and the PEIE bit (INTCON<6>) must be set to enable the interrupts. In addition, the GIE bit must also be set. If any of these bits are cleared, the interrupt is not enabled, though the CxIF bits will still be set if an interrupt condition occurs.

The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

a) Any read or write of CMCON0. This will end the mismatch condition.
b) Clear flag bit CxIF

A mismatch condition will continue to set flag bit CxIF. Reading CMCON0 will end the mismatch condition and allow flag bits CxIF to be cleared.

Note: If a change in the CMCON0 register (CxOUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CxIF (PIR2<6:5>) interrupt flag may not get set.

9.1 LCD Clock Source Selection

The LCD driver module has 3 possible clock sources:

- FOSC/8192
- T1OSC/32
- LFINTOSC/32

The first clock source is the system clock divided by 8192 (FOSC/8192). This divider ratio is chosen to provide about 1 kHz output when the system clock is 8 MHz. The divider is not programmable. Instead, the LCD prescaler bits, LCDPS<3:0>, are used to set the LCD frame clock rate.

The second clock source is the T1OSC/32. This also gives about 1 kHz when a 32.768 kHz crystal is used with the Timer1 oscillator. To use the Timer1 oscillator as a clock source, the T1OSCEN (T1CON<3>) bit should be set.

The third clock source is the 31 kHz LFINTOSC/32, which provides approximately 1 kHz output.

The second and third clock sources may be used to continue running the LCD while the processor is in Sleep.

Using the bits, CS<1:0> (LCDCON<3:2>), any of these clock sources can be selected.

9.1.1 LCD PRESCALER

A 16-bit counter is available as a prescaler for the LCD clock. The prescaler is not directly readable or writable; its value is set by the LP<3:0> bits (LCDPS<3:0>), which determine the prescaler assignment and prescale ratio.

The prescale values from 1:1 through 1:16.

9.2 LCD Bias Types

The LCD driver module can be configured into three bias types:

- Static Bias (2 voltage levels: VSS and VDD)
- 1/2 Bias (3 voltage levels: VSS, 1/2 VDD and VDD)
- 1/3 Bias (4 voltage levels: VSS, 1/3 VDD, 2/3 VDD and VDD)

This module uses an external resistor ladder to generate the LCD bias voltages.

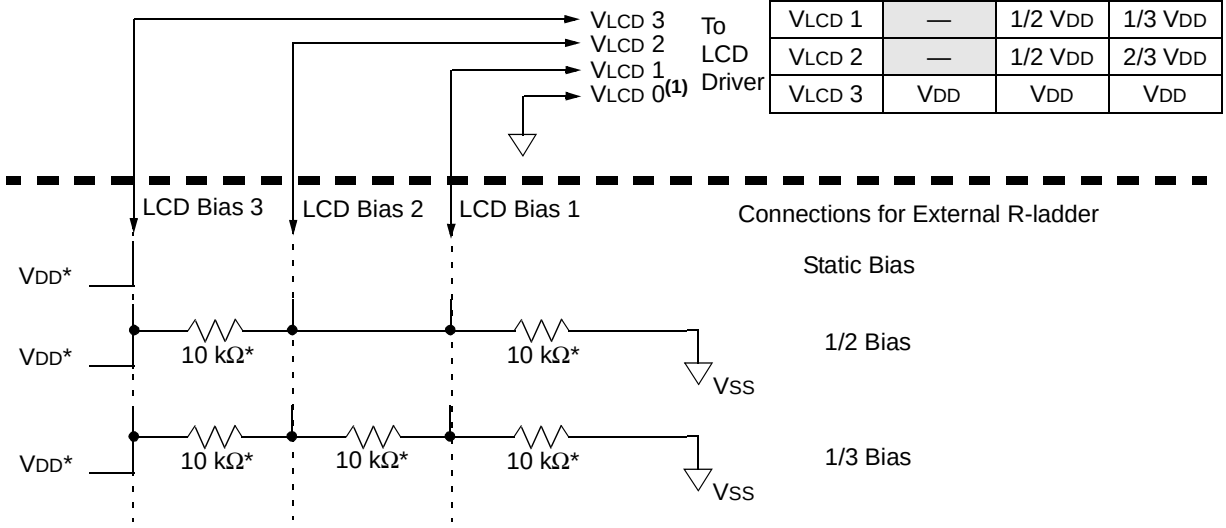
The external resistor ladder should be connected to the Bias 1 pin, Bias 2 pin, Bias 3 pin and VSS. The Bias 3 pin should also be connected to VDD.

Figure 9-2 shows the proper way to connect the resistor ladder to the Bias pins.

Note:	VLCD pins used to supply LCD bias voltage are enabled on power-up (POR) and must be disabled by the user by clearing LCDCON<4>, the VLCDEN bit, (see Register 9-1).

FIGURE 9-2: LCD BIAS RESISTOR LADDER CONNECTION DIAGRAM

	Static Bias	1/2 Bias	1/3 Bias
VLCD 0	VSS	VSS	VSS
VLCD 1	—	1/2 VDD	1/3 VDD
VLCD 2	—	1/2 VDD	2/3 VDD
VLCD 3	VDD	VDD	VDD



* These values are provided for design guidance only and should be optimized for the application by the designer.

Note 1: Internal connection.

9.9 Operation During Sleep

The LCD module can operate during Sleep. The selection is controlled by bit SLPEN (LCDCON<6>). Setting the SLPEN bit allows the LCD module to go to Sleep. Clearing the SLPEN bit allows the module to continue to operate during Sleep.

If a SLEEP instruction is executed and SLPEN = 1, the LCD module will cease all functions and go into a very low-current Consumption mode. The module will stop operation immediately and drive the minimum LCD voltage on both segment and common lines. Figure 9-18 shows this operation.

To ensure that no DC component is introduced on the panel, the SLEEP instruction should be executed immediately after a LCD frame boundary. The LCD interrupt can be used to determine the frame boundary. See **Section 9.8 "LCD Interrupts"** for the formulas to calculate the delay.

If a SLEEP instruction is executed and SLPEN = 0, the module will continue to display the current contents of the LCDDATA registers. To allow the module to continue operation while in Sleep, the clock source must be either the LFINTOSC or T1OSC external oscillator. While in Sleep, the LCD data cannot be changed. The LCD module current consumption will not decrease in this mode; however, the overall consumption of the device will be lower due to shut down of the core and other peripheral functions.

Table 9-4 shows the status of the LCD module during a Sleep while using each of the three available clock sources:

TABLE 9-4: LCD MODULE STATUS DURING SLEEP

Clock Source	SLPEN	Operation During Sleep?
T1OSC	0	Yes
	1	No
LFINTOSC	0	Yes
	1	No
FOSC/4	0	No
	1	No

Note:	The LFINTOSC or external T1OSC oscillator must be used to operate the LCD module during Sleep.

9.10 Configuring the LCD Module

The following is the sequence of steps to configure the LCD module.

1. Select the frame clock prescale using bits LP<3:0> (LCDPS<3:0>).
2. Configure the appropriate pins to function as segment drivers using the LCDSEn registers.
3. Configure the LCD module for the following using the LCDCON register:

   -Multiplex and Bias mode, bits LMUX<1:0>

   -Timing source, bits CS<1:0>

   -Sleep mode, bit SLPEN
4. Write initial values to pixel data registers, LCDDATA0 through LCDDATA11.
5. Clear LCD Interrupt Flag, LCDIF (PIR2<4>) and if desired, enable the interrupt by setting bit LCDIE (PIE2<4>).
6. Enable bias voltage pins (VLCD<3:1>) by setting VLCDEN (LCDCON<4>).
7. Enable the LCD module by setting bit LCDEN (LCDCON<7>).

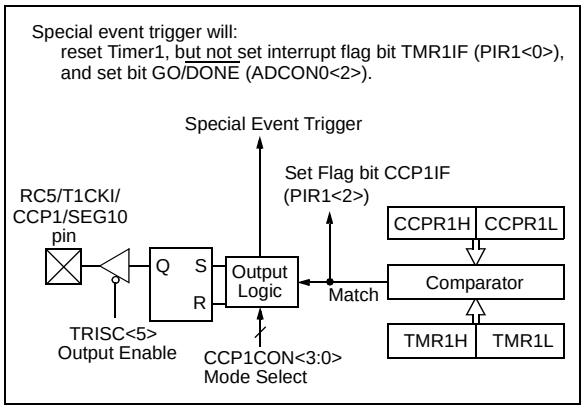
15.2 Compare Mode

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the RC5/T1CKI/CCP1/SEG10 pin is:

- Driven high
- Driven low
- Remains unchanged

The action on the pin is based on the value of control bits CCP1M<3:0> (CCP1CON<3:0>). At the same time, interrupt flag bit CCP1IF is set.

FIGURE 15-4: COMPARE MODE OPERATION BLOCK DIAGRAM



15.2.1 CCP PIN CONFIGURATION

The user must configure the RC5/T1CKI/CCP1/SEG10 pin as an output by clearing the TRISC<5> bit.

Note:	Clearing the CCP1CON register will force the RC5/T1CKI/CCP1/SEG10 compare output latch to the default low level. This is not the PORTC I/O data latch.

15.2.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode, or Synchronized Counter mode, if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

15.2.3 SOFTWARE INTERRUPT MODE

When Generate Software Interrupt mode is chosen, the RC5/T1CKI/CCP1/SEG10 pin is not affected. The CCPIF bit is set, causing a CCP interrupt (if enabled).

15.2.4 SPECIAL EVENT TRIGGER

In this mode, an internal hardware trigger is generated, which may be used to initiate an action.

The special event trigger output of CCP1 resets the TMR1 register pair. This allows the CCPR1 register to effectively be a 16-bit programmable period register for Timer1.

The special event trigger output of CCP2 resets the TMR1 register pair and starts an A/D conversion (if the A/D module is enabled).

Note:	The special event trigger from the CCP1and CCP2 modules will not set interrupt flag bit TMR1IF (PIR1<0>).

15.3 PWM Mode (PWM)

In Pulse-Width Modulation mode, the CCPx pin produces up to a 10-bit resolution PWM output. Since the RC5/T1CKI/CCP1/SEG10 pin is multiplexed with the PORTC data latch, the TRISC<5> bit must be cleared to make the RC5/T1CKI/CCP1/SEG10 pin an output.

Note:	Clearing the CCP1CON register will force the CCP1 PWM output latch to the default low level. This is not the PORTC I/O data latch.

Figure 15-5 shows a simplified block diagram of the CCP module in PWM mode.

For a step-by-step procedure on how to set up the CCP module for PWM operation, see **Section 15.3.3 "Setup for PWM Operation"**.

TABLE 16-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	Status Register	PCON Register
Power-on Reset	000h	0001 1xxx	--01 --0x
$\overline{\text{MCLR}}$ Reset during normal operation	000h	000u uuuu	--0u --uu
$\overline{\text{MCLR}}$ Reset during Sleep	000h	0001 0uuu	--0u --uu
WDT Reset	000h	0000 uuuu	--0u --uu
WDT Wake-up	PC + 1	uuu0 0uuu	--uu --uu
Brown-out Reset	000h	0001 1uuu	--01 --10
Interrupt Wake-up from Sleep	PC + 1(1)	uuu1 0uuu	--uu --uu

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and Global Interrupt Enable bit, GIE, is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

16.6 Watchdog Timer (WDT)

For PIC16F946, the WDT has been modified from previous PIC16F devices. The new WDT is code and functionally compatible with previous PIC16F WDT modules and adds a 16-bit prescaler to the WDT. This allows the user to have a scaled value for the WDT and TMR0 at the same time. In addition, the WDT time-out value can be extended to 268 seconds. WDT is cleared under certain conditions described in Table 16-7.

16.6.1 WDT OSCILLATOR

The WDT derives its time base from the 31 kHz LFINTOSC. The LTS bit does not reflect that the LFINTOSC is enabled.

The value of WDTCON is '---0 1000' on all Resets. This gives a nominal time base of 16 ms, which is compatible with the time base generated with previous PIC16F microcontroller versions.

Note:	When the Oscillator Start-up Timer (OST) is invoked, the WDT is held in Reset, because the WDT Ripple Counter is used by the OST to perform the oscillator delay count. When the OST count has expired, the WDT will begin counting (if enabled).

A new prescaler has been added to the path between the INTOSC and the multiplexers used to select the path for the WDT. This prescaler is 16 bits and can be programmed to divide the INTOSC by 32 to 65536, giving the WDT a nominal range of 1 ms to 268s.

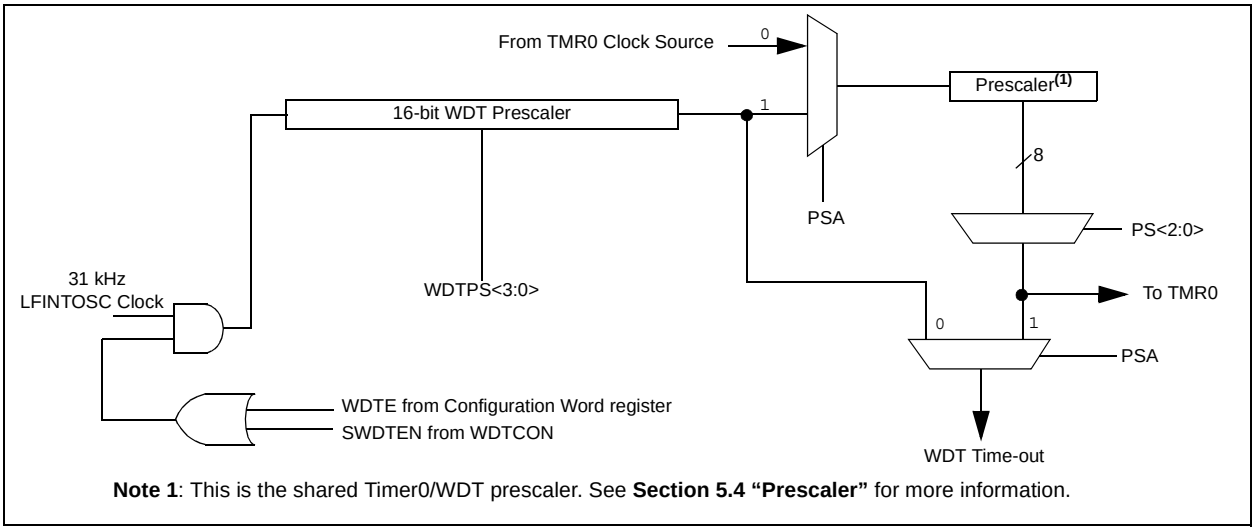
16.6.2 WDT CONTROL

The WDTE bit is located in the Configuration Word register. When set, the WDT runs continuously.

When the WDTE bit in the Configuration Word register is set, the SWDTEN bit (WDTCON<0>) has no effect. If WDTE is clear, then the SWDTEN bit can be used to enable and disable the WDT. Setting the bit will enable it and clearing the bit will disable it.

The PSA and PS<2:0> bits (OPTION_REG) have the same function as in previous versions of the PIC16F family of microcontrollers. See **Section 5.0 "Timer0 Module"** for more information.

FIGURE 16-9: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: This is the shared Timer0/WDT prescaler. See **Section 5.4 "Prescaler"** for more information.

TABLE 16-7: WDT STATUS

Conditions	WDT
WDTE = 0	Cleared
CLRWDT Command	
Oscillator Fail Detected	
Exit Sleep + System Clock = T1OSC, EXTRC, INTOSC, EXTCLK	
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST

16.8 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out using ICSP for verification purposes.

Note:	The entire data EEPROM and Flash program memory will be erased when the code protection is turned off. See the "*PIC16F91X/946 Memory Programming Specification*" (DS41244) for more information.

16.9 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during Program/Verify mode. Only the Least Significant 7 bits of the ID locations are used.

16.10 In-Circuit Serial Programming

The PIC16F946 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data and three other lines for:

- power
- ground
- programming voltage

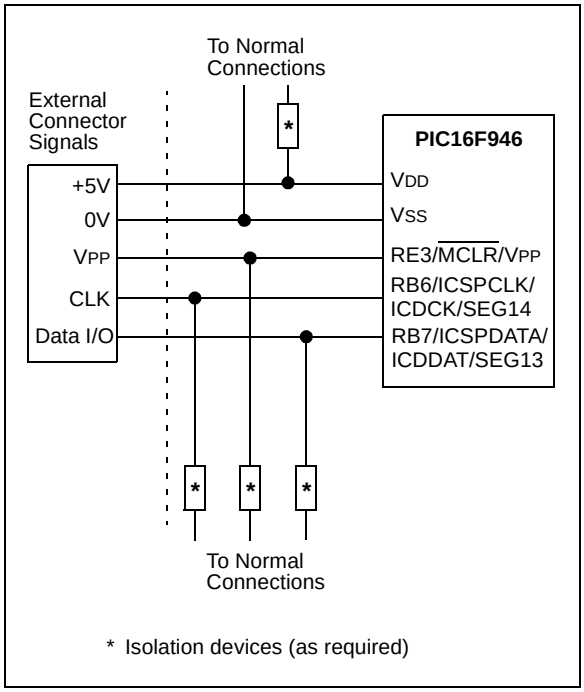
This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a Program/Verify mode by holding the RB7/ICSPDAT/ICDDAT/SEG13 and RB6/ICSPCLK/ICDCK/SEG14 pins low, while raising the $\overline{MCLR}$ (V_{PP}) pin from V_{IL} to V_{IHH}. See "*PIC16F91X/946 Memory Programming Specification*" (DS41244) for more information. RB7/ICSPDAT/ICDDAT/SEG13 becomes the programming data and RB6/ICSPCLK/ICDCK/SEG14 becomes the programming clock. Both RB7/ICSPDAT/ICDDAT/SEG13 and RB6/ICSPCLK/ICDCK/SEG14 are Schmitt Trigger inputs in this mode.

After Reset, to place the device into Program/Verify mode, the Program Counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14 bits of program data are then supplied to or from the device, depending on whether the command was a load or a read. For complete details of serial programming, please refer to the "*PIC16F91X/946 Memory Programming Specification*" (DS41244).

A typical In-Circuit Serial Programming connection is shown in Figure 16-11.

FIGURE 16-11: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



18.9 MPLAB ICE 2000 High-Performance Universal In-Circuit Emulator

The MPLAB ICE 2000 universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro microcontrollers. Software control of the MPLAB ICE 2000 in-circuit emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PICmicro microcontrollers.

The MPLAB ICE 2000 in-circuit emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft® Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

18.10 MPLAB ICE 4000 High-Performance Universal In-Circuit Emulator

The MPLAB ICE 4000 universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for high-end PICmicro microcontrollers. Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICD 4000 is a premium emulator system, providing the features of MPLAB ICE 2000, but with increased emulation memory and high-speed performance for dsPIC30F and PIC18XXXX devices. Its advanced emulator features include complex triggering and timing, up to 2 Mb of emulation memory and the ability to view variables in real-time.

The MPLAB ICE 4000 in-circuit emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

18.11 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low-cost, run-time development tool, connecting to the host PC via an RS-232 or high-speed USB interface. This tool is based on the Flash PICmicro MCUs and can be used to develop for these and other PICmicro microcontrollers. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the Flash devices. This feature, along with Microchip's In-Circuit Serial Programming™ (ICSP™) protocol, offers cost effective in-circuit Flash debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single-stepping and watching variables, CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real-time. MPLAB ICD 2 also serves as a development programmer for selected PICmicro devices.

18.12 PRO MATE II Universal Device Programmer

The PRO MATE II is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features an LCD display for instructions and error messages and a modular detachable socket assembly to support various package types. In Stand-Alone mode, the PRO MATE II device programmer can read, verify and program PICmicro devices without a PC connection. It can also set code protection in this mode.

18.13 MPLAB PM3 Device Programmer

The MPLAB PM3 is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 device programmer can read, verify and program PICmicro devices without a PC connection. It can also set code protection in this mode. MPLAB PM3 connects to the host PC via an RS-232 or USB cable. MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an SD/MMC card for file storage and secure data applications.

TABLE 19-2: PRECISION INTERNAL OSCILLATOR PARAMETERS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C								
Param No.	**Sym**	**Characteristic**	**Freq. Tolerance**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
F10	FOSC	Internal Calibrated INTOSC Frequency(1)	±1%	—	8.00	TBD	MHz	VDD and Temperature TBD
			±2%	—	8.00	TBD	MHz	2.5V ≤ VDD ≤ 5.5V 0°C ≤ TA ≤ +85°C
			±5%	—	8.00	TBD	MHz	2.0V ≤ VDD ≤ 5.5V -40°C ≤ TA ≤ +85°C (Ind.) -40°C ≤ TA ≤ +125°C (Ext.)
F14	TIOSC ST	Oscillator Wake-up from Sleep Start-up Time*	—	—	TBD	TBD	µs	VDD = 2.0V, -40°C to +85°C
			—	—	TBD	TBD	µs	VDD = 3.0V, -40°C to +85°C
			—	—	TBD	TBD	µs	VDD = 5.0V, -40°C to +85°C

Legend: TBD = To Be Determined

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 uF and 0.01 uF values in parallel are recommended.

TABLE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET REQUIREMENTS

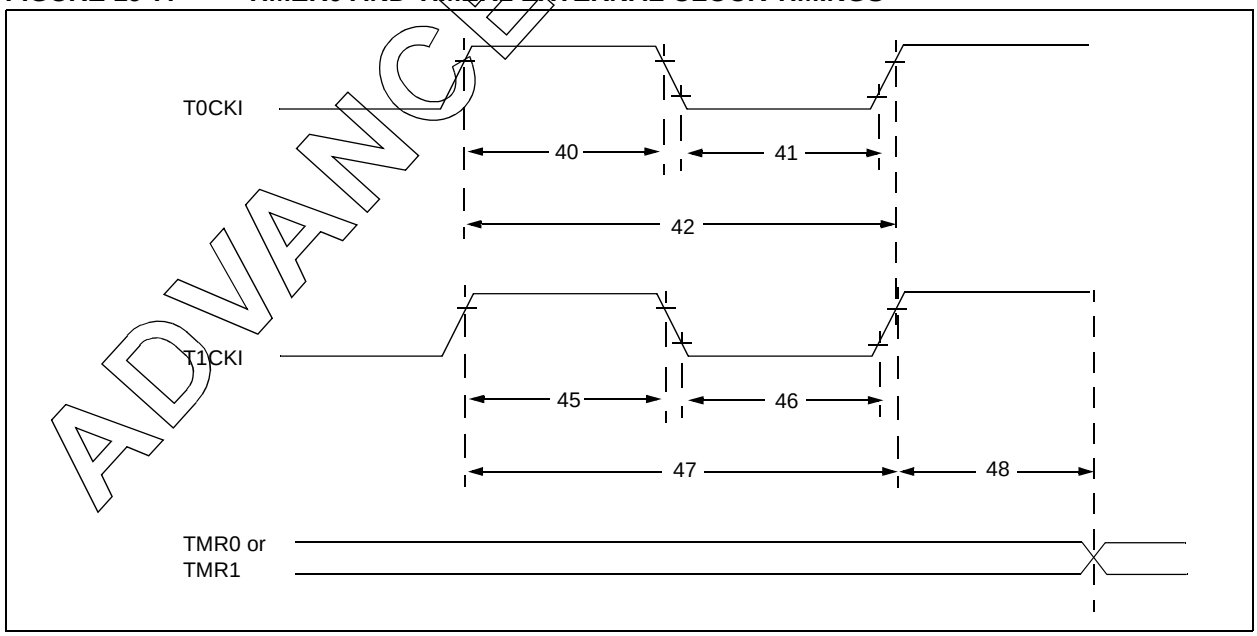
Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
30	TMCL	$\overline{MCLR}$ Pulse Width (low)	2 11	— 18	— 24	µs ms	VDD = 5V, -40°C to +85°C Extended temperature
31	TWDT	Watchdog Timer Time-out Period (No Prescaler)	10 10	17 17	25 30	ms ms	VDD = 5V, -40°C to +85°C Extended temperature
32	TOST	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = OSC1 period
33*	TPWRT	Power-up Timer Period	28* TBD	64 TBD	132* TBD	ms ms	VDD = 5V, -40°C to +85°C Extended Temperature
34	TIOZ	I/O High-impedance from $\overline{MCLR}$ Low or Watchdog Timer Reset	—	—	2.0	µs	
	BVDD	Brown-out Reset Voltage	2.025	—	2.175	V	
35	TBOR	Brown-out Reset Pulse Width	100*	—	—	µs	VDD ≤ BVDD (D005)

Legend: TBD = To Be Determined

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 19-7: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS



20.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

Graphs are not available at this time.

APPENDIX C: CONVERSION CONSIDERATIONS

Considerations for converting from previous versions of devices to the ones listed in this data sheet are listed in Table C-1.

TABLE C-1: CONVERSION CONSIDERATIONS

Characteristic	PIC16F946	PIC16F926	PIC18F6490
Pins	64	64	64
Timers	3	3	4
Interrupts	20	9	22
Communication	USART, SSP (SPI™, I^2C™ Slave)	SSP (SPI, I^2C Master/Slave)	USART, SSP (SPI, I^2C Master/Slave)
Frequency	20 MHz	20 MHz	20 MHz
Voltage	2.0V-5.5V	2.5V-5.5V	2.0V-5.5V
A/D	10-bit, 7 conversion clock selects	10-bit, 4 conversion clock selects	10-bit, 8 conversion clock selects
CCP	2	1	2
Comparator	2	—	2
Comparator Voltage Reference	Yes	—	Yes
Program Memory	8K Flash	8K OTP	8K Flash
RAM	332 bytes	336 bytes	768 bytes
EEPROM Data	256 bytes	—	—
Code Protection	On/Off	Segmented, starting at end of program memory	On/Off
Program Memory Write Protection	—	—	—
LCD Module	42 segment drivers, 4 commons	32 segment drivers, 4 commons	32 segment drivers, 4 commons
Other	In-Circuit Debugger	—	In-Circuit Debugger

