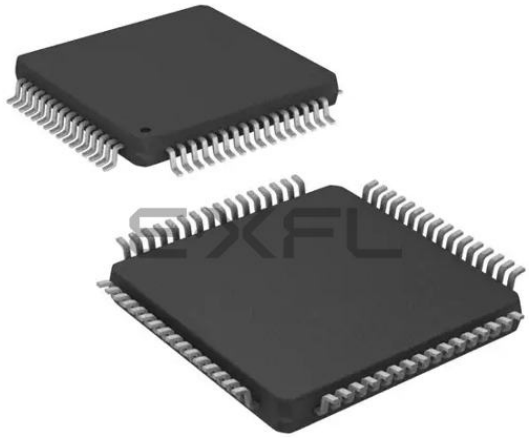

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	336 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f946t-i-pt

TABLE 1-1: PIC16F946 PINOUT DESCRIPTIONS (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC7/RX/DT/SDI/SDA/SEG8	RC7	ST	CMOS	General purpose I/O.
	RX	ST	—	USART asynchronous serial receive.
	DT	ST	CMOS	USART synchronous serial data.
	SDI	ST	CMOS	SPI™ data input.
	SDA	ST	CMOS	I^2C™ data.
	SEG8	—	AN	LCD analog output.
RD0/COM3	RD0	ST	CMOS	General purpose I/O.
	COM3	—	AN	LCD analog output.
RD1	RD1	ST	CMOS	General purpose I/O.
RD2/CCP2	RD2	ST	CMOS	General purpose I/O.
	CCP2	ST	CMOS	Capture 2 input/Compare 2 output/PWM 2 output.
RD3/SEG16	RD3	ST	CMOS	General purpose I/O.
	SEG16	—	AN	LCD analog output.
RD4/SEG17	RD4	ST	CMOS	General purpose I/O.
	SEG17	—	AN	LCD analog output.
RD5/SEG18	RD5	ST	CMOS	General purpose I/O.
	SEG18	—	AN	LCD analog output.
RD6/SEG19	RD6	ST	CMOS	General purpose I/O.
	SEG19	—	AN	LCD analog output.
RD7/SEG20	RD7	ST	CMOS	General purpose I/O.
	SEG20	—	AN	LCD analog output.
RE0/AN5/SEG21	RE0	ST	CMOS	General purpose I/O.
	AN5	AN	—	Analog input Channel 5.
	SEG21	—	AN	LCD analog output.
RE1/AN6/SEG22	RE1	ST	CMOS	General purpose I/O.
	AN6	AN	—	Analog input Channel 6.
	SEG22	—	AN	LCD analog output.
RE2/AN7/SEG23	RE2	ST	CMOS	General purpose I/O.
	AN7	AN	—	Analog input Channel 7.
	SEG23	—	AN	LCD analog output.
RE3/$\overline{MCLR}$/V_{PP}	RE3	ST	—	Digital input only.
	$\overline{MCLR}$	ST	—	Master Clear with internal pull-up.
	V_{PP}	HV	—	Programming voltage.
RE4/SEG24	RE4	ST	CMOS	General purpose I/O.
	SEG24	—	AN	LCD analog output.
RE5/SEG25	RE5	ST	CMOS	General purpose I/O.
	SEG25	—	AN	LCD analog output.
RE6/SEG26	RE6	ST	CMOS	General purpose I/O.
	SEG26	—	AN	LCD analog output.
RE7/SEG27	RE7	ST	CMOS	General purpose I/O.
	SEG27	—	AN	LCD analog output.
RF0/SEG32	RF0	ST	CMOS	General purpose I/O.
	SEG32	—	AN	LCD analog output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output D = Direct
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels
HV = High Voltage XTAL = Crystal

3.4 PORTC and TRISC Registers

PORTC is an 8-bit bidirectional port. PORTC is multiplexed with several peripheral functions. PORTC pins have Schmitt Trigger input buffers.

All PORTC pins have latch bits (PORTC register). They, when written, will modify the contents of the PORTC latch; thus, modifying the value driven out on a pin if the corresponding TRISC bit is configured for output.

Note:	Analog lines that carry LCD signals (i.e., SEGx, VLCDy, where x and y are segment and LCD bias voltage identifiers) are shown as direct connections to the device pins. The signals are outputs from the LCD module and may be tri-stated, depending on the configuration of the LCD module.

EXAMPLE 3-3: INITIALIZING PORTC

```
BCF     STATUS,RP0 ;Bank 0
BCF     STATUS,RP1 ;
CLRF    PORTC      ;Init PORTC
BSF     STATUS,RP0 ;Bank 1
BCF     STATUS,RP1 ;
MOVLW   FFh        ;Set RC<7:0> as inputs
MOVWF   TRISC      ;
BCF     STATUS,RP0 ;Bank 2
BSF     STATUS,RP1 ;
CLRF    LCDCON     ;Disable VLCD<3:1>
                   ;inputs on RC<2:0>
BCF     STATUS,RP0 ;Bank 0
BCF     STATUS,RP1 ;
```

REGISTER 3-7: PORTC – PORTC REGISTER (ADDRESS: 07h)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
bit 7							bit 0

bit 7-0 **RC<7:0>**: PORTC I/O Pin bits
1 = Port pin is >V_{IH}
0 = Port pin is <V_{IL}

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 3-8: TRISC – PORTC TRI-STATE REGISTER (ADDRESS: 87h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
bit 7							bit 0

bit 7-0 **TRISC<7:0>:** PORTC Tri-State Control bits
1 = PORTC pin configured as an input (tri-stated)
0 = PORTC pin configured as an output

Note: TRISC<7:6> always reads '1' in XT, HS and LP OSC modes.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

FIGURE 3-15: BLOCK DIAGRAM OF RC1/VLCD2

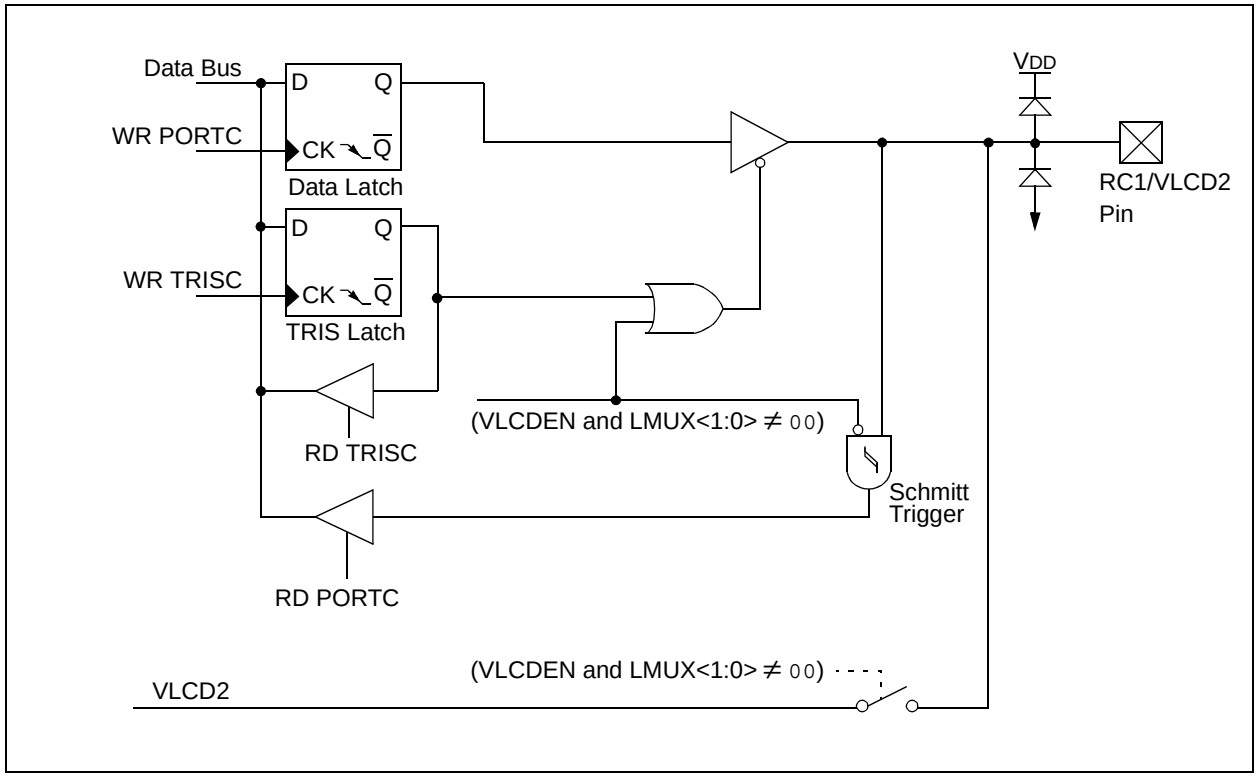
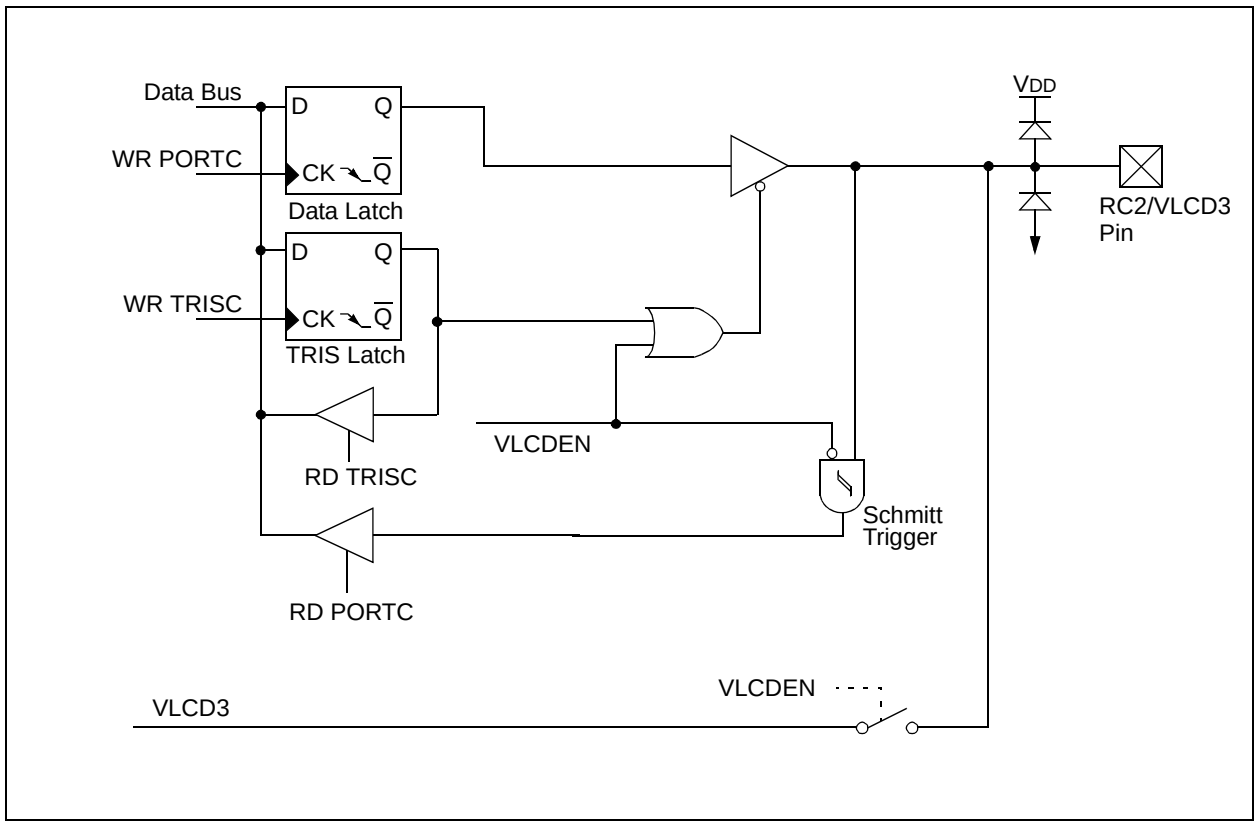


FIGURE 3-16: BLOCK DIAGRAM OF RC2/VLCD3



4.2 Clock Source Modes

Clock source modes can be classified as external or internal.

- External clock modes rely on external circuitry for the clock source. Examples are oscillator modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes), and Resistor-Capacitor (RC mode) circuits.
- Internal clock sources are contained internally within the PIC16F946. The PIC16F946 has two internal oscillators: the 8 MHz High-Frequency Internal Oscillator (HFINTOSC) and 31 kHz Low-Frequency Internal Oscillator (LFINTOSC).

The system clock can be selected between external or internal clock sources via the System Clock Selection (SCS) bit (see **Section 4.5 "Clock Switching"**).

4.3 External Clock Modes

4.3.1 OSCILLATOR START-UP TIMER (OST)

If the PIC16F946 is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from the OSC1 pin, following a Power-on Reset (POR), and the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the PIC16F946. When switching between clock sources a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 4-1.

4.3.1.1 Special Case

An exception to this is when the device is put to Sleep while the following conditions are true:

- LP is the selected primary oscillator mode.
- T1OSCEN = 1 (Timer1 oscillator is enabled).
- SCS = 0 (oscillator mode is defined by FOSC<2:0>).
- OSTS = 1 (device is running from primary system clock).

For this case, the OST is not necessary after a wake-up from Sleep, since Timer1 continues to run during Sleep and uses the same LP oscillator circuit as its clock source. For these devices, this case is typically seen when the LCD module is running during Sleep.

In applications where the OSCTUNE register is used to shift the FINTOSC frequency, the application should not expect the FINTOSC frequency to stabilize immediately. In this case, the frequency may shift gradually toward the new value. The time for this frequency shift is less than eight cycles of the base frequency.

Note:	When the OST is invoked, the WDOG is held in **Reset,** because the WDOG ripple counter is used by the OST to perform the oscillator delay count. When the OST count has expired, the WDOG will begin counting (if enabled).

Table 4-1 shows examples where the oscillator delay is invoked.

In order to minimize latency between external oscillator start-up and code execution, the Two-Speed Clock Start-up mode can be selected (see **Section 4.6 "Two-Speed Clock Start-up Mode"**).

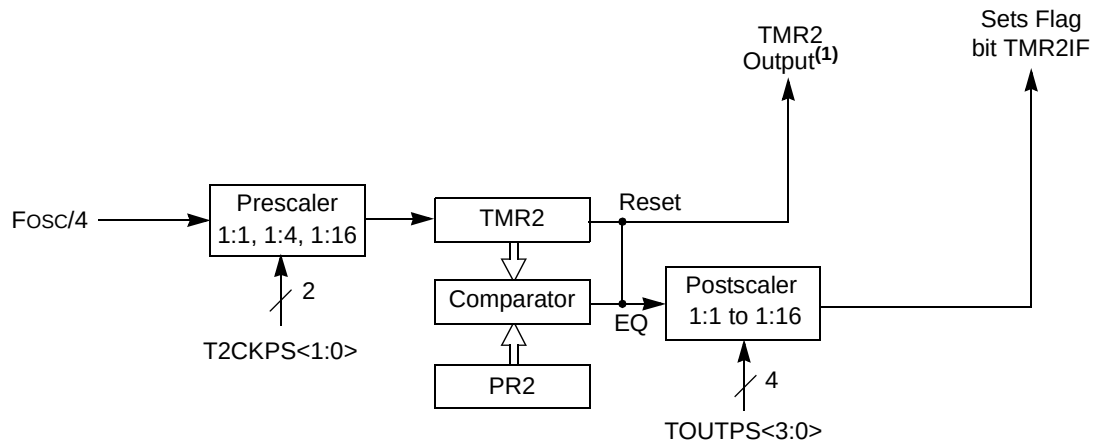
7.2 Timer2 Interrupt

The Timer2 module has an 8-bit period register, PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon Reset.

7.3 Timer2 Output

The output of TMR2 (before the postscaler) is fed to the SSP module, which optionally uses it to generate the shift clock.

FIGURE 7-1: TIMER2 BLOCK DIAGRAM



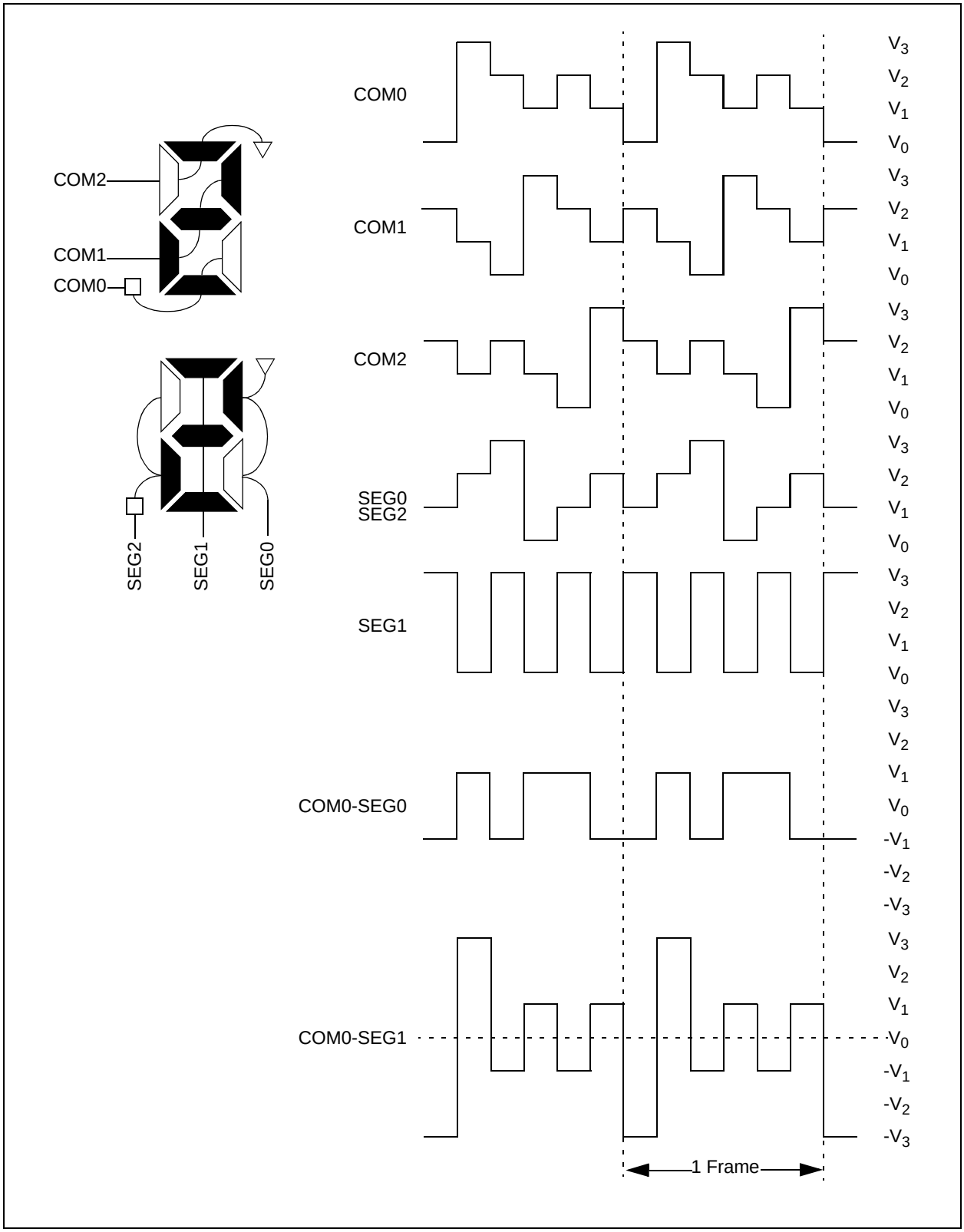
Note 1: TMR2 register output can be software selected by the SSP module as a baud clock.

TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER2

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Bh/ 8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
0Ch	PIR1	EEIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
11h	TMR2	Holding Register for the 8-bit TMR2 Register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
8Ch	PIE1	EEIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
92h	PR2	Timer2 Period Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, – = unimplemented, read as '0'. Shaded cells are not used by the Timer2 module.

FIGURE 9-13: TYPE-A WAVEFORMS IN 1/3 MUX, 1/3 BIAS DRIVE



9.8 LCD Interrupts

The LCD timing generation provides an interrupt that defines the LCD frame timing. This interrupt can be used to coordinate the writing of the pixel data with the start of a new frame. Writing pixel data at the frame boundary allows a visually crisp transition of the image. This interrupt can also be used to synchronize external events to the LCD.

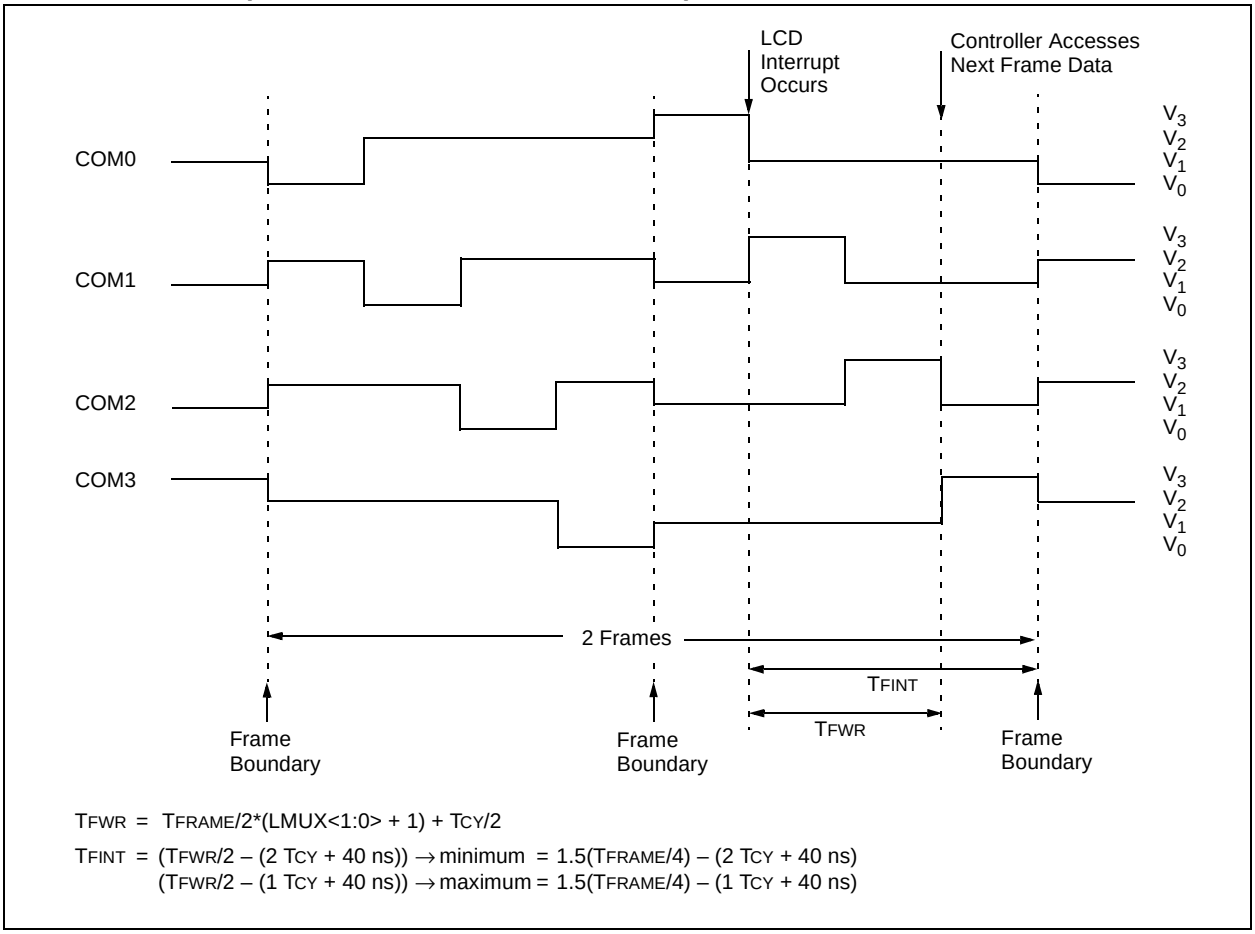
A new frame is defined to begin at the leading edge of the COM0 common signal. The interrupt will be set immediately after the LCD controller completes accessing all pixel data required for a frame. This will occur at a fixed interval before the frame boundary (TFINT), as shown in Figure 9-17. The LCD controller will begin to access data for the next frame within the interval from the interrupt to when the controller begins to access data after the interrupt (TFWR). New data must be written within TFWR, as this is when the LCD controller will begin to access the data for the next frame.

When the LCD driver is running with Type-B waveforms and the LMUX<1:0> bits are not equal to '00', there are some additional issues that must be addressed. Since the DC voltage on the pixel takes two frames to maintain zero volts, the pixel data must not change between subsequent frames. If the pixel data were allowed to change, the waveform for the odd frames would not necessarily be the complement of the waveform generated in the even frames and a DC component would be introduced into the panel. Therefore, when using Type-B waveforms, the user must synchronize the LCD pixel updates to occur within a subframe after the frame interrupt.

To correctly sequence writing while in Type-B, the interrupt will only occur on complete phase intervals. If the user attempts to write when the write is disabled, the WERR (LCDCON<5>) bit is set.

Note:	The interrupt is not generated when the Type-A waveform is selected and when the Type-B with no multiplex (static) is selected.

FIGURE 9-17: WAVEFORMS AND INTERRUPT TIMING IN QUARTER-DUTY CYCLE DRIVE (EXAMPLE – TYPE-B, NON-STATIC)



$T_{FWR} = T_{FRAME}/2*(LMUX<1:0> + 1) + T_{CY}/2$

$T_{FINT} = (T_{FWR}/2 – (2\ T_{CY} + 40\ ns)) \rightarrow \text{minimum} = 1.5(T_{FRAME}/4) – (2\ T_{CY} + 40\ ns)$
$(T_{FWR}/2 – (1\ T_{CY} + 40\ ns)) \rightarrow \text{maximum} = 1.5(T_{FRAME}/4) – (1\ T_{CY} + 40\ ns)$

FIGURE 11-4: USART RECEIVE BLOCK DIAGRAM

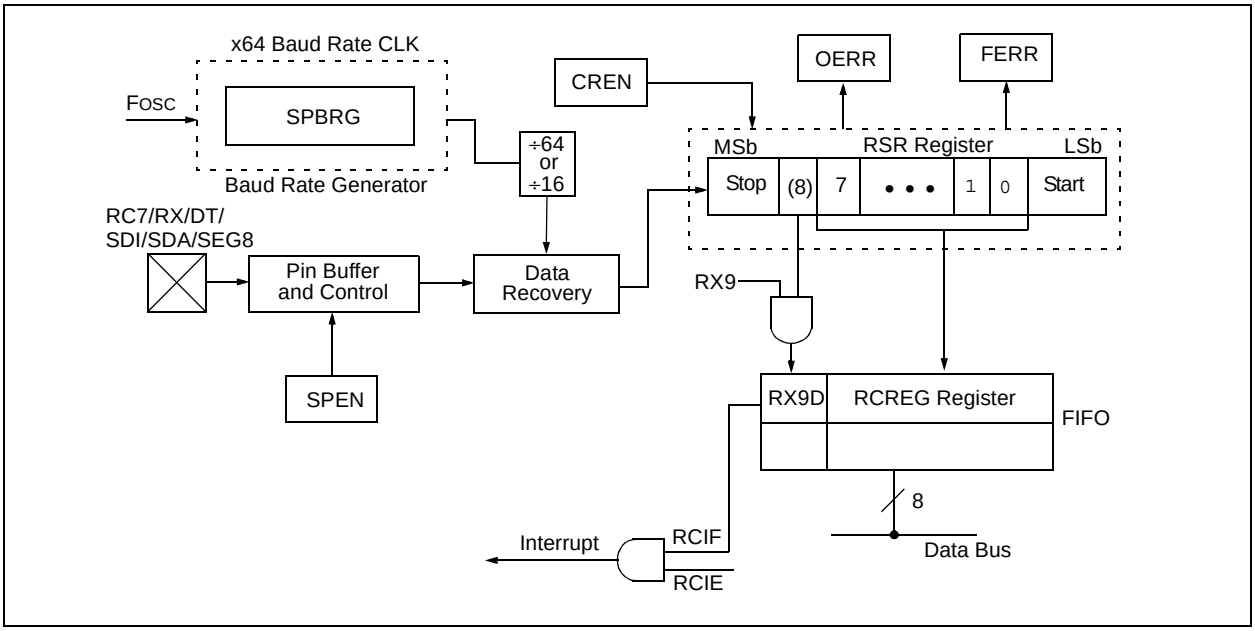
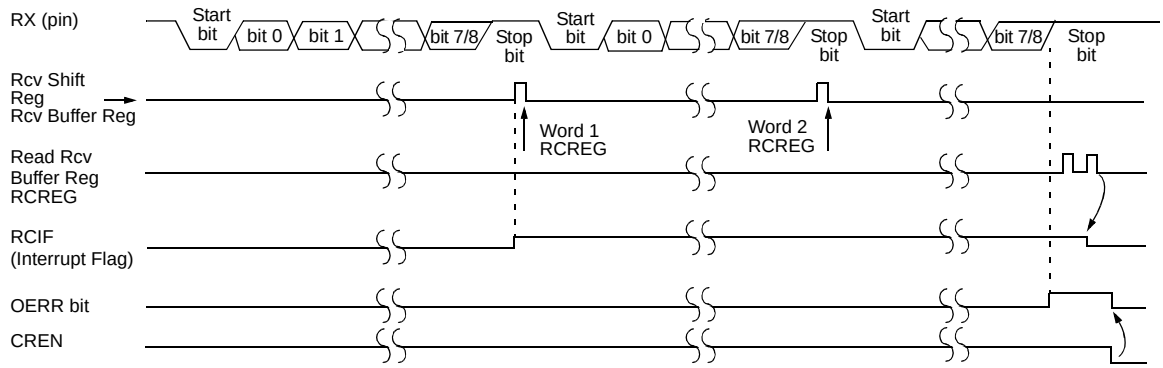


FIGURE 11-5: ASYNCHRONOUS RECEPTION



Note: This timing diagram shows three words appearing on the RX input. The RCREG (Receive Buffer) is read after the third word, causing the OERR (Overrun Error) bit to be set.

TABLE 11-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000x
0Ch	PIR1	EEIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
1Ah	RCREG	USART Receive Data Register								0000 0000	0000 0000
8Ch	PIE1	EEIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, – = unimplemented locations read as '0'. Shaded cells are not used for asynchronous reception.

12.1 A/D Configuration and Operation

There are three registers available to control the functionality of the A/D module:

1. ANSEL (Register 12-1)
2. ADCON0 (Register 12-2)
3. ADCON1 (Register 12-3)

12.1.1 ANALOG PORT PINS

The ANS<7:0> bits (ANSEL<7:0>) and the TRIS bits control the operation of the A/D port pins. Set the corresponding TRIS bits to set the pin output driver to its high-impedance state. Likewise, set the corresponding ANSEL bit to disable the digital input buffer.

Note:	Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.

12.1.2 CHANNEL SELECTION

There are up to eight analog channels on the PIC16F946, AN<7:0>. The CHS<2:0> bits (ADCON0<4:2>) control which channel is connected to the sample and hold circuit.

12.1.3 VOLTAGE REFERENCE

There are two options for each reference to the A/D converter, VREF+ and VREF-. VREF+ can be connected to either VDD or an externally applied voltage. Alternatively, VREF- can be connected to either VSS or an externally applied voltage. VCFG<1:0> bits are used to select the reference source.

12.1.4 CONVERSION CLOCK

The A/D conversion cycle requires 11 TAD. The source of the conversion clock is software selectable via the ADCS bits (ADCON1<6:4>). There are seven possible clock options:

- FOSC/2
- FOSC/4
- FOSC/8
- FOSC/16
- FOSC/32
- FOSC/64
- FRC (dedicated internal oscillator)

For correct conversion, the A/D conversion clock (1/TAD) must be selected to ensure a minimum TAD of 1.6 µs. Table 12-1 shows a few TAD calculations for selected frequencies.

TABLE 12-1: TAD VS. DEVICE OPERATING FREQUENCIES

A/D Clock Source (TAD)		Device Frequency			
Operation	**ADCS<2:0>**	**20 MHz**	**5 MHz**	**4 MHz**	**1.25 MHz**
2 TOSC	000	100 ns(2)	400 ns(2)	500 ns(2)	1.6 µs
4 TOSC	100	200 ns(2)	800 ns(2)	1.0 µs(2)	3.2 µs
8 TOSC	001	400 ns(2)	1.6 µs	2.0 µs	6.4 µs
16 TOSC	101	800 ns(2)	3.2 µs	4.0 µs	12.8 µs(3)
32 TOSC	010	1.6 µs	6.4 µs	8.0 µs(3)	25.6 µs(3)
64 TOSC	110	3.2 µs	12.8 µs(3)	16.0 µs(3)	51.2 µs(3)
A/D RC	x11	2-6 µs(1,4)	2-6 µs(1,4)	2-6 µs(1,4)	2-6 µs(1,4)

Legend: Shaded cells are outside of recommended range.

Note 1: The A/D RC source has a typical TAD time of 4 µs for VDD > 3.0V.

2: These values violate the minimum required TAD time.

3: For faster conversion times, the selection of another clock source is recommended.

4: When the device frequency is greater than 1 MHz, the A/D RC clock source is only recommended if the conversion will be performed during Sleep.

12.1.5 STARTING A CONVERSION

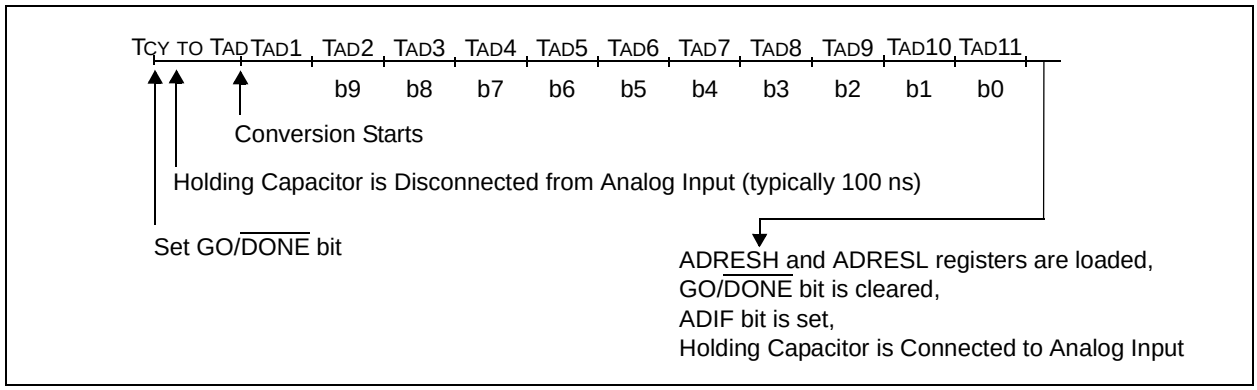
The A/D conversion is initiated by setting the GO/$\overline{\text{DONE}}$ bit (ADCON0<1>). When the conversion is complete, the A/D module:

- Clears the GO/$\overline{\text{DONE}}$ bit
- Sets the ADIF flag (PIR1<6>)
- Generates an interrupt (if enabled)

If the conversion must be aborted, the GO/$\overline{\text{DONE}}$ bit can be cleared in software. The ADRESH:ADRESL registers will not be updated with the partially complete A/D conversion sample. Instead, the ADRESH:ADRESL registers will retain the value of the previous conversion. After an aborted conversion, a 2 TAD delay is required before another acquisition can be initiated. Following the delay, an input acquisition is automatically started on the selected channel.

Note:	The GO/$\overline{\text{DONE}}$ bit should not be set in the same instruction that turns on the A/D.

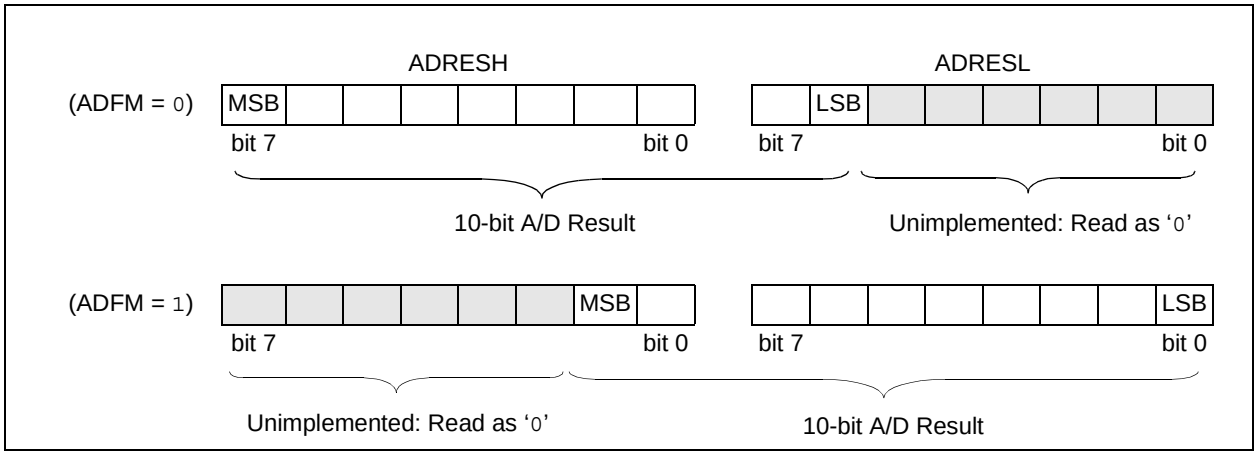
FIGURE 12-2: A/D CONVERSION TAD CYCLES



12.1.6 CONVERSION OUTPUT

The A/D conversion can be supplied in two formats: left or right shifted. The ADFM bit (ADCON0<7>) controls the output format. Figure 12-3 shows the output formats.

FIGURE 12-3: 10-BIT A/D RESULT FORMAT



REGISTER 12-3: ADCON1 – A/D CONTROL REGISTER 1 (ADDRESS: 9Fh)

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	ADCS2	ADCS1	ADCS0	—	—	—	—
bit 7							bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **ADCS<2:0>:** A/D Conversion Clock Select bits

000 = FOSC/2
001 = FOSC/8
010 = FOSC/32
x11 = FRC (clock derived from a dedicated internal oscillator = 500 kHz max.)
100 = FOSC/4
101 = FOSC/16
110 = FOSC/64

bit 3-0 **Unimplemented:** Read as '0'

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

12.1.7 CONFIGURING THE A/D

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as inputs.

To determine sample time, see **Section 19.0 "Electrical Specifications"**. After this sample time has elapsed, the A/D conversion can be started.

These steps should be followed for an A/D conversion:

1. Configure the A/D module:
   - Configure analog/digital I/O (ANSEL)
   - Configure voltage reference (ADCON0)
   - Select A/D input channel (ADCON0)
   - Select A/D conversion clock (ADCON1)
   - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
   - Clear ADIF bit (PIR1<6>)
   - Set ADIE bit (PIE1<6>)
   - Set PEIE and GIE bits (INTCON<7:6>)
3. Wait the required acquisition time.
4. Start conversion:
   - Set GO/$\overline{\text{DONE}}$ bit (ADCON0<1>)
5. Wait for A/D conversion to complete, by either:
   - Polling for the GO/$\overline{\text{DONE}}$ bit to be cleared (with interrupts disabled); OR
   - Waiting for the A/D interrupt
6. Read A/D Result register pair (ADRESH:ADRESL); clear bit ADIF if required.
7. For next conversion, go to step 1 or step 2 as required. The A/D conversion time per bit is defined as T_{AD}. A minimum wait of 2 T_{AD} is required before the next acquisition starts.

EXAMPLE 12-1: A/D CONVERSION

```
;This code block configures the A/D
;for polling, Vdd reference, R/C clock
;and RA0 input.
;
;Conversion start and wait for complete
;polling code included.
;
 BSF    STATUS,RP0     ;Bank 1
 MOVLW  B'01110000'    ;A/D RC clock
 MOVWF  ADCON1
 BSF    TRISA,0        ;Set RA0 to input
 BSF    ANSEL,0        ;Set RA0 to analog
 BCF    STATUS,RP0     ;Bank 0
 MOVLW  B'10000001'    ;Right, Vdd Vref, AN0
 MOVWF  ADCON0
 CALL   SampleTime     ;Wait min sample time
 BSF    ADCON0,GO      ;Start conversion
 BTFSC  ADCON0,GO      ;Is conversion done?
 GOTO   $-1            ;No, test again
 MOVF   ADRESH,W       ;Read upper 2 bits
 MOVWF  RESULTHI
 BSF    STATUS,RP0     ;Bank 1
 MOVF   ADRESL,W       ;Read lower 8 bits
 MOVWF  RESULTLO
```

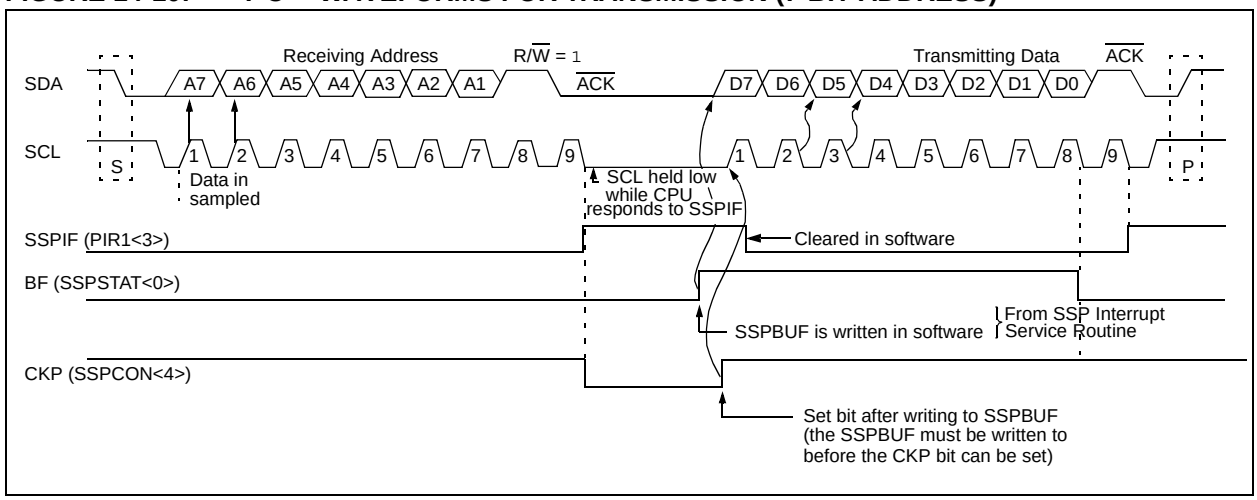

14.12.3 TRANSMISSION

When the R/$\overline{W}$ bit of the incoming address byte is set and an address match occurs, the R/$\overline{W}$ bit of the SSPSTAT register is set. The received address is loaded into the SSPBUF register. The $\overline{ACK}$ pulse will be sent on the ninth bit, and pin RC6/TX/CK/SCK/SCL/SEG9 is held low. The transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then, pin RC6/TX/CK/SCK/SCL/SEG9 should be enabled by setting bit CKP (SSPCON<4>). The master must monitor the SCL pin prior to asserting another clock pulse. The slave devices may be holding off the master by stretching the clock. The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time (Figure 14-10).

An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF must be cleared in software, and the SSPSTAT register is used to determine the status of the byte. Flag bit SSPIF is set on the falling edge of the ninth clock pulse.

As a slave-transmitter, the $\overline{ACK}$ pulse from the master receiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line was high (not $\overline{ACK}$), then the data transfer is complete. When the $\overline{ACK}$ is latched by the slave, the slave logic is reset (resets SSPSTAT register) and the slave then monitors for another occurrence of the Start bit. If the SDA line was low ($\overline{ACK}$), the transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then pin RC6/TX/CK/SCK/SCL/SEG9 should be enabled by setting bit CKP.

FIGURE 14-10: I²C™ WAVEFORMS FOR TRANSMISSION (7-BIT ADDRESS)



REGISTER 15-1: CCP1CON – CCP2CON(1) REGISTER (ADDRESS: 17h/1Dh)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CCPxX	CCPxY	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **CCPxX:CCPxY**: PWM Least Significant bits

Capture mode:
Unused

Compare mode:
Unused

PWM mode:
These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPRxL.

bit 3-0 **CCPxM<3:0>**: CCPx Mode Select bits

0000 = Capture/Compare/PWM disabled (resets CCPx module)
0100 = Capture mode, every falling edge
0101 = Capture mode, every rising edge
0110 = Capture mode, every 4th rising edge
0111 = Capture mode, every 16th rising edge
1000 = Compare mode, set output on match (CCPxIF bit is set)
1001 = Compare mode, clear output on match (CCPxIF bit is set)
1010 = Compare mode, generate software interrupt on match (CCPxIF bit is set, CCPx pin is unaffected)
1011 = Compare mode, trigger special event (CCPxIF bit is set, CCPx pin is unaffected); CCP1 resets TMR1; CCP2 resets TMR1 and starts an A/D conversion (if A/D module is enabled)
11xx = PWM mode

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

19.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings(†)

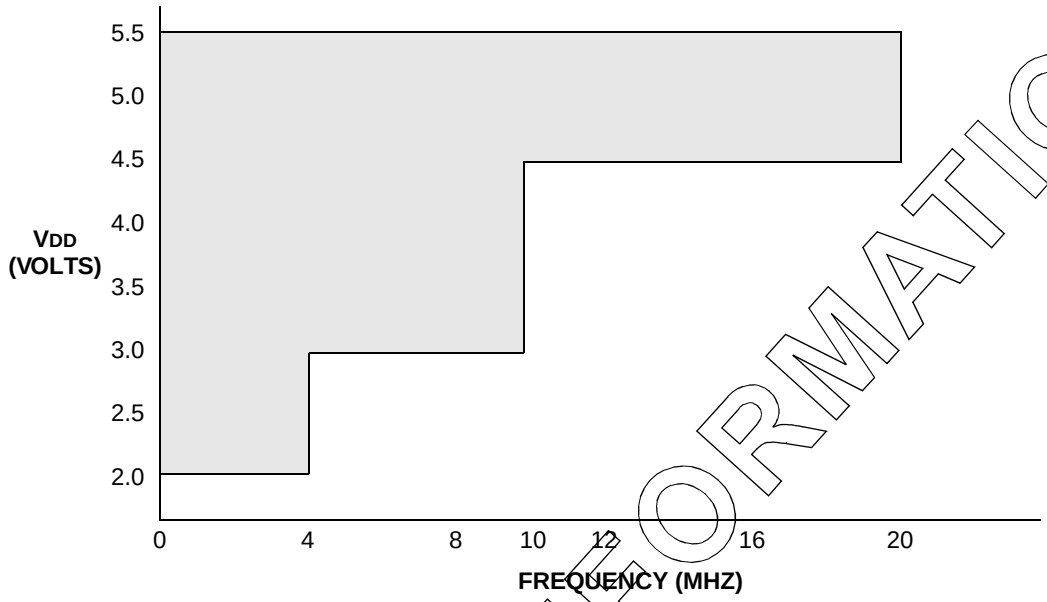
Ambient temperature under bias ..... -40° to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +6.5V
Voltage on $\overline{MCLR}$ with respect to Vss(2) ..... -0.3V to +13.5V
Voltage on all other pins with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)
Total power dissipation(1) ..... 1.0 W
Maximum current out of V_{SS} pin ..... 300 mA
Maximum current into V_{DD} pin ..... 250 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output clamp current, I_{OK} (Vo < 0 or Vo >V_{DD}) ..... ±20 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by all ports (combined) ..... 200 mA
Maximum current sourced by all ports (combined) ..... 200 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$.

2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a “low” level to the $\overline{MCLR}$ pin, rather than pulling this pin directly to V_{SS}.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FIGURE 19-1: PIC16F946 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

19.2 DC Characteristics: PIC16F946-I (Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D010	Supply Current (IDD)(1, 2)	—	8	TBD	µA	2.0	FOSC = 32 kHz LP Oscillator mode
		—	11	TBD	µA	3.0	
		—	33	TBD	µA	5.0	
D011		—	110	TBD	µA	2.0	FOSC = 1 MHz XT Oscillator mode
		—	190	TBD	µA	3.0	
		—	330	TBD	µA	5.0	
D012		—	220	TBD	µA	2.0	FOSC = 4 MHz XT Oscillator mode
		—	370	TBD	µA	3.0	
		—	0.6	TBD	mA	5.0	
D013		—	70	TBD	µA	2.0	FOSC = 1 MHz EC Oscillator mode
		—	140	TBD	µA	3.0	
		—	260	TBD	µA	5.0	
D014		—	180	TBD	µA	2.0	FOSC = 4 MHz EC Oscillator mode
		—	320	TBD	µA	3.0	
		—	500	TBD	µA	5.0	
D015		—	5	TBD	µA	2.0	FOSC = 31 kHz INTOSC mode
		—	14	TBD	µA	3.0	
		—	30	TBD	mA	5.0	
D016		—	340	TBD	µA	2.0	FOSC = 4 MHz INTOSC mode
		—	500	TBD	µA	3.0	
		—	0.8	TBD	mA	5.0	
D017		—	180	TBD	µA	2.0	FOSC = 4 MHz EXTRC mode
		—	320	TBD	µA	3.0	
		—	580	TBD	µA	5.0	
D018		—	2.1	TBD	mA	4.5	FOSC = 20 MHz HS Oscillator mode
		—	3.0	TBD	mA	5.0	

Legend: TBD = To Be Determined

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral ∆ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

4: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

19.3 DC Characteristics: PIC16F946-E (Extended) (Continued)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D020E	**Power-down Base Current (IPD)(4)**	—	0.1	TBD	µA	2.0	WDT, BOR, Comparators, VREF and T1OSC disabled
		—	0.5	TBD	µA	3.0	
		—	0.75	TBD	µA	5.0	
D021E		—	0.6	TBD	µA	2.0	WDT Current
		—	1.8	TBD	µA	3.0	
		—	8.4	TBD	µA	5.0	
D022E		—	58	TBD	µA	3.0	BOR Current
		—	75	TBD	µA	5.0	
D023E		—	35	TBD	µA	2.0	Comparator Current(3)
		—	65	TBD	µA	3.0	
		—	130	TBD	µA	5.0	
D024E		—	40	TBD	µA	2.0	CVREF Current
		—	50.5	TBD	µA	3.0	
		—	80	TBD	µA	5.0	
D025E		—	2.1	TBD	µA	2.0	T1OSC Current
		—	2.5	TBD	µA	3.0	
		—	3.4	TBD	µA	5.0	
D026E		—	1.2	TBD	µA	3.0	A/D Current(3)
		—	0.0022	TBD	µA	5.0	

Legend: TBD = To Be Determined

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

4: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

19.4 DC Characteristics: PIC16F946-I (Industrial), PIC16F946-E (Extended) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin	—	—	15*	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	CIO	All I/O pins	—	—	50*	pF	
		Data EEPROM Memory					
D120	ED	Byte Endurance	100K	1M	—	E/W	-40°C ≤ TA ≤ +85°C
D120A	ED	Byte Endurance	10K	100K	—	E/W	+85°C ≤ TA ≤ +125°C
D121	VDRW	VDD for Read/Write	VMIN	—	5.5	V	Using EECON1 to read/write VMIN = Minimum operating voltage
D122	TDEW	Erase/Write Cycle Time	—	5	6	ms	
D123	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated
D124	TREF	Number of Total Erase/Write Cycles before Refresh(2)	1M	10M	—	E/W	-40°C ≤ TA ≤ +85°C
		Program Flash Memory					
D130	EP	Cell Endurance	10K	100K	—	E/W	-40°C ≤ TA ≤ +85°C
D130A	ED	Cell Endurance	1K	10K	—	E/W	+85°C ≤ TA ≤ +125°C
D131	VPR	VDD for Read	VMIN	—	5.5	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for Erase/Write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	2	2.5	ms	
D134	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device:	PIC16F946[1], PIC16F946T[2]
Temperature Range:	I = -40°C to +85°C E = -40°C to +125°C
Package:	PT = TQFP (Thin Quad Flatpack)
Pattern:	3-Digit Pattern Code for QTP (blank otherwise)

Examples:

a) PIC16F946-E/SP 301 = Extended Temp., skinny PDIP package, 20 MHz, QTP pattern #301

b) PIC16F946-I/SO = Industrial Temp., SOIC package, 20 MHz

Note 1: F = Standard Voltage Range
LF = Wide Voltage Range

2: T = In tape and reel.

* JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirement of each oscillator type.