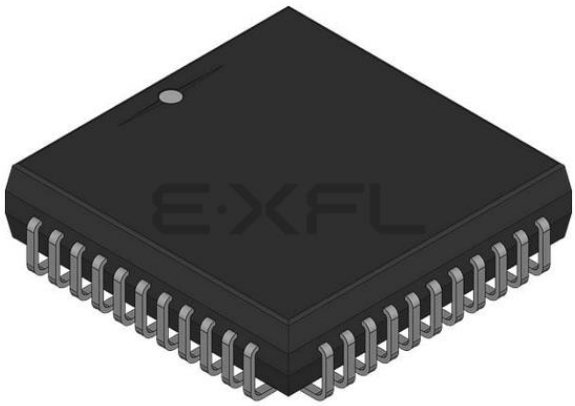

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	20 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	24
Number of Gates	2500
Number of I/O	24
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/atf2500c-20jc

The ATF2500C is organized around a single universal array. All pins and feedback terms are always available to every macrocell. Each of the 38 logic pins are array inputs, as are the outputs of each flip-flop.

In the ATF2500C, four product terms are input to each sum term. Furthermore, each macrocell's three sum terms can be combined to provide up to 12 product terms per sum term with no performance penalty. Each flip-flop is individually selectable to be either D- or T-type, providing further logic compaction. Also, 24 of the flip-flops may be bypassed to provide internal combinatorial feedback to the logic array.

Product terms provide individual clocks and asynchronous resets for each flip-flop. The flip-flops may also be individually configured to have direct input pin clocking. Each output has its own enable product term. Eight synchronous preset product terms serve local groups of either four or eight flip-flops. Register preload functions are provided to simplify testing. All registers automatically reset upon power-up.

2. Pin Configurations

Table 2-1. Pin Configurations

Pin Name	Function
IN	Logic Inputs
CLK/IN	Pin Clock and Input
I/O	Bi-directional Buffers
I/O 0,2,4...	Even I/O Buffers
I/O 1,3,5...	Odd I/O Buffers
GND	Ground
VCC	+5V Supply

Figure 2-1. DIP

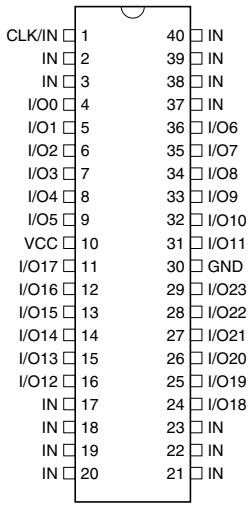
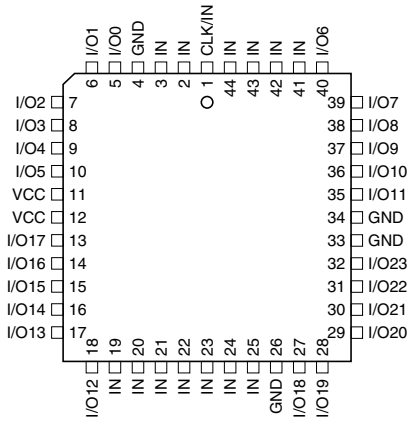


Figure 2-2. PLCC



Note: (PLCC package) pin 4 and pin 26 GND connections are not required, but are recommended for improved noise immunity.

3. Using the ATF2500C Family's Many Advanced Features

The ATF2500Cs advanced flexibility packs more usable gates into 44 leads than other PLDs. Some of the ATF2500Cs key features are:

- **Fully Connected Logic Array –** Each array input is always available to every product term. This makes logic placement a breeze.
- **Selectable D- and T-Type Registers –** Each ATF2500C flip-flop can be individually configured as either D- or T-type. Using the T-type configuration, JK and SR flip-flops are also easily created. These options allow more efficient product term usage.
- **Buried Combinatorial Feedback –** Each macrocell's Q2 register may be bypassed to feed its input (D/T2) directly back to the logic array. This provides further logic expansion capability without using precious pin resources.
- **Selectable Synchronous/Asynchronous Clocking –** Each of the ATF2500Cs flip-flops has a dedicated clock product term. This removes the constraint that all registers use the same clock. Buried state machines, counters and registers can all coexist in one device while running on separate clocks. Individual flip-flop clock source selection further allows mixing higher performance pin clocking and flexible product term clocking within one design.
- **A Total of 48 Registers –** The ATF2500C provides two flip-flops per macrocell – a total of 48. Each register has its own clock and reset terms, as well as its own sum term.
- **Independent I/O Pin and Feedback Paths –** Each I/O pin on the ATF2500C has a dedicated input path. Each of the 48 registers has its own feedback term into the array as well. These features, combined with individual product terms for each I/O's output enable, facilitate true bi-directional I/O design.
- **Combinable Sum Terms –** Each output macrocell's three sum terms may be combined into a single term. This provides a fan in of up to 12 product terms per sum term with *no speed penalty.*
- **Programmable Pin-keeper Circuits –** These weak feedback latches are useful for bus interfacing applications. Floating pins can be set to a known state if the Pin-keepers are enabled.
- **User Row (64 bits) –** Use to store information such as unit history.

4. Power-up Reset

The registers in the ATF2500Cs are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state as nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin or terms high, and
3. The clock pin, and any signals from which clock terms are derived, must remain stable during t_{PR}.

Figure 4-1. Power-up Reset Waveform

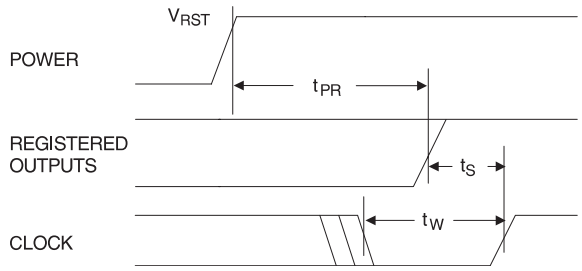


Table 4-1. Power-up Reset

Parameter	Description	Typ	Max	Units
t_{PR}	Power-up Reset Time	600	1000	ns
V_{RST}	Power-up Reset Voltage	3.8	4.5	V

5. Preload and Observability of Registered Outputs

The ATF2500Cs registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the odd I/O pins will force the appropriate register high; a V_{IL} will force it low, independent of the polarity or other configuration bit settings.

The PRELOAD state is entered by placing an 10.25V to 10.75V signal on SMP lead 42. When the preload clock SMP lead 23 is pulsed high, the data on the I/O pins is placed into the 12 registers chosen by the Q select and even/odd select pins.

Register 2 observability mode is entered by placing an 10.25V to 10.75V signal on pin/lead 2. In this mode, the contents of the buried register bank will appear on the associated outputs when the OE control signals are active.

Figure 5-1. Preload Waveforms

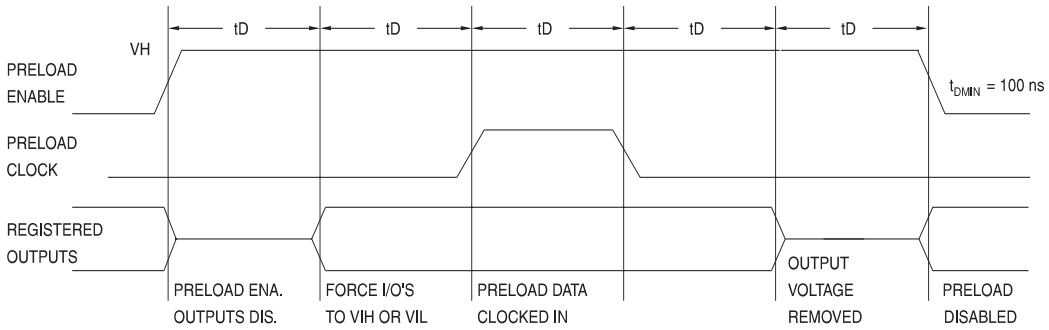


Table 5-1. Preload Levels

Level Forced on Odd I/O Pin during PRELOAD Cycle	Q Select Pin State	Even/Odd Select	Even Q1 State after Cycle	Even Q2 State after Cycle	Odd Q1 State after Cycle	Odd Q2 State after Cycle
V_{IH}/V_{IL}	Low	Low	High/Low	X	X	X
V_{IH}/V_{IL}	High	Low	X	High/Low	X	X
V_{IH}/V_{IL}	Low	High	X	X	High/Low	X
V_{IH}/V_{IL}	High	High	X	X	X	High/Low

6. Software Support

All family members of the ATF2500C can be designed with Atmel-WinCUPL.

Additionally, the ATF2500C may be programmed to perform the ATV2500Hs functional subset (no T-type flip-flops, pin clocking or D/T2 feedback) using the ATV2500H JEDEC file. In this case, the ATF2500C becomes a direct replacement or speed upgrade for the ATV2500H. The ATF2500C are direct replacements for the ATV2500B/BQ and the ATV2500H, including the lack of extra grounds on P4 and P26.

6.1 Software Compiler Mode Selection

Table 6-1. Software Compiler Mode Selection

Device	Atmel - WinCupL Device Mnemonic	Pin-keeper
ATF2500C-DIP	V2500C V2500CPPK	Disabled Enabled
ATF2500C-PLCC	V2500LCC V2500CPPKLCC	Disabled Enabled

6.2 Third Party Programmer Support

Table 6-2. Third Party Programmer Support
Major Third Party Device Programmers support three types of JEDEC files.

Device	Description
ATF2500C (V2500)	**V2500 Cross-programming**. JEDEC file compatible with **standard V2500** JEDEC file (Total fuses in JEDEC file = 71648). The Programmer will automatically disable the User row fuses and also disable the pin-keeper feature. The Fuse checksum will be the same as the old ATV2500H/L file. This Device type is recommended for customers that are directly migrating from an ATV2500H/L device to an ATF2500C device.
ATF2500C (V2500B)	**V2500B Cross-programming**. JEDEC file compatible with **standard V2500B** JEDEC file (Total fuses in JEDEC file = **71745**). The Programmer will automatically disable the User row fuses and also disable the pin-keeper feature. The Fuse checksum will be the same as the old ATV2500B/BQ/BQL/BL file. This Device type is recommended for customers that are directly migrating from an ATV2500B/BQ/BQL/BL device to an ATF2500C device.
ATF2500C	Programming of User Row bits supported and Pin keeper bit is user-programmable. (Total fuses in JEDEC file = **71816**). This is the default device type and is recommended for users that have Re-compiled their Source Design files to specifically target the ATF2500C device.

Note: The ATF2500C has 71816 Jedec fuses.

7. Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of ATF2500C fuse patterns. Once programmed, the outputs will read programmed during verify.

The security fuse should be programmed last, as its effect is immediate.

The security fuse also inhibits Preload and Q2 observability.

8. Bus-friendly Pin-keeper Input and I/O

All ATF2500C family members have programmable internal input and I/O pin-keeper circuits.

The default condition, including when using the AT2500C/CQ family to replace the AT2500B/BQ or AT2500H, is that the pin-keepers are not activated.

When pin-keepers are active, inputs or I/Os not being driven externally will maintain their last driven state. This ensures that all logic array inputs and device outputs are known states. Pin-keepers are relatively weak active circuits that can be easily overridden by TTL-compatible drivers (see input and I/O diagrams below).

Enabling or disabling of the pin-keeper circuits is controlled by the device type chosen in the logic compiler device selection menu. Please refer to the Software Compiler Mode Selection table for more details. Once the pin-keeper circuits are disabled, normal termination procedures required for unused inputs and I/Os.

Figure 8-1. Input Diagram

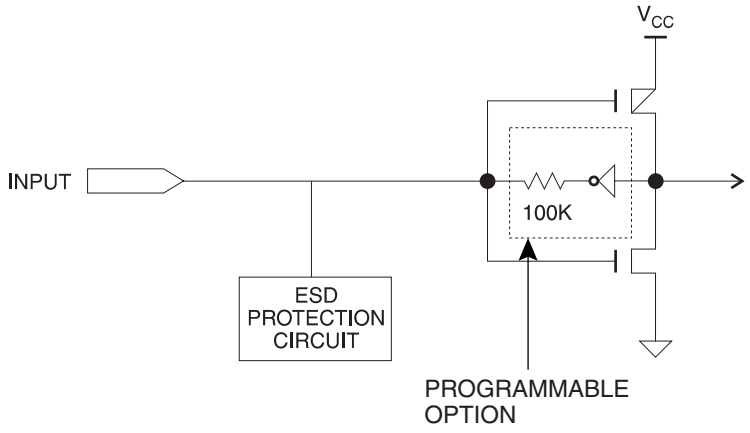
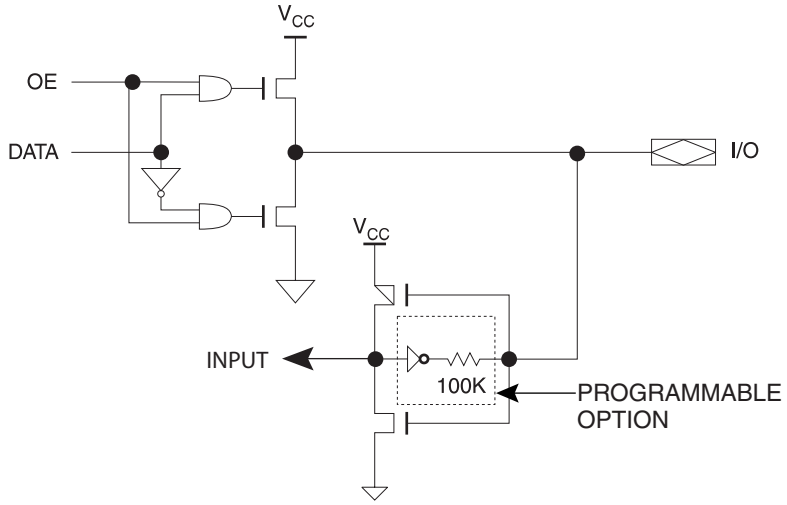


Figure 8-2. I/O Diagram



9. Functional Logic Diagram Description

The ATF2500C functional logic diagram describes the interconnections between the input, feedback pins and logic cells. All interconnections are routed through the single global bus.

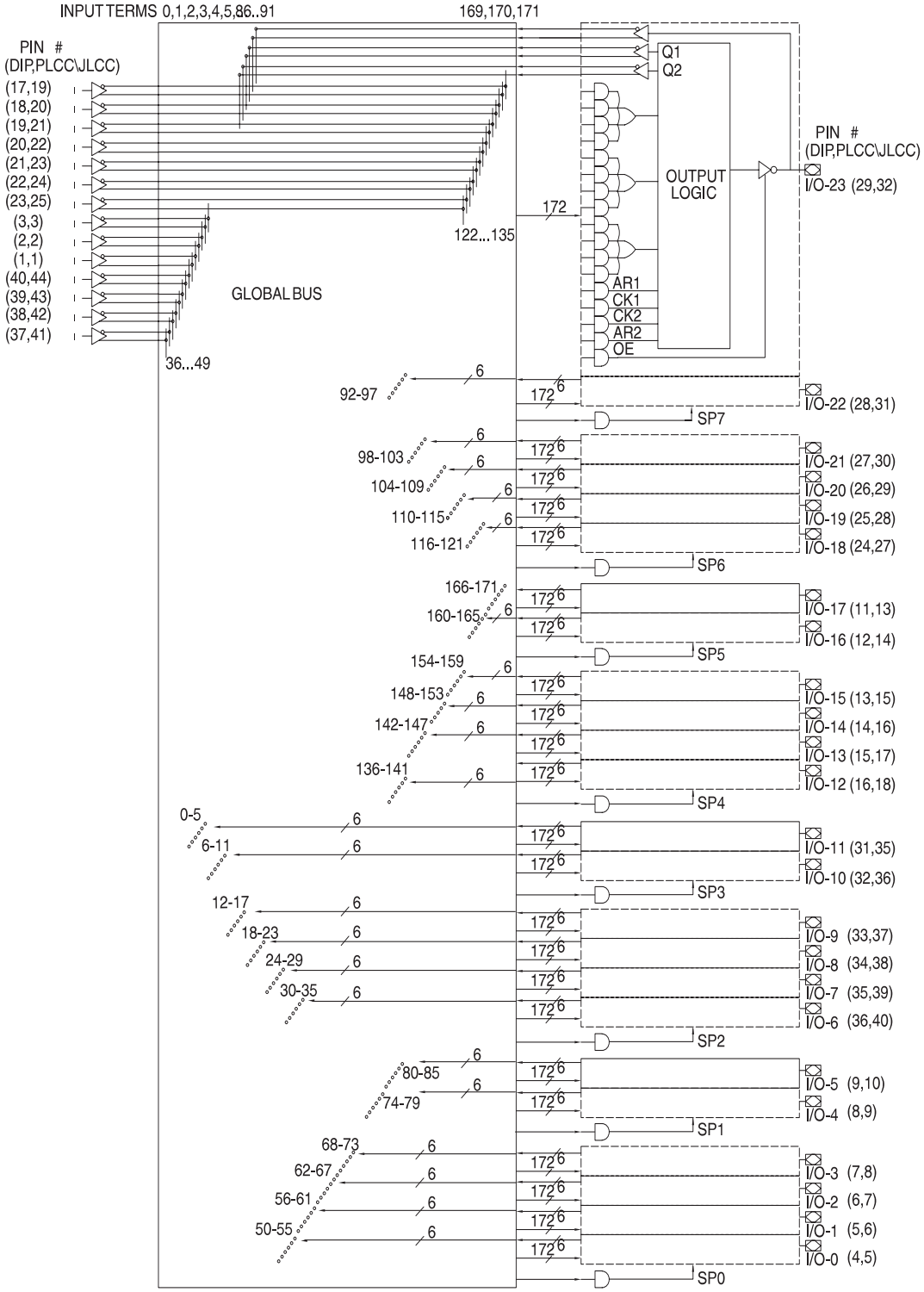
The ATF2500Cs are straightforward and uniform PLDs. The 24 macrocells are numbered 0 through 23. Each macrocell contains 17 AND gates. All AND gates have 172 inputs. The five lower product terms provide AR1, CK1, CK2, AR2, and OE. These are: one asynchronous reset and clock per flip-flop, and an output enable. The top 12 product terms are grouped into three sum terms, which are used as shown in the macrocell diagrams.

Eight synchronous preset terms are distributed in a 2/4 pattern. The first four macrocells share Preset 0, the next two share Preset 1, and so on, ending with the last two macrocells sharing Preset 7.

The 14 dedicated inputs and their complements use the numbered positions in the global bus as shown. Each macrocell provides six inputs to the global bus: (left to right) feedback F2[(1)] true and false, flip-flop Q1 true and false, and the pin true and false. The positions occupied by these signals in the global bus are the six numbers in the bus diagram next to each macrocell.

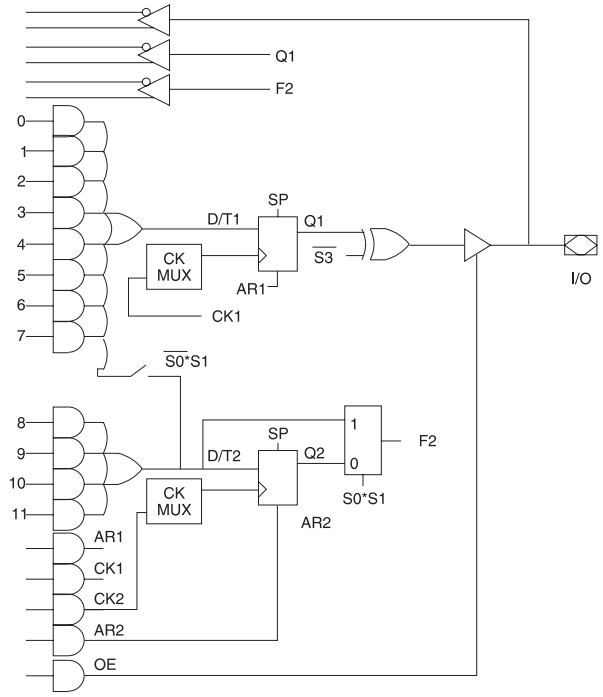
Note: 1. Either the flip-flop input (D/T2) or output (Q2) may be fed back in the ATF2500Cs.

9.1 Functional Logic Diagram ATF2500C



Notes:
1. Pin 4 and Pin 26 are “ground” connections and are not required for PLCC, LCC and JLCC versions of ATF2500C, making them compatible with ATV2500H, ATV2500B and ATV2500BQ pinouts.
2. For DIP package, VCC = P10 and GND = P30. For, PLCC, LCC and JLCC packages, VCC = P11 and P12, GND = P33 and P34, and GND = P4, P26 (See Note 1, above).

9.2 Output Logic, Registered[1]



S2 = 0		Terms in		
S1	S0	D/T1	D/T2	Output Configuration
0	0	8	4	Registered (Q1); Q2 FB
1	0	12	4[1]	Registered (Q1); Q2 FB
1	1	8	4	Registered (Q1); D/T2 FB

S3	Output Configuration
0	Active Low
1	Active High

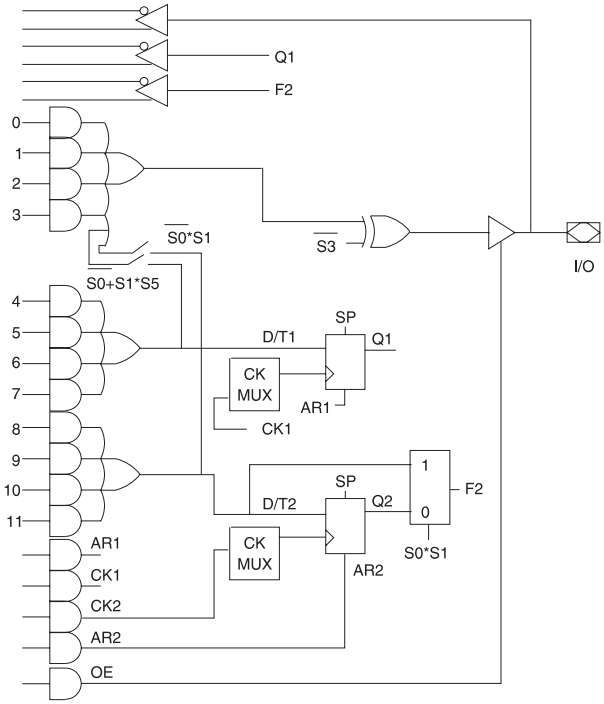
S6	Q1 CLOCK
0	CK1
1	CK1 • PIN1

S4	Register 1 Type
0	D
1	T

S7	Q2 CLOCK
0	CK2
1	CK2 • PIN1

S5	Register 2 Type
0	D
1	T

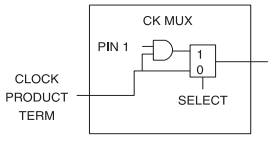
9.3 Output Logic, Combinatorial[1]



S2 = 1			Terms in		
S5	S1	S0	D/T1	D/T2	Output Configuration
X	0	0	4[1]	4	Combinatorial (8 Terms); Q2 FB
X	0	1	4	4	Combinatorial (4 Terms); Q2 FB
X	1	0	4[1]	4[1]	Combinatorial (12 Terms); Q2 FB
1	1	1	4[1]	4	Combinatorial (8 Terms); D/T2 FB
0	1	1	4	4	Combinatorial (4 Terms); D/T2 FB

Note: 1. These four terms are shared with D/T1.

Figure 9-1. Clock Option



Note: 1. These diagrams show equivalent logic functions, not necessarily the actual circuit implementation.

10. Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Junction Temperature	150°C Max
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC which may overshoot to +7.0V for pulses of less than 20 ns.

11. DC and AC Operating Conditions

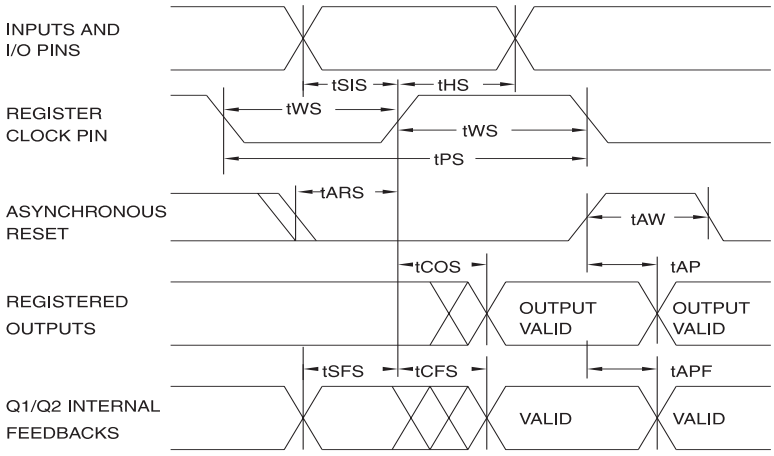
	Commercial	Industrial	Military
Operating Temperature	0°C - 70°C (Ambient)	-40°C - 85°C (Ambient)	-55°C - 125°C (Case)
V_{CC} Power Supply	5V ± 5%	5V ± 10%	5V ± 10%

11.1 ATF2500C DC Characteristics

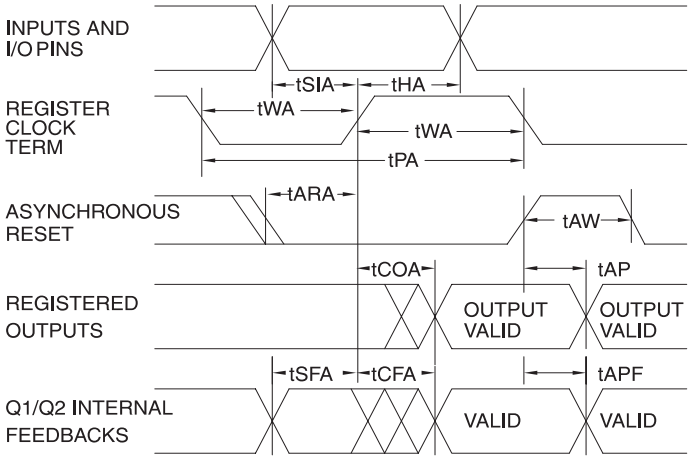
Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V					10	µA
I_{CC}	Power Supply Current Standby	V_{CC} = MAX, V_{IN} = GND or V_{CC} f = 0 MHz, Outputs Open	ATF2500C	Com.		80	110	mA
				Ind., Mil.		80	130	mA
V_{IL}	Input Low Voltage	MIN ≤V_{CC} ≤MAX			-0.6		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC} + 0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = 4.5V	I_{OL} = 8 mA	Com., Ind.			0.5	V
			I_{OL} = 6 mA	Mil.			0.5	V
V_{OH}	Output High Voltage	V_{CC} = MIN	I_{OH} = -100 µA		V_{CC} - 0.3			V
			I_{OH} = -4.0 mA		2.4			

Note: 1. See I_{CC} versus frequency characterization curves.

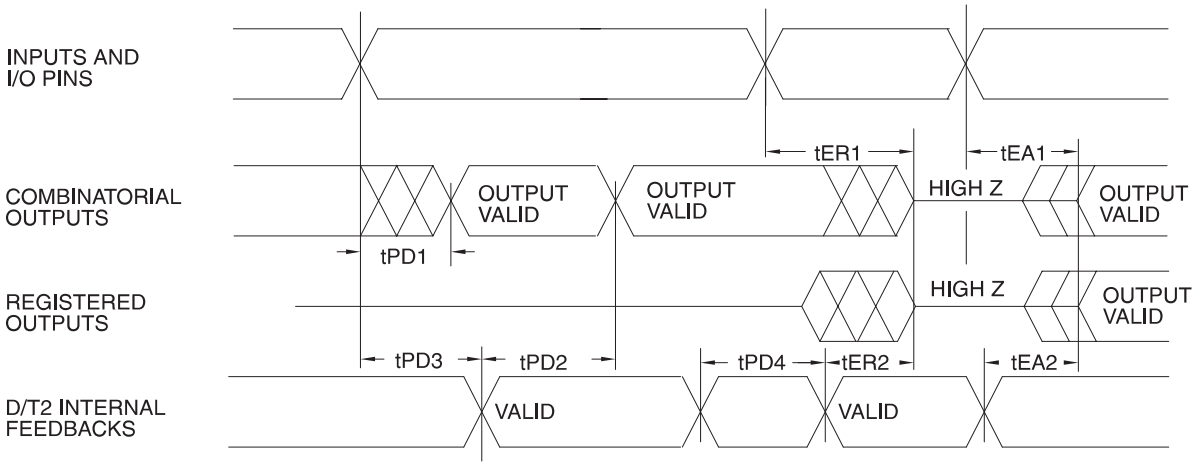
11.2 AC Waveforms[1] Input Pin Clock



11.3 AC Waveforms[1] Product Term Clock



11.4 AC Waveforms[1] Combinatorial Outputs and Feedback



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

11.5 ATF2500C AC Characteristics

Symbol	Parameter	-15		-20		Units
		Min	Max	Min	Max	
t_{PD1}	Input to Non-registered Output		15		20	ns
t_{PD2}	Feedback to Non-registered Output		15		20	ns
t_{PD3}	Input to Non-registered Feedback		11		15	ns
t_{PD4}	Feedback to Non-registered Feedback		11		15	ns
t_{EA1}	Input to Output Enable		15		20	ns
t_{ER1}	Input to Output Disable		15		20	ns
t_{EA2}	Feedback to Output Enable		15		20	ns
t_{ER2}	Feedback to Output Disable		15		20	ns
t_{AW}	Asynchronous Reset Width	8		12		ns
t_{AP}	Asynchronous Reset to Registered Output		18		22	ns
t_{APF}	Asynchronous Reset to Registered Feedback		15		19	ns

11.6 ATF2500C Register AC Characteristics, Input Pin Clock

Symbol	Parameter	-15		-20		Units
		Min	Max	Min	Max	
t_{COS}	Clock to Output		10		11	ns
t_{CFS}	Clock to Feedback	0	5	0	6	ns
t_{SIS}	Input Setup Time	9		14		ns
t_{SFS}	Feedback Setup Time	9		14		ns
t_{HS}	Hold Time	0		0		ns
t_{WS}	Clock Width	6		7		ns
t_{PS}	Clock Period	12		14		ns
F_{MAXS}	External Feedback $1/(t_{SIS} + t_{COS})$		52		40	MHz
	Internal Feedback $1/(t_{SFS} + t_{CFS})$		71		50	MHz
	No Feedback $1/(t_{PS})$		83		71	MHz
t_{ARS}	Asynchronous Reset/Preset Recovery Time	12		15		ns

11.7 ATF2500C Register AC Characteristics, Product Term Clock

Symbol	Parameter	-15		-20		Units
		Min	Max	Min	Max	
t_{COA}	Clock to Output		15		20	ns
t_{CFA}	Clock to Feedback	5	12	10	16	ns
t_{SIA}	Input Setup Time	5		10		ns
t_{SFA}	Feedback Setup Time	5		8		ns
t_{HA}	Hold Time	5		10		ns
t_{WA}	Clock Width	7.5		11		ns
t_{PA}	Clock Period	15		22		ns
F_{MAXA}	External Feedback $1/(t_{SIA} + t_{COA})$		50		33	MHz
	Internal Feedback $1/(t_{SFA} + t_{CFA})$		58		38	MHz
	No Feedback $1/(t_{PS})$		66		45	MHz
t_{ARA}	Asynchronous Reset/Preset Recovery Time	8		12		ns

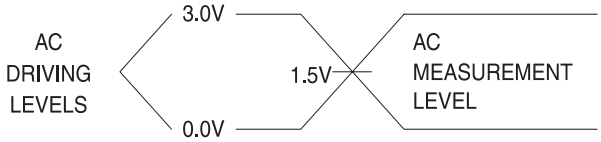
11.8 Pin Capacitance

f = 1 MHz, T = 25°C[1]

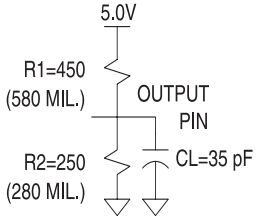
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

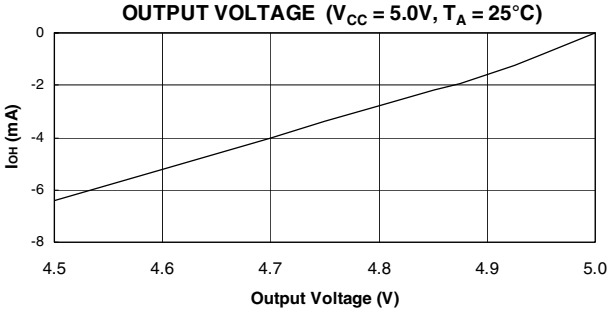
11.9 Test Waveforms and Measurement Levels



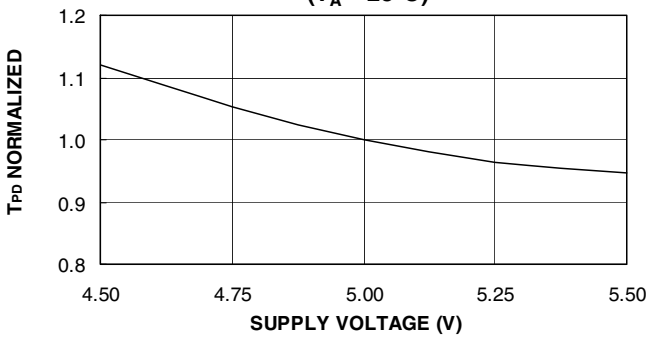
11.10 Output Test Load



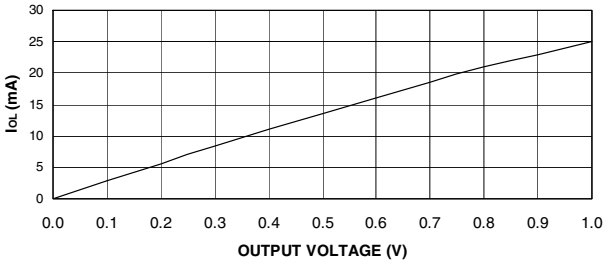
ATF2500C OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



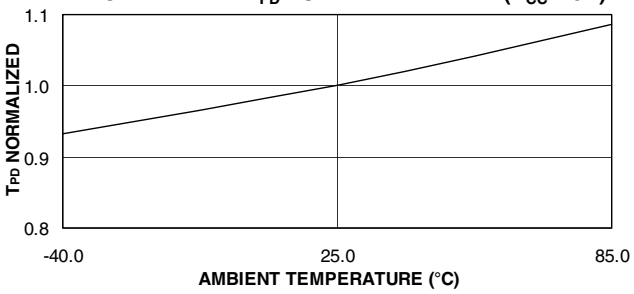
NORMALIZED T_{PD} VS. SUPPLY VOLTAGE (T_A = 25°C)



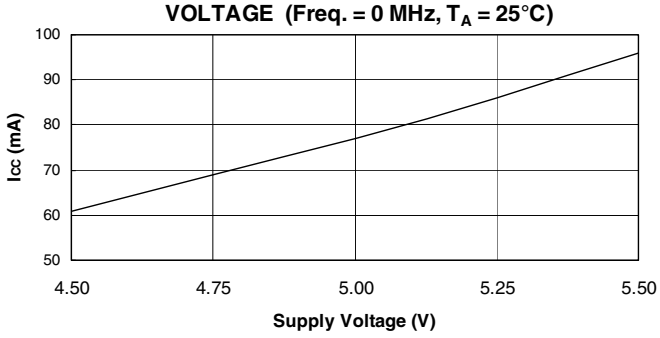
ATF2500C OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5.0V, T_A = 25°C)



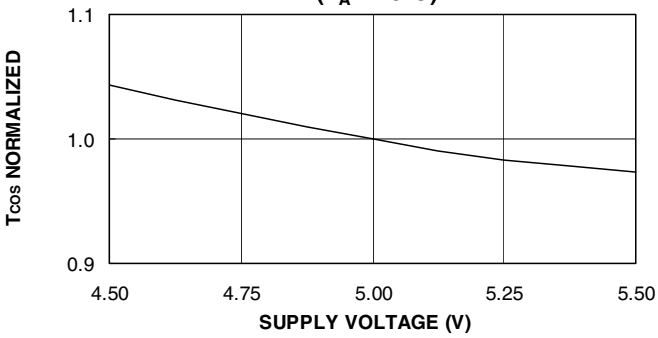
NORMALIZED T_{PD} VS. AMBIENT TEMP (V_{CC} = 5V)



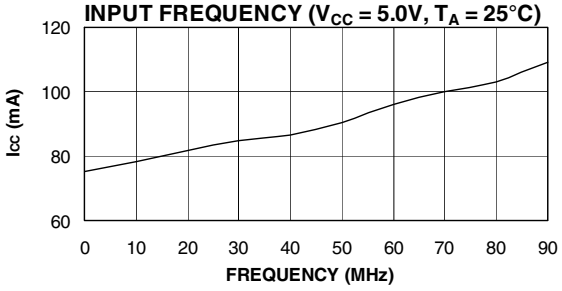
ATF2500C SUPPLY CURRENT VS. SUPPLY VOLTAGE (Freq. = 0 MHz, T_A = 25°C)



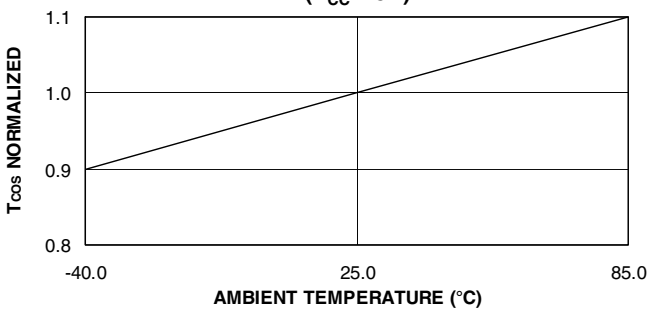
NORMALIZED T_{COS} VS. SUPPLY VOLTAGE (T_A = 25°C)



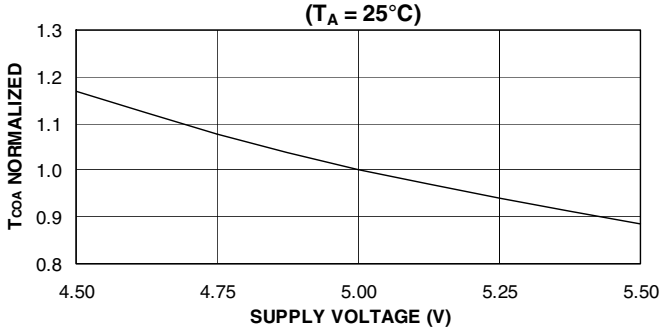
ATF2500C SUPPLY CURRENT VS. INPUT FREQUENCY (V_{CC} = 5.0V, T_A = 25°C)



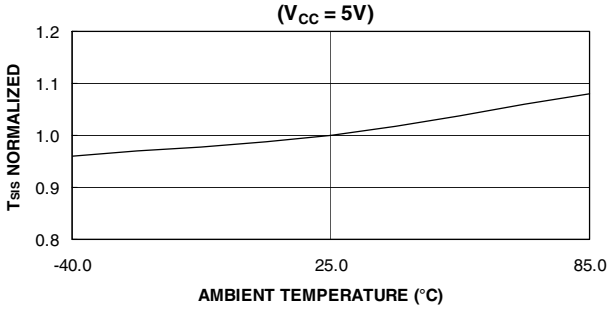
NORMALIZED T_{COS} VS. AMBIENT TEMP (V_{CC} = 5V)



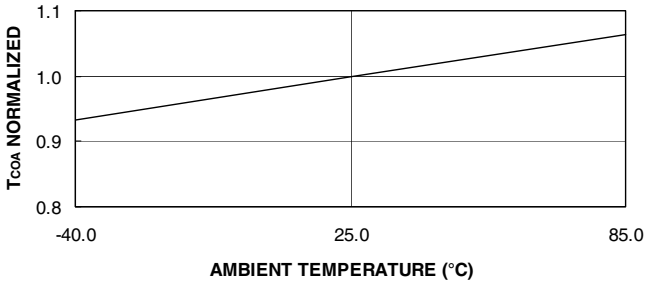
NORMALIZED T_{COA} VS. SUPPLY VOLTAGE
(T_A = 25°C)



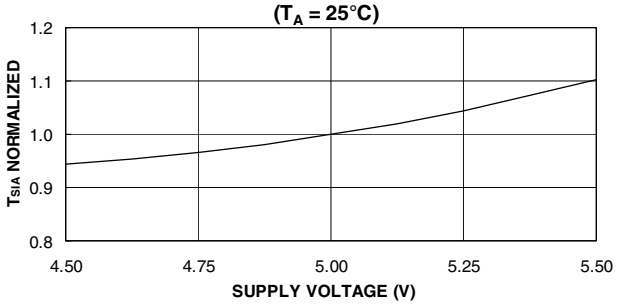
NORMALIZED T_{SIS} VS. AMBIENT TEMP
(V_{CC} = 5V)



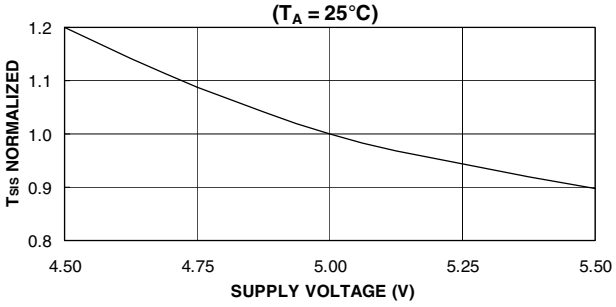
NORMALIZED T_{COA} VS. AMBIENT TEMP
(V_{CC} = 5V)



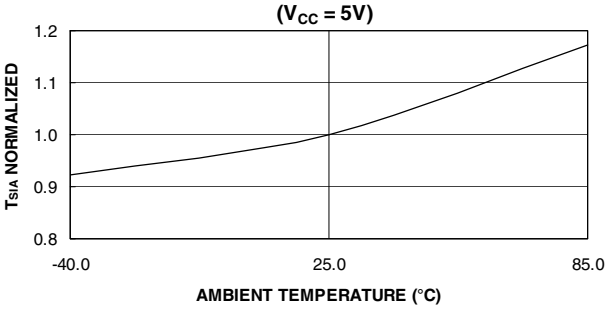
NORMALIZED T_{SIA} VS. SUPPLY VOLTAGE
(T_A = 25°C)



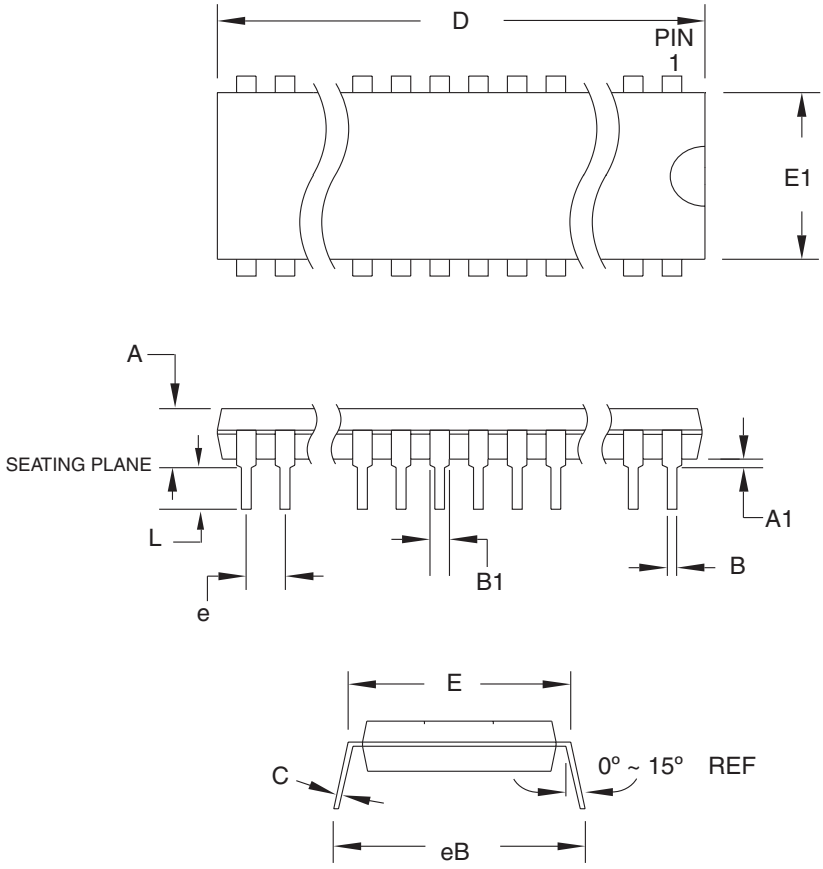
NORMALIZED T_{SIS} VS. SUPPLY VOLTAGE
(T_A = 25°C)



NORMALIZED T_{SIA} VS. AMBIENT TEMP
(V_{CC} = 5V)



14.2 40P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

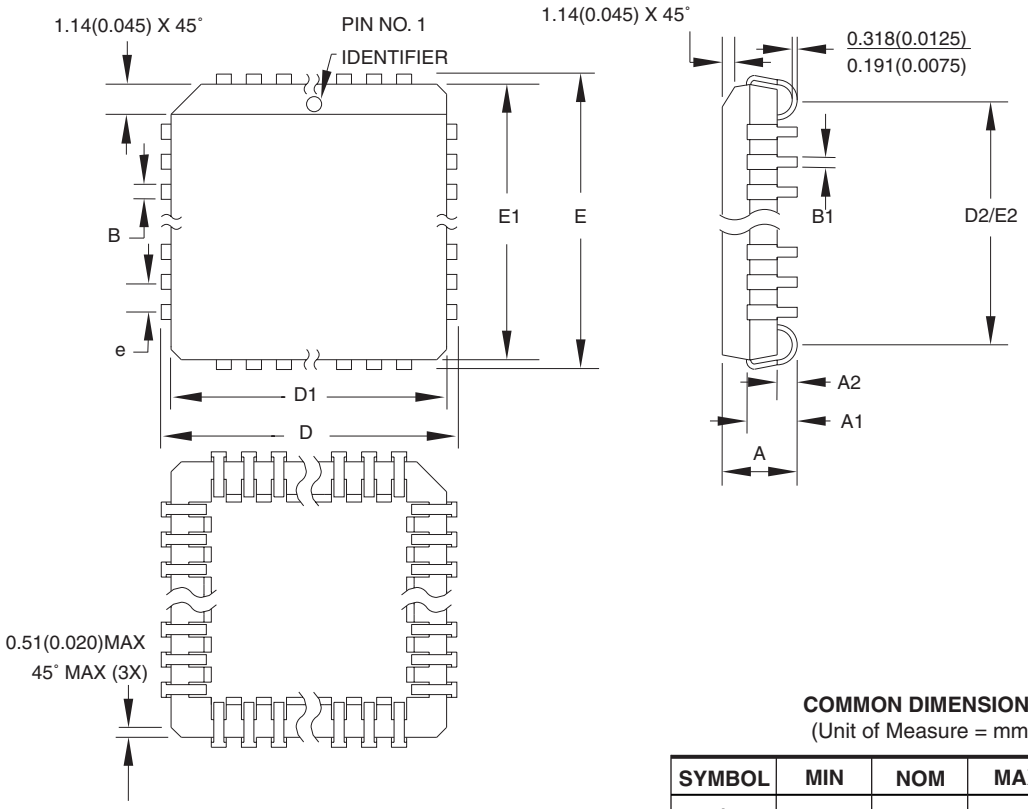
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

14.3 44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

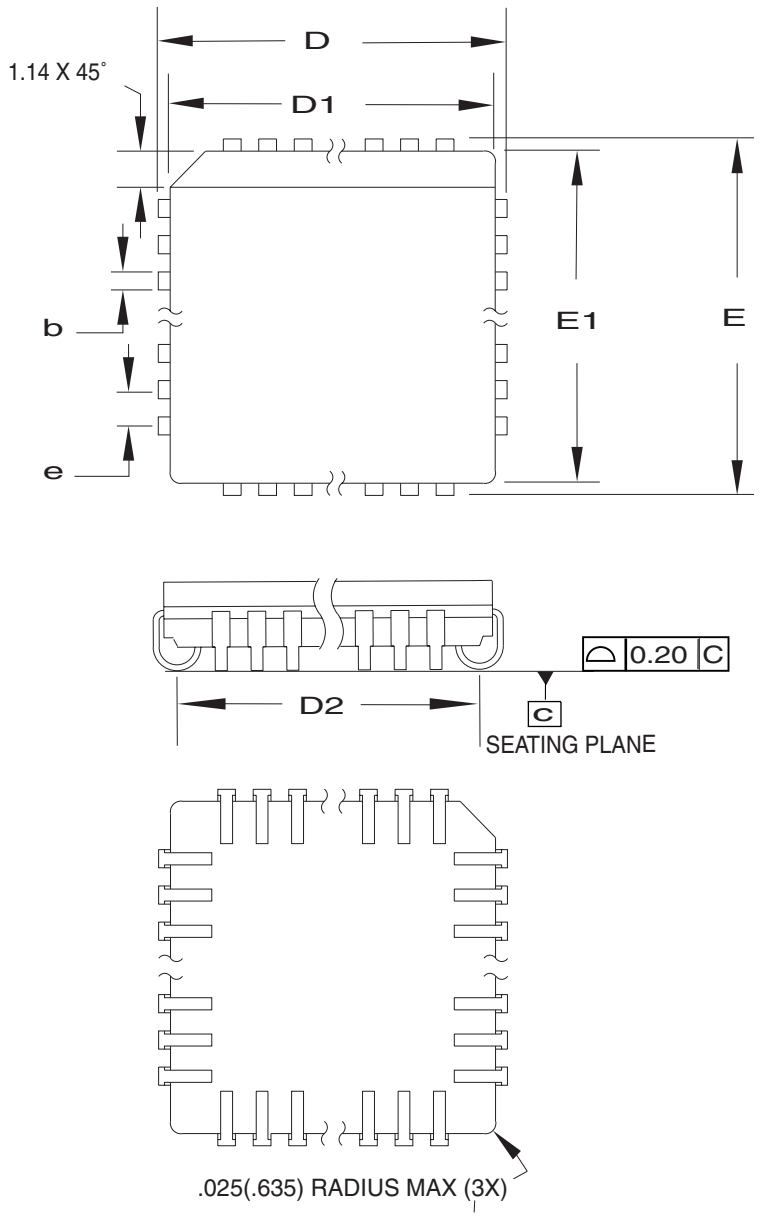
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

14.4 44K – JLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	3.93	4.36	4.57	
A1	2.28	2.66	3.04	
A2	0.89	-	1.14	
D	17.40	17.52	17.65	
D1	16.38	16.63	16.89	
D2	15.00	15.50	16.00	
E	17.40	17.52	17.65	
E1	16.38	16.63	16.89	
E2	15.00	15.50	16.00	
b	0.66	0.73	0.81	
b1	0.43	-	0.58	
c	0.15	-	0.30	
e	1.27 TYP			

Note : Refer to MIL-STD-1835C-J1

09/18/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44K**, 44-lead, Non-windowed, Ceramic J-leaded Chip Carrier (JLCC)	44K	A

15. Revision History

Revision Level – Release Date	History
J – May 2005	Added fully Green and Military temperatures packages in Section 13. ”Ordering Information” on page 18.
K – Jan. 2008	Added 40-pin CerDIP Package Option.

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
pld@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature