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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	20 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	24
Number of Gates	-
Number of I/O	24
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atf2500c-20pu

The ATF2500C is organized around a single universal array. All pins and feedback terms are always available to every macrocell. Each of the 38 logic pins are array inputs, as are the outputs of each flip-flop.

In the ATF2500C, four product terms are input to each sum term. Furthermore, each macrocell's three sum terms can be combined to provide up to 12 product terms per sum term with no performance penalty. Each flip-flop is individually selectable to be either D- or T-type, providing further logic compaction. Also, 24 of the flip-flops may be bypassed to provide internal combinatorial feedback to the logic array.

Product terms provide individual clocks and asynchronous resets for each flip-flop. The flip-flops may also be individually configured to have direct input pin clocking. Each output has its own enable product term. Eight synchronous preset product terms serve local groups of either four or eight flip-flops. Register preload functions are provided to simplify testing. All registers automatically reset upon power-up.

2. Pin Configurations

Table 2-1. Pin Configurations

Pin Name	Function
IN	Logic Inputs
CLK/IN	Pin Clock and Input
I/O	Bi-directional Buffers
I/O 0,2,4...	Even I/O Buffers
I/O 1,3,5...	Odd I/O Buffers
GND	Ground
VCC	+5V Supply

Figure 2-1. DIP

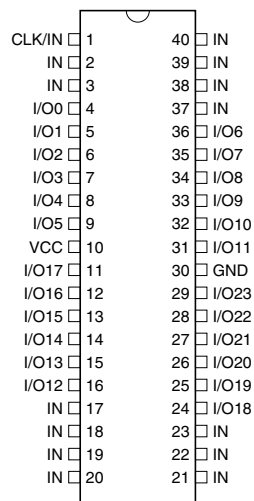
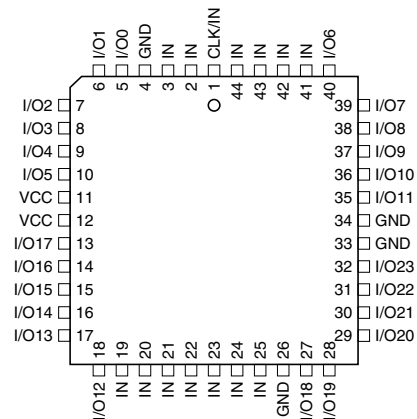


Figure 2-2. PLCC



Note: (PLCC package) pin 4 and pin 26 GND connections are not required, but are recommended for improved noise immunity.

3. Using the ATF2500C Family's Many Advanced Features

The ATF2500Cs advanced flexibility packs more usable gates into 44 leads than other PLDs. Some of the ATF2500Cs key features are:

- **Fully Connected Logic Array** – Each array input is always available to every product term. This makes logic placement a breeze.
- **Selectable D- and T-Type Registers** – Each ATF2500C flip-flop can be individually configured as either D- or T-type. Using the T-type configuration, JK and SR flip-flops are also easily created. These options allow more efficient product term usage.
- **Buried Combinatorial Feedback** – Each macrocell's Q2 register may be bypassed to feed its input (D/T2) directly back to the logic array. This provides further logic expansion capability without using precious pin resources.
- **Selectable Synchronous/Asynchronous Clocking** – Each of the ATF2500Cs flip-flops has a dedicated clock product term. This removes the constraint that all registers use the same clock. Buried state machines, counters and registers can all coexist in one device while running on separate clocks. Individual flip-flop clock source selection further allows mixing higher performance pin clocking and flexible product term clocking within one design.
- **A Total of 48 Registers** – The ATF2500C provides two flip-flops per macrocell – a total of 48. Each register has its own clock and reset terms, as well as its own sum term.
- **Independent I/O Pin and Feedback Paths** – Each I/O pin on the ATF2500C has a dedicated input path. Each of the 48 registers has its own feedback term into the array as well. These features, combined with individual product terms for each I/O's output enable, facilitate true bi-directional I/O design.
- **Combinable Sum Terms** – Each output macrocell's three sum terms may be combined into a single term. This provides a fan in of up to 12 product terms per sum term with *no speed penalty*.
- **Programmable Pin-keeper Circuits** – These weak feedback latches are useful for bus interfacing applications. Floating pins can be set to a known state if the Pin-keepers are enabled.
- **User Row (64 bits)** – Use to store information such as unit history.

4. Power-up Reset

The registers in the ATF2500Cs are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing V_{RST} , all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state as nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin or terms high, and
3. The clock pin, and any signals from which clock terms are derived, must remain stable during t_{PR} .

Figure 4-1. Power-up Reset Waveform

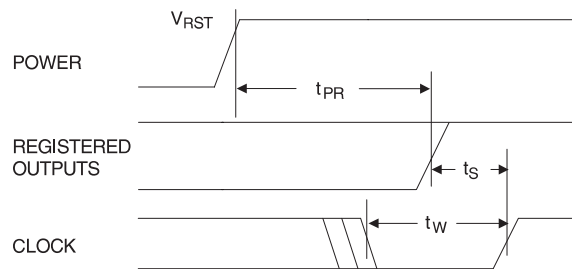


Table 4-1. Power-up Reset

Parameter	Description	Typ	Max	Units
t_{PR}	Power-up Reset Time	600	1000	ns
V_{RST}	Power-up Reset Voltage	3.8	4.5	V

6. Software Support

All family members of the ATF2500C can be designed with Atmel-WinCUPL.

Additionally, the ATF2500C may be programmed to perform the ATV2500Hs functional subset (no T-type flip-flops, pin clocking or D/T2 feedback) using the ATV2500H JEDEC file. In this case, the ATF2500C becomes a direct replacement or speed upgrade for the ATV2500H. The ATF2500C are direct replacements for the ATV2500B/BQ and the ATV2500H, including the lack of extra grounds on P4 and P26.

6.1 Software Compiler Mode Selection

Table 6-1. Software Compiler Mode Selection

Device	Atmel - WinCupL Device Mnemonic	Pin-keeper
ATF2500C-DIP	V2500C	Disabled
	V2500CPPK	Enabled
ATF2500C-PLCC	V2500LCC	Disabled
	V2500CPPKLCC	Enabled

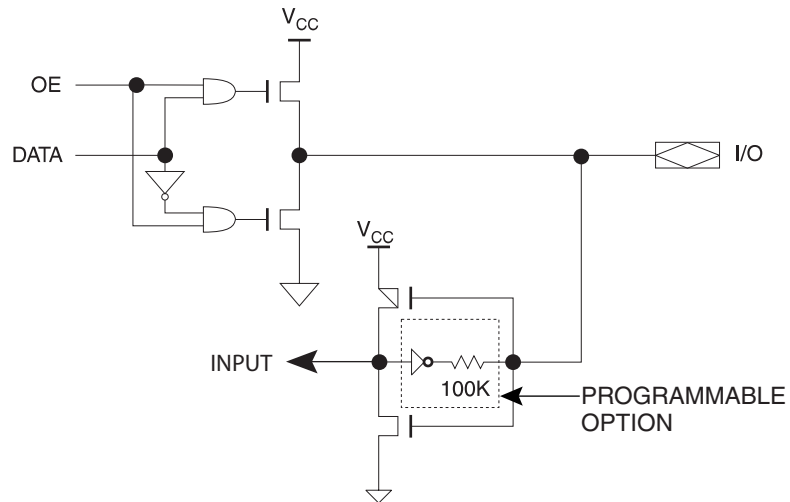
6.2 Third Party Programmer Support

Table 6-2. Third Party Programmer Support
Major Third Party Device Programmers support three types of JEDEC files.

Device	Description
ATF2500C (V2500)	V2500 Cross-programming. JEDEC file compatible with standard V2500 JEDEC file (Total fuses in JEDEC file = 71648). The Programmer will automatically disable the User row fuses and also disable the pin-keeper feature. The Fuse checksum will be the same as the old ATV2500H/L file. This Device type is recommended for customers that are directly migrating from an ATV2500H/L device to an ATF2500C device.
ATF2500C (V2500B)	V2500B Cross-programming. JEDEC file compatible with standard V2500B JEDEC file (Total fuses in JEDEC file = 71745). The Programmer will automatically disable the User row fuses and also disable the pin-keeper feature. The Fuse checksum will be the same as the old ATV2500B/BQ/BQL/BL file. This Device type is recommended for customers that are directly migrating from an ATV2500B/BQ/BQL/BL device to an ATF2500C device.
ATF2500C	Programming of User Row bits supported and Pin keeper bit is user-programmable. (Total fuses in JEDEC file = 71816). This is the default device type and is recommended for users that have Re-compiled their Source Design files to specifically target the ATF2500C device.

Note: The ATF2500C has 71816 Jedec fuses.

Figure 8-2. I/O Diagram



9. Functional Logic Diagram Description

The ATF2500C functional logic diagram describes the interconnections between the input, feedback pins and logic cells. All interconnections are routed through the single global bus.

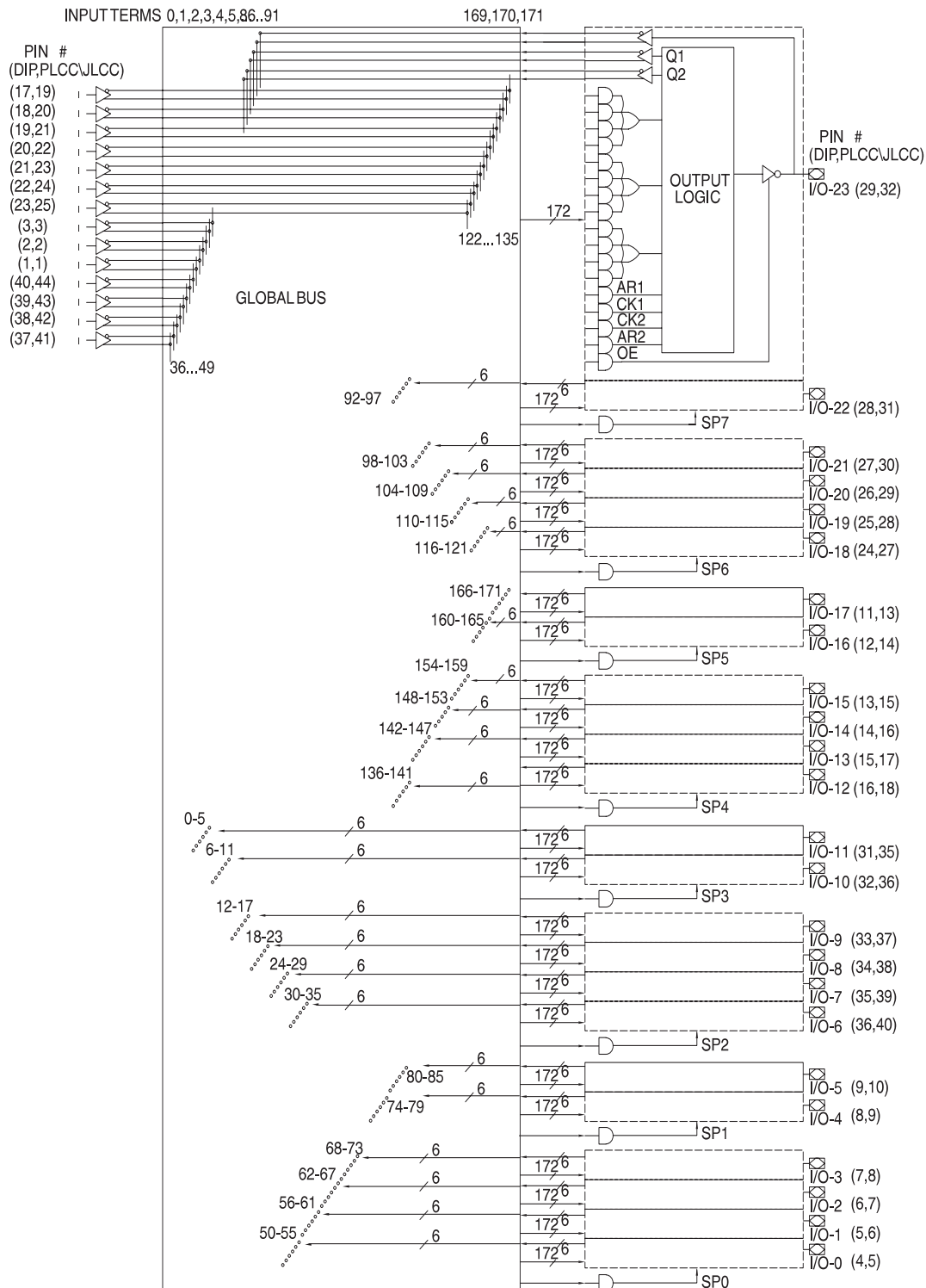
The ATF2500Cs are straightforward and uniform PLDs. The 24 macrocells are numbered 0 through 23. Each macrocell contains 17 AND gates. All AND gates have 172 inputs. The five lower product terms provide AR1, CK1, CK2, AR2, and OE. These are: one asynchronous reset and clock per flip-flop, and an output enable. The top 12 product terms are grouped into three sum terms, which are used as shown in the macrocell diagrams.

Eight synchronous preset terms are distributed in a 2/4 pattern. The first four macrocells share Preset 0, the next two share Preset 1, and so on, ending with the last two macrocells sharing Preset 7.

The 14 dedicated inputs and their complements use the numbered positions in the global bus as shown. Each macrocell provides six inputs to the global bus: (left to right) feedback F2⁽¹⁾ true and false, flip-flop Q1 true and false, and the pin true and false. The positions occupied by these signals in the global bus are the six numbers in the bus diagram next to each macrocell.

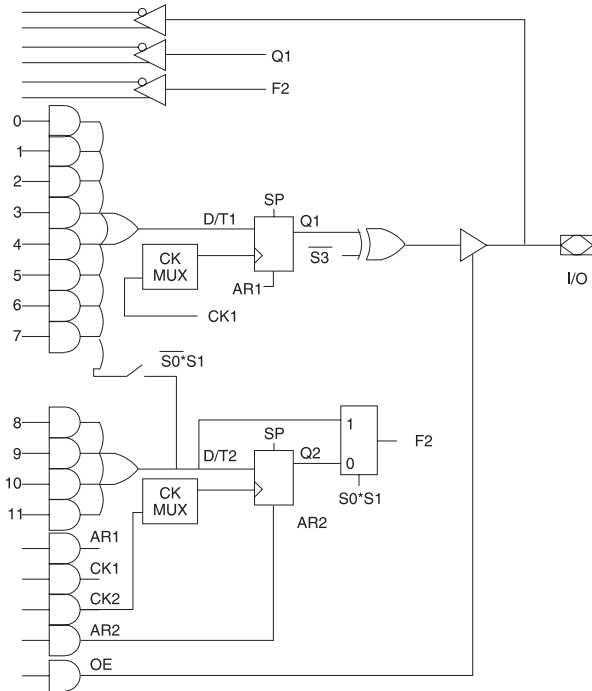
Note: 1. Either the flip-flop input (D/T2) or output (Q2) may be fed back in the ATF2500Cs.

9.1 Functional Logic Diagram ATF2500C



- Notes:
1. Pin 4 and Pin 26 are "ground" connections and are not required for PLCC, LCC and JLCC versions of ATF2500C, making them compatible with ATV2500H, ATV2500B and ATV2500BQ pinouts.
 2. For DIP package, VCC = P10 and GND = P30. For, PLCC, LCC and JLCC packages, VCC = P11 and P12, GND = P33 and P34, and GND = P4, P26 (See Note 1, above).

9.2 Output Logic, Registered⁽¹⁾



S2 = 0		Terms in		Output Configuration
S1	S0	D/T1	D/T2	
0	0	8	4	Registered (Q1); Q2 FB
1	0	12	4 ⁽¹⁾	Registered (Q1); Q2 FB
1	1	8	4	Registered (Q1); D/T2 FB

S3	Output Configuration
0	Active Low
1	Active High

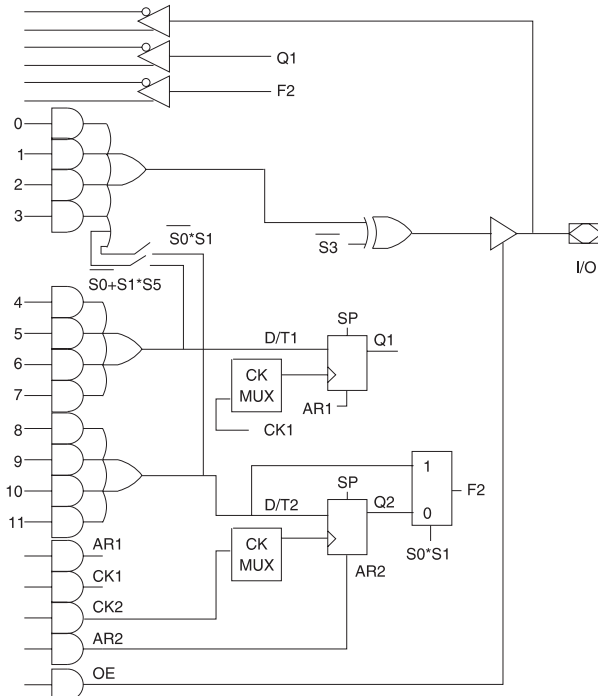
S6	Q1 CLOCK
0	CK1
1	CK1 • PIN1

S4	Register 1 Type
0	D
1	T

S7	Q2 CLOCK
0	CK2
1	CK2 • PIN1

S5	Register 2 Type
0	D
1	T

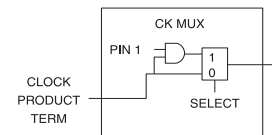
9.3 Output Logic, Combinatorial⁽¹⁾



S2 = 1			Terms in		Output Configuration
S5	S1	S0	D/T1	D/T2	
X	0	0	4 ⁽¹⁾	4	Combinatorial (8 Terms); Q2 FB
X	0	1	4	4	Combinatorial (4 Terms); Q2 FB
X	1	0	4 ⁽¹⁾	4 ⁽¹⁾	Combinatorial (12 Terms); Q2 FB
1	1	1	4 ⁽¹⁾	4	Combinatorial (8 Terms); D/T2 FB
0	1	1	4	4	Combinatorial (4 Terms); D/T2 FB

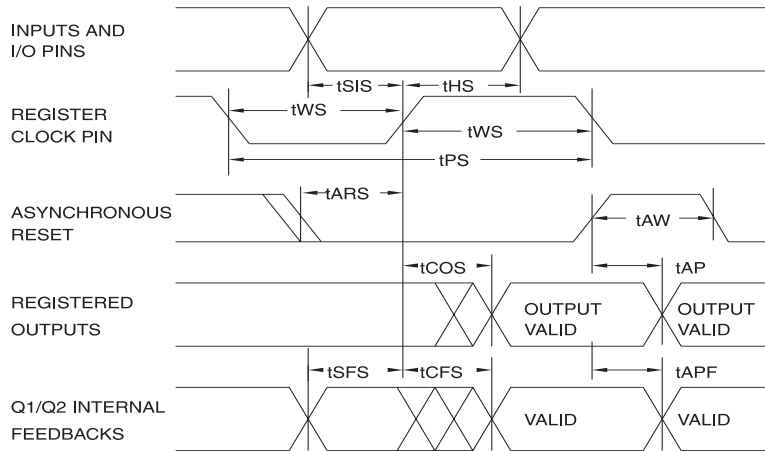
Note: 1. These four terms are shared with D/T1.

Figure 9-1. Clock Option

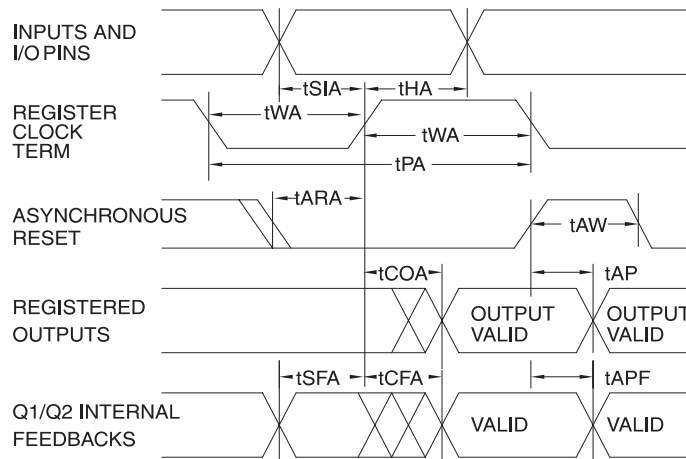


Note: 1. These diagrams show equivalent logic functions, not necessarily the actual circuit implementation.

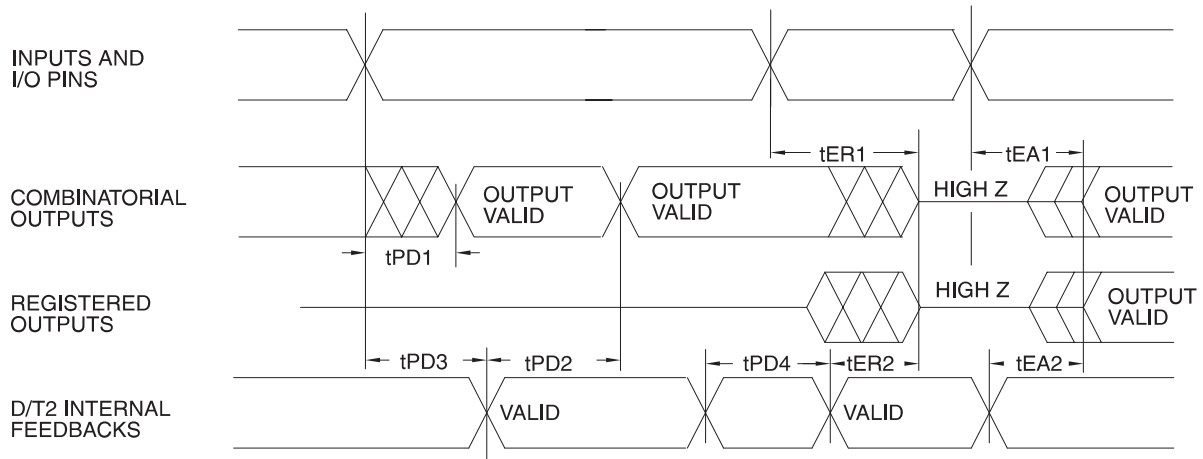
11.2 AC Waveforms⁽¹⁾ Input Pin Clock



11.3 AC Waveforms⁽¹⁾ Product Term Clock



11.4 AC Waveforms⁽¹⁾ Combinatorial Outputs and Feedback



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

11.5 ATF2500C AC Characteristics

Symbol	Parameter	-15		-20		Units
		Min	Max	Min	Max	
t_{PD1}	Input to Non-registered Output		15		20	ns
t_{PD2}	Feedback to Non-registered Output		15		20	ns
t_{PD3}	Input to Non-registered Feedback		11		15	ns
t_{PD4}	Feedback to Non-registered Feedback		11		15	ns
t_{EA1}	Input to Output Enable		15		20	ns
t_{ER1}	Input to Output Disable		15		20	ns
t_{EA2}	Feedback to Output Enable		15		20	ns
t_{ER2}	Feedback to Output Disable		15		20	ns
t_{AW}	Asynchronous Reset Width	8		12		ns
t_{AP}	Asynchronous Reset to Registered Output		18		22	ns
t_{APF}	Asynchronous Reset to Registered Feedback		15		19	ns

11.6 ATF2500C Register AC Characteristics, Input Pin Clock

Symbol	Parameter	-15		-20		Units
		Min	Max	Min	Max	
t_{COS}	Clock to Output		10		11	ns
t_{CFS}	Clock to Feedback	0	5	0	6	ns
t_{SIS}	Input Setup Time	9		14		ns
t_{SFS}	Feedback Setup Time	9		14		ns
t_{HS}	Hold Time	0		0		ns
t_{WS}	Clock Width	6		7		ns
t_{PS}	Clock Period	12		14		ns
F_{MAXS}	External Feedback $1/(t_{SIS} + t_{COS})$		52		40	MHz
	Internal Feedback $1/(t_{SFS} + t_{CFS})$		71		50	MHz
	No Feedback $1/(t_{PS})$		83		71	MHz
t_{ARS}	Asynchronous Reset/Preset Recovery Time	12		15		ns

11.7 ATF2500C Register AC Characteristics, Product Term Clock

Symbol	Parameter	-15		-20		Units
		Min	Max	Min	Max	
t_{COA}	Clock to Output		15		20	ns
t_{CFA}	Clock to Feedback	5	12	10	16	ns
t_{SIA}	Input Setup Time	5		10		ns
t_{SFA}	Feedback Setup Time	5		8		ns
t_{HA}	Hold Time	5		10		ns
t_{WA}	Clock Width	7.5		11		ns
t_{PA}	Clock Period	15		22		ns
F_{MAXA}	External Feedback $1/(t_{SIA} + t_{COA})$		50		33	MHz
	Internal Feedback $1/(t_{SFA} + t_{CFA})$		58		38	MHz
	No Feedback $1/(t_{PS})$		66		45	MHz
t_{ARA}	Asynchronous Reset/Preset Recovery Time	8		12		ns

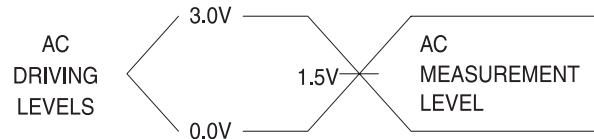
11.8 Pin Capacitance

$f = 1 \text{ MHz}$, $T = 25^\circ\text{C}^{(1)}$

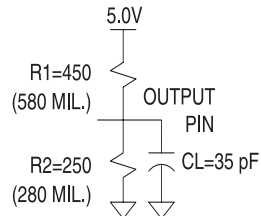
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	$V_{IN} = 0V$
C_{OUT}	8	12	pF	$V_{OUT} = 0V$

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

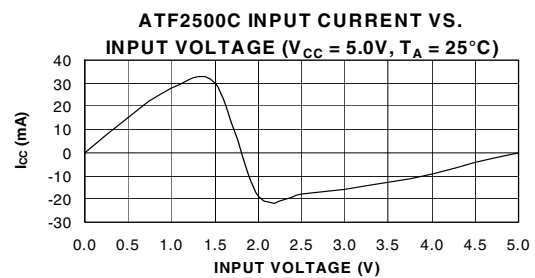
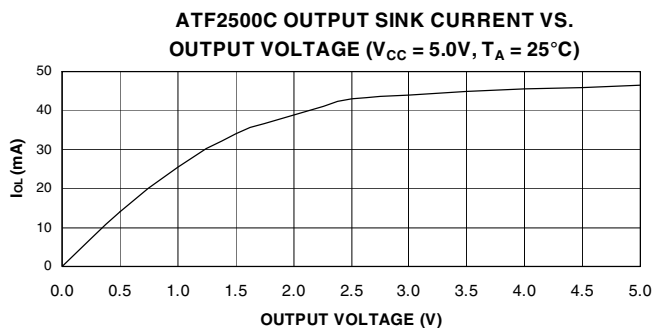
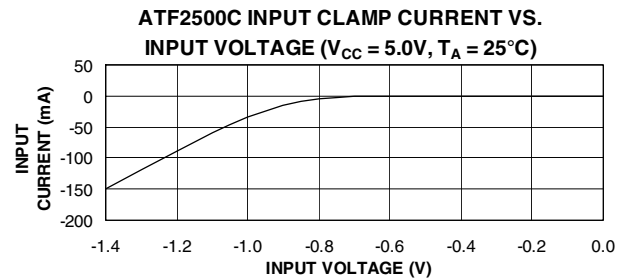
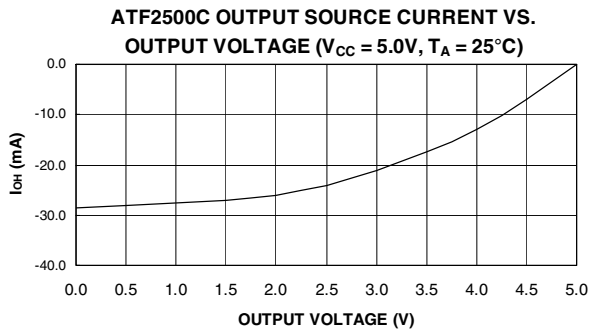
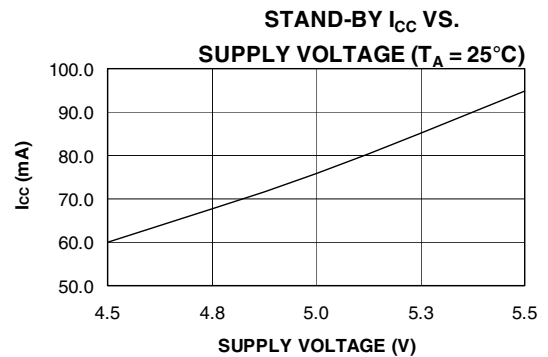
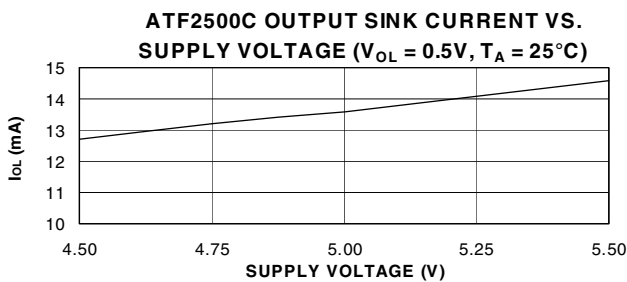
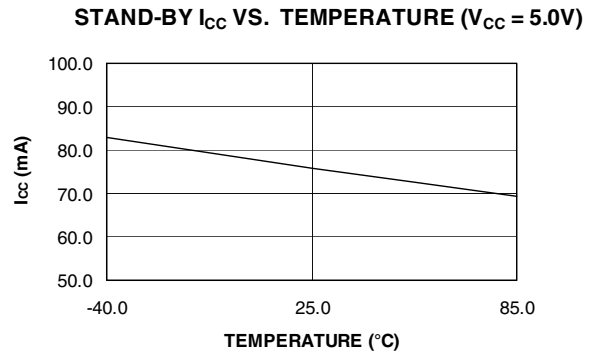
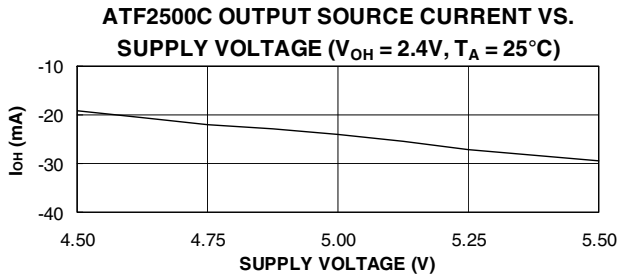
11.9 Test Waveforms and Measurement Levels

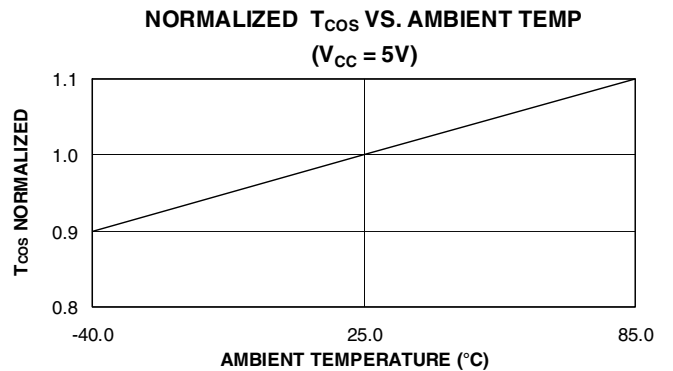
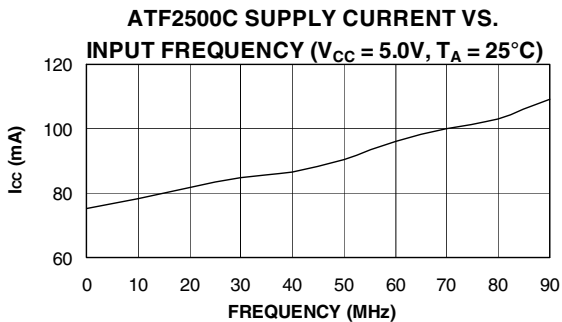
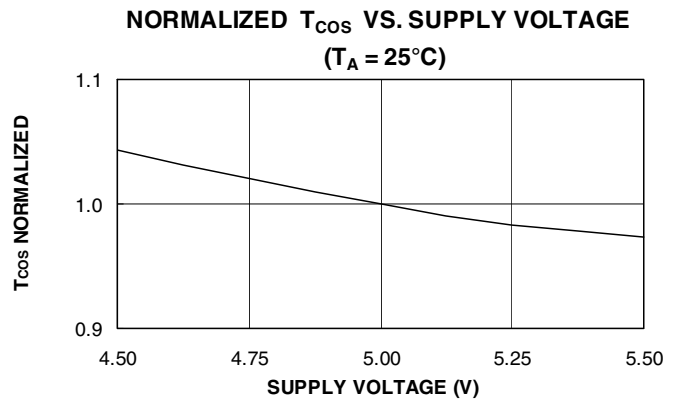
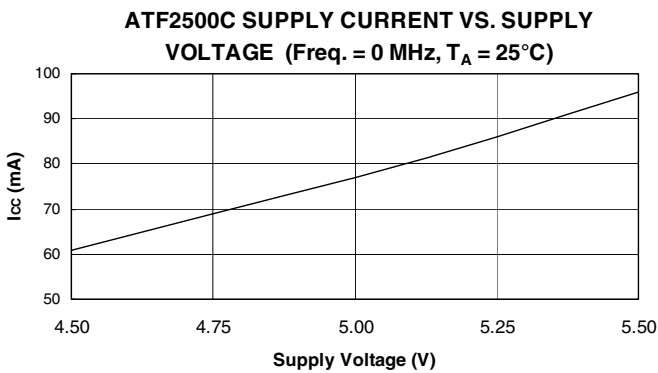
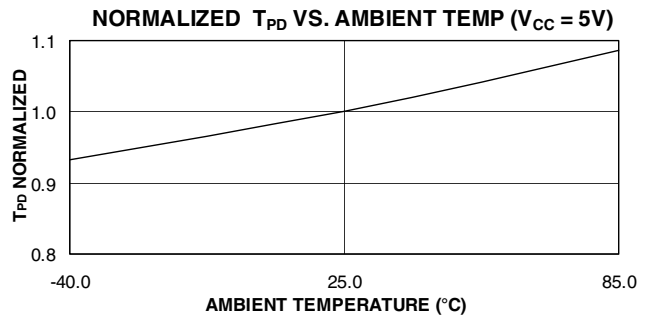
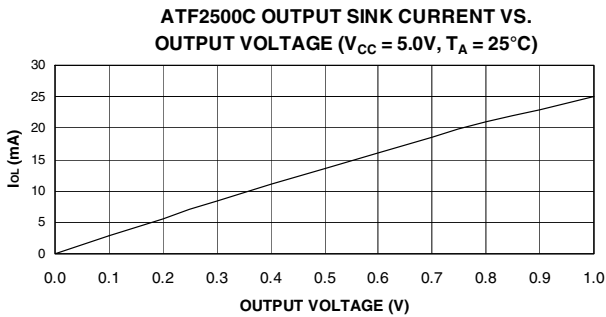
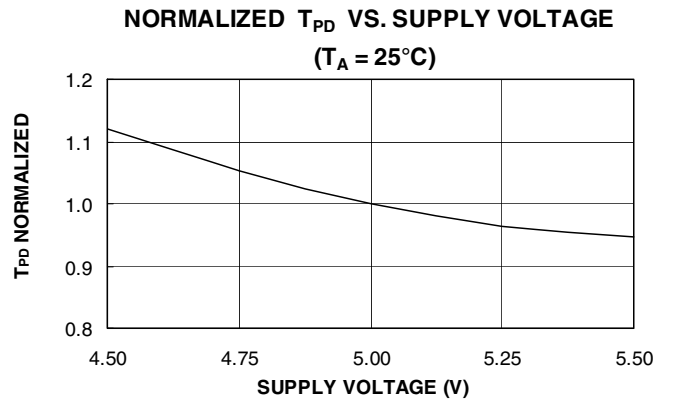
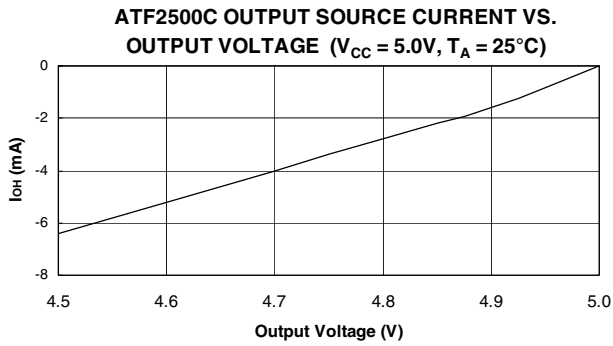


11.10 Output Test Load

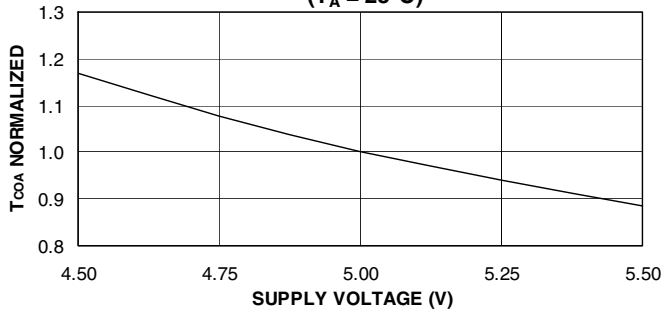


12. ATF2500C Characterization Data

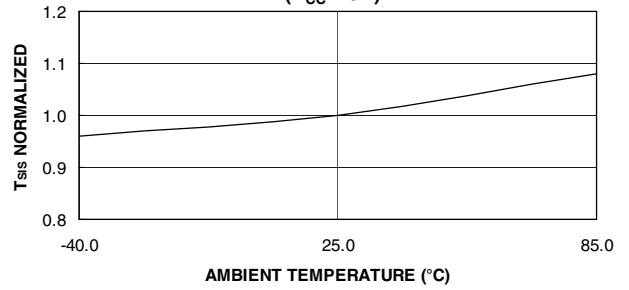




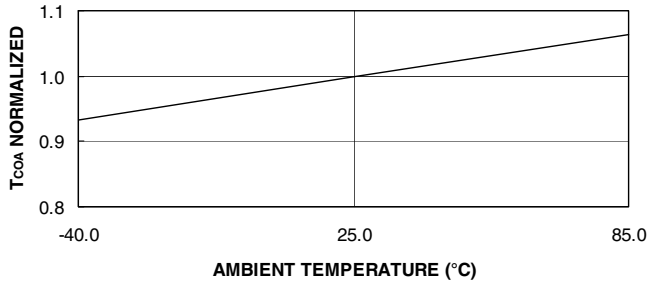
NORMALIZED T_{COA} VS. SUPPLY VOLTAGE
($T_A = 25^\circ\text{C}$)



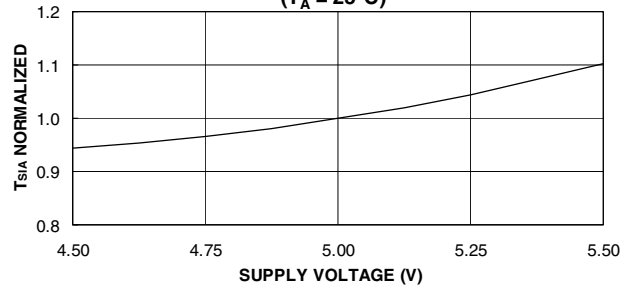
NORMALIZED T_{SIS} VS. AMBIENT TEMP
($V_{CC} = 5\text{V}$)



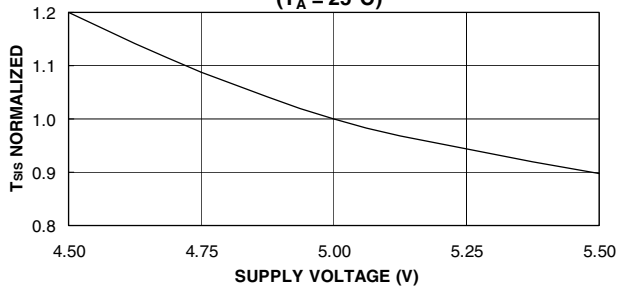
NORMALIZED T_{COA} VS. AMBIENT TEMP
($V_{CC} = 5\text{V}$)



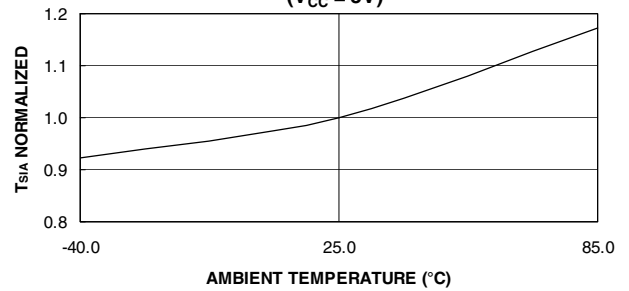
NORMALIZED T_{SIA} VS. SUPPLY VOLTAGE
($T_A = 25^\circ\text{C}$)



NORMALIZED T_{SIS} VS. SUPPLY VOLTAGE
($T_A = 25^\circ\text{C}$)



NORMALIZED T_{SIA} VS. AMBIENT TEMP
($V_{CC} = 5\text{V}$)



13. Ordering Information

13.1 Standard Package Options

t_{PD} (ns)	t_{COS} (ns)	Ext. f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
15	10	52	ATF2500C-15JC	44J	Commercial (0° C to 70° C)
			ATF2500C-15JI	44J	Industrial (-40° C to 85° C)
20	11	40	ATF2500C-20JC	44J	Commercial (0° C to 70° C)
			ATF2500C-20PC	40P6	
			ATF2500C-20JI ATF2500C-20PI	44J 40P6	Industrial (-40° C to 85° C)

13.2 Military Temperature Grade Standard Package Options

t_{PD} (ns)	t_{COS} (ns)	Ext. f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
20	11	40	ATF2500C-20KM	44K	Military (-55° C to 125° C)
			ATF2500C-20GM	40D6	

13.3 Green Package Options (Pb/Halide-free/RoHS Compliant)

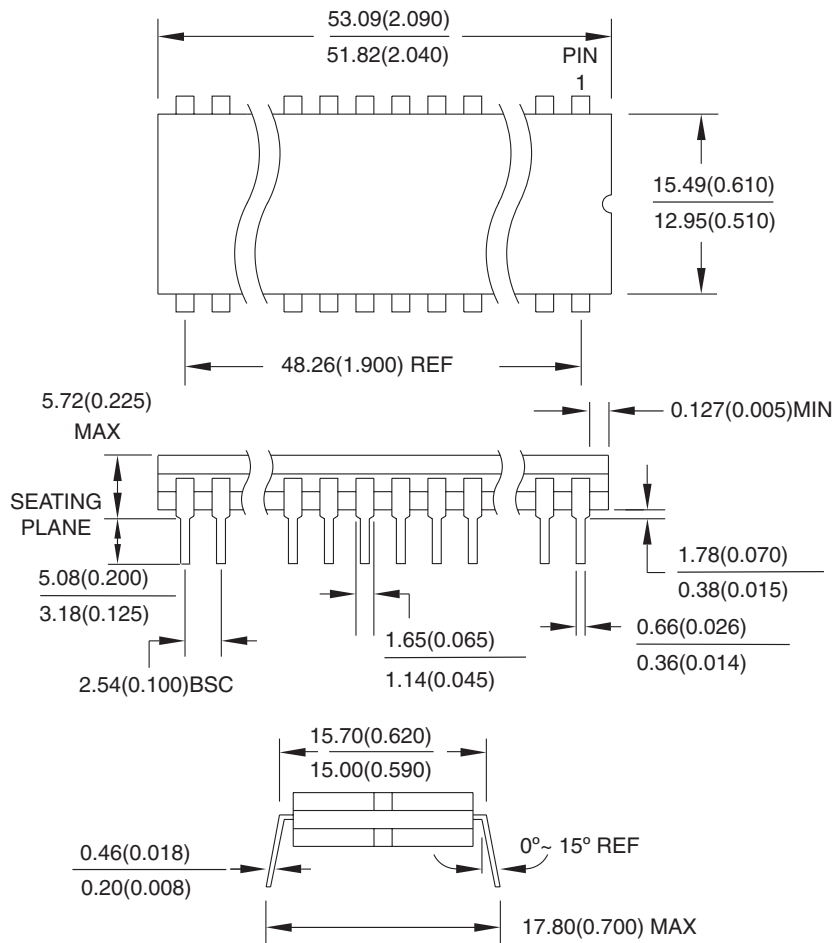
t_{PD} (ns)	t_{COS} (ns)	Ext. f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
15	10	52	ATF2500C-15JU	44J	Industrial (-40° C to 85° C)
20	11	40	ATF2500C-20PU	40P6	

Package Type	
40D6	40-lead, Non-windowed, Ceramic Dual Inline Package (Cer DIP)
40P6	40-pin, 0.600" Wide, Plastic, Dual Inline Package (PDIP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
44K	44-lead, Non-windowed, Ceramic J-leaded Chip Carrier (JLCC)

14. Packaging Information

14.1 40D6 – DIP (CerDIP)

Dimensions in Millimeters and (Inches).
 Controlling dimension: Inches.
 MIL-STD 1835 D-5 Config A (Glass Sealed)



10/23/03



2325 Orchard Parkway
 San Jose, CA 95131

TITLE

40D6, 40-lead, 0.600" Wide, Non-windowed,
 Ceramic Dual Inline Package (CerDip)

DRAWING NO.

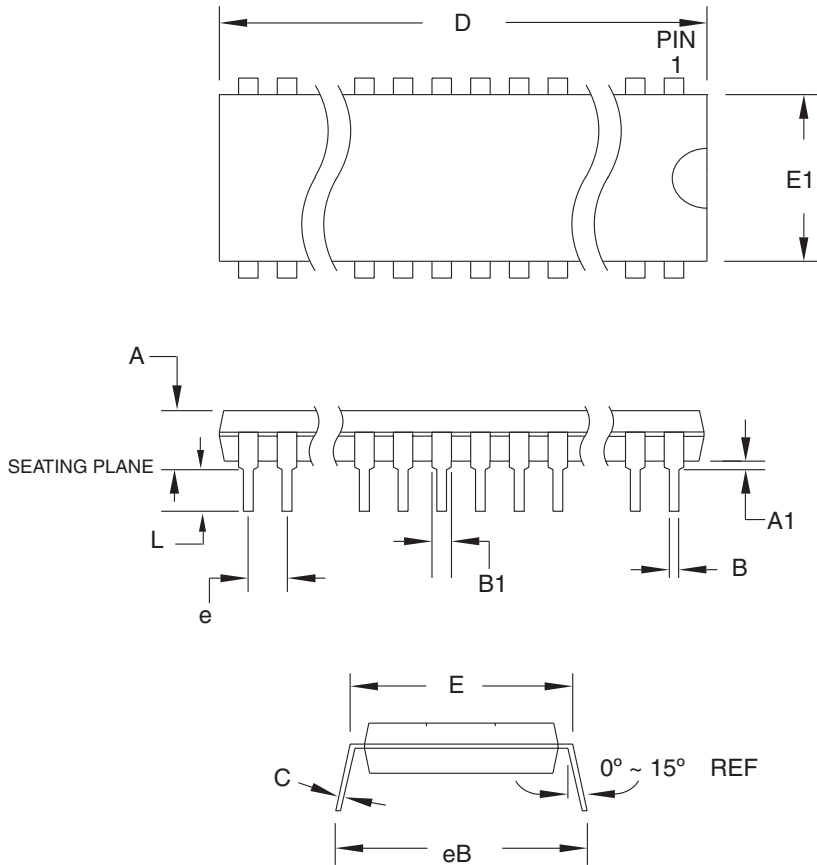
40D6

REV.

B



14.2 40P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
 2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

40P6, 40-lead (0.600"/15.24 mm Wide) Plastic Dual
Inline Package (PDIP)

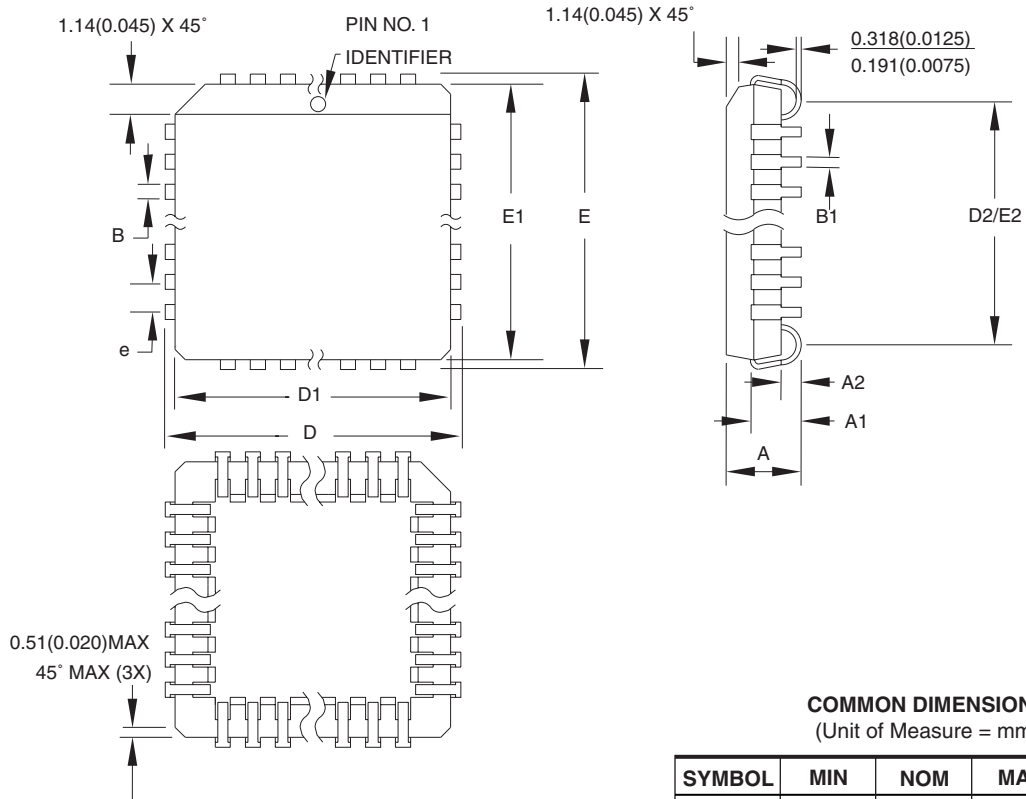
DRAWING NO.

40P6

REV.

B

14.3 44J – PLCC



- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)

DRAWING NO.

44J

REV.

B



Revision Level – Release Date	History
J – May 2005	Added fully Green and Military temperatures packages in Section 13. "Ordering Information" on page 18.
K – Jan. 2008	Added 40-pin CerDIP Package Option.



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