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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21226kfp-u1

1. Overview

This MCU is built using the high-performance silicon gate CMOS process using the R8C CPU core and is packaged in a 48-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1 Mbyte of address space, it is capable of executing instructions at high speed. This MCU is equipped with one CAN module and suited to in-vehicle or FA networking.

Furthermore, the data flash (1 KB x 2 blocks) is embedded in the R8C/23 Group.

The difference between R8C/22 and R8C/23 Groups is only the existence of the data flash. Their peripheral functions are the same.

1.1 Applications

Automotive, etc.

Table 1.4 Product Information for R8C/23 Group

Current of Aug. 2008

Type No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data Flash				
R5F21236DFP	32 Kbytes	1 Kbyte X 2	2 Kbytes	PLQP0048KB-A	D version	Flash memory version
R5F21237DFP	48 Kbytes	1 Kbyte X 2	2.5 Kbytes	PLQP0048KB-A		
R5F21238DFP	64 Kbytes	1 Kbyte X 2	3 Kbytes	PLQP0048KB-A		
R5F21236JFP	32 Kbytes	1 Kbyte X 2	2 Kbytes	PLQP0048KB-A	J version	
R5F21237JFP	48 Kbytes	1 Kbyte X 2	2.5 Kbytes	PLQP0048KB-A		
R5F21238JFP	64 Kbytes	1 Kbyte X 2	3 Kbytes	PLQP0048KB-A		
R5F2123AJFP	96 Kbytes	1 Kbyte X 2	5 Kbytes	PLQP0048KB-A		
R5F2123CJFP	128 Kbytes ⁽¹⁾	1 Kbyte X 2	6 Kbytes	PLQP0048KB-A	K version	
R5F21236KFP	32 Kbytes	1 Kbyte X 2	2 Kbytes	PLQP0048KB-A		
R5F21237KFP	48 Kbytes	1 Kbyte X 2	2.5 Kbytes	PLQP0048KB-A		
R5F21238KFP	64 Kbytes	1 Kbyte X 2	3 Kbytes	PLQP0048KB-A		
R5F2123AKFP	96 Kbytes	1 Kbyte X 2	5 Kbytes	PLQP0048KB-A		
R5F2123CKFP	128 Kbytes ⁽¹⁾	1 Kbyte X 2	6 Kbytes	PLQP0048KB-A		

NOTE:

1. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **24. Notes on Emulator Debugger** of Hardware Manual.

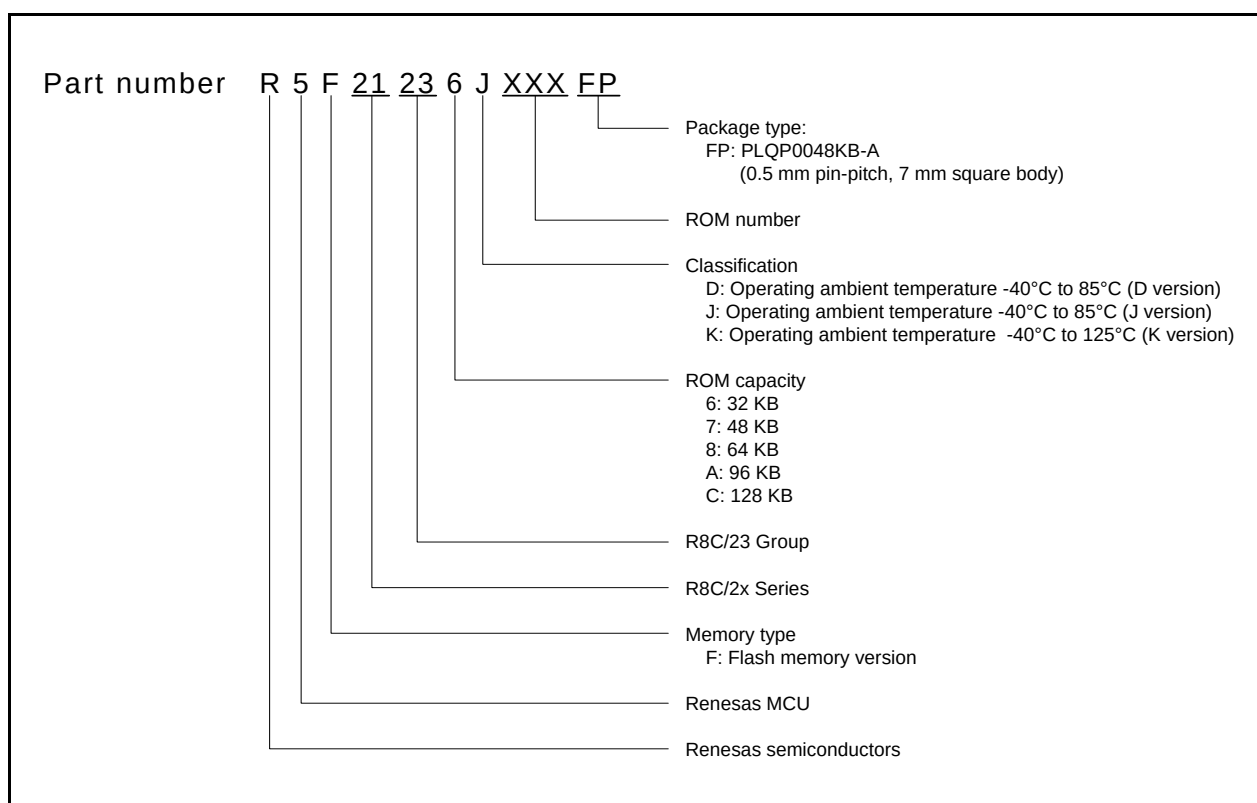


Figure 1.3 Type Number, Memory Size, and Package of R8C/23 Group

1.5 Pin Assignments

Figure 1.4 shows Pin Assignments (Top View).

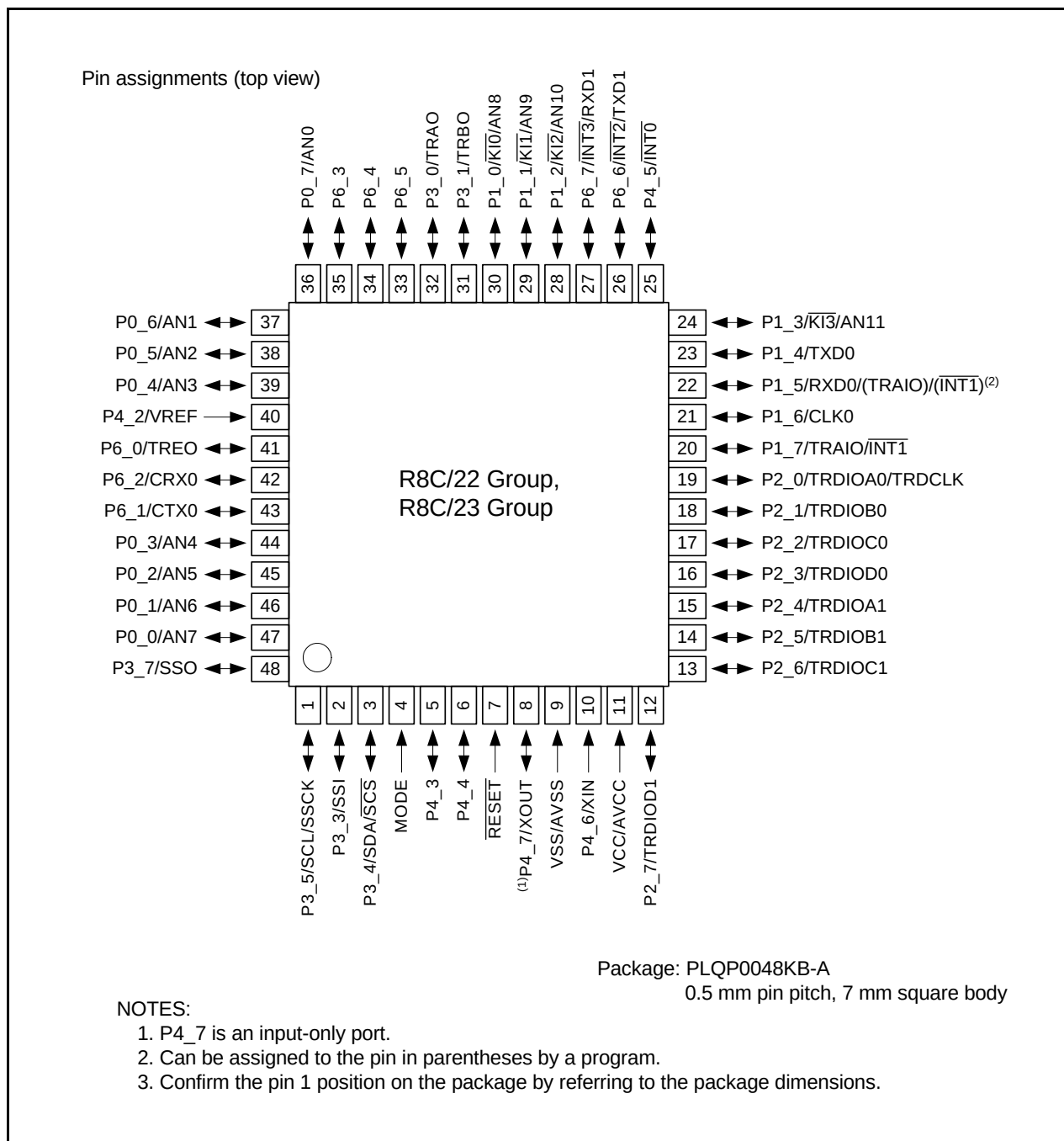


Figure 1.4 Pin Assignments (Top View)

1.6 Pin Functions

Table 1.5 lists the Pin Functions and Table 1.6 lists the Pin Name Information by Pin Number.

Table 1.5 Pin Functions

Type	Symbol	I/O Type	Description
Power Supply Input	VCC VSS	I	Apply 2.7 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog Power Supply Input	AVCC, AVSS	I	Applies the power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset Input	RESET	I	Input "L" on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN Clock Input	XIN	I	These pins are provided for the XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
XIN Clock Output	XOUT	O	
INT Interrupt Input	INT0 to INT3	I	INT interrupt input pins. INT0 Timer RD input pins. INT1 Timer RA input pins.
Key Input Interrupt	KI0 to KI3	I	Key input interrupt input pins.
Timer RA	TRAIO	I/O	Timer RA I/O pin.
	TRA0	O	Timer RA output pin.
Timer RB	TRBO	O	Timer RB output pin.
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDI0C0, TRDI0C1, TRDI0D0, TRDI0D1	I/O	Timer RD I/O ports.
	TRDCLK	I	External clock input pin.
Timer RE	TRE0	O	Divided clock output pin.
Serial Interface	CLK0	I/O	Transfer clock I/O pin.
	RXD0, RXD1	I	Serial data input pins.
	TXD0, TXD1	O	Serial data output pins.
I ² C Bus Interface	SCL	I/O	Clock I/O pin.
	SDA	I/O	Data I/O pin.
Clock Synchronous Serial I/O with Chip Select	SSI	I/O	Data I/O pin.
	SCS	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
CAN Module	CRX0	I	CAN data input pin.
	CTX0	O	CAN data output pin.
Reference Voltage Input	VREF	I	Reference voltage input pin to A/D converter.
A/D Converter	AN0 to AN11	I	Analog input pins to A/D converter.
I/O Port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5, P6_0 to P6_7	I/O	CMOS I/O ports. Each port contains an input/output select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by a program.
Input Port	P4_2, P4_6, P4_7	I	Input only ports.

I: Input O: Output I/O: Input and output

Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules						
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I ² C Bus Interface	CAN Module	A/D Converter
1		P3_5				SSCK	SCL		
2		P3_3				SSI			
3		P3_4				SCS	SDA		
4	MODE								
5		P4_3							
6		P4_4							
7	RESET								
8	XOUT	P4_7							
9	VSS/AVSS								
10	XIN	P4_6							
11	VCC/AVCC								
12		P2_7		TRDIOD1					
13		P2_6		TRDIOD1					
14		P2_5		TRDIOD1					
15		P2_4		TRDIOD1					
16		P2_3		TRDIOD0					
17		P2_2		TRDIOD0					
18		P2_1		TRDIOD0					
19		P2_0		TRDIOD0/TRDCLK					
20		P1_7	INT1	TRAIO					
21		P1_6			CLK0				
22		P1_5	(INT1) ⁽¹⁾	(TRAIO) ⁽¹⁾	RXD0				
23		P1_4			TXD0				
24		P1_3	KI3						AN11
25		P4_5	INT0	INT0					
26		P6_6	INT2		TXD1				
27		P6_7	INT3		RXD1				
28		P1_2	KI2						AN10
29		P1_1	KI1						AN9
30		P1_0	KI0						AN8
31		P3_1		TRBO					
32		P3_0		TRAIO					
33		P6_5							
34		P6_4							
35		P6_3							
36		P0_7							AN0
37		P0_6							AN1
38		P0_5							AN2
39		P0_4							AN3
40	VREF	P4_2							
41		P6_0		TREO					
42		P6_2						CRX0	
43		P6_1						CTX0	
44		P0_3							AN4
45		P0_2							AN5
46		P0_1							AN6
47		P0_0							AN7
48		P3_7				SSO			

NOTE:

1. Can be assigned to the pin in parentheses by a program.

2.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

An interrupt is disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function.

Table 4.1 to Table 4.13 list the SFR Information.

Table 4.1 SFR Information (1)(1)

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protect Mode Register	CSPR	00h 10000000b ⁽⁸⁾
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0030h			
0031h	Voltage Detection Register 1 ⁽²⁾	VCA1	00001000b
0032h	Voltage Detection Register 2 ⁽⁶⁾	VCA2	00h ⁽³⁾ 01000000b ⁽⁴⁾
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register ⁽⁷⁾	VW1C	0000X000b ⁽³⁾ 0100X001b ⁽⁴⁾
0037h	Voltage Monitor 2 Circuit Control Register ⁽⁵⁾	VW2C	00h
0038h			
0039h			
003Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1.
4. Power-on reset, voltage monitor 1 reset or the LVD0ON bit in the OFS register is set to 0.
5. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect b2 and b3.
6. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect b7.
7. Software reset, the watchdog timer reset, and the voltage monitor 2 reset do not affect other than the b0 and b6.
8. The CSPROINI bit in the OFS register is 0.

Table 4.6 SFR Information (6)⁽¹⁾

Address	Register	Symbol	After reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIOA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIOA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.9 SFR Information (9)⁽¹⁾

Address	Register	Symbol	After reset
1340h			
1341h			
1342h	CAN0 Acceptance Filter Support Register	C0AFS	XXh
1343h			XXh
1344h			
1345h			
1346h			
1347h			
1348h			
1349h			
134Ah			
134Bh			
134Ch			
134Dh			
134Eh			
134Fh			
1350h			
1351h			
1352h			
1353h			
1354h			
1355h			
1356h			
1357h			
1358h			
1359h			
135Ah			
135Bh			
135Ch			
135Dh			
135Eh			
135Fh	CAN0 Clock Select Register	CCLKR	00h
1360h	CAN0 Slot 0: Identifier/DLC		XXh
1361h			XXh
1362h			XXh
1363h			XXh
1364h			XXh
1365h			XXh
1366h	CAN0 Slot 0: Data Field		XXh
1367h			XXh
1368h			XXh
1369h			XXh
136Ah			XXh
136Bh			XXh
136Ch			XXh
136Dh			XXh
136Eh	CAN0 Slot 0: Time Stamp		XXh
136Fh			XXh
1370h	CAN0 Slot 1: Identifier/DLC		XXh
1371h			XXh
1372h			XXh
1373h			XXh
1374h			XXh
1375h			XXh
1376h	CAN0 Slot 1: Data Field		XXh
1377h			XXh
1378h			XXh
1379h			XXh
137Ah			XXh
137Bh			XXh
137Ch			XXh
137Dh			XXh
137Eh	CAN0 Slot 1: Time Stamp		XXh
137Fh			XXh

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.11 SFR Information (11)⁽¹⁾

Address	Register	Symbol	After reset
13C0h	CAN0 Slot 6: Identifier/DLC		XXh
13C1h			XXh
13C2h			XXh
13C3h			XXh
13C4h			XXh
13C5h			XXh
13C6h	CAN0 Slot 6: Data Field		XXh
13C7h			XXh
13C8h			XXh
13C9h			XXh
13CAh			XXh
13CBh			XXh
13CCh			XXh
13CDh			XXh
13CEh	CAN0 Slot 6: Time Stamp		XXh
13CFh			XXh
13D0h	CAN0 Slot 7: Identifier/DLC		XXh
13D1h			XXh
13D2h			XXh
13D3h			XXh
13D4h			XXh
13D5h			XXh
13D6h	CAN0 Slot 7: Data Field		XXh
13D7h			XXh
13D8h			XXh
13D9h			XXh
13DAh			XXh
13DBh			XXh
13DCh			XXh
13DDh			XXh
13DEh	CAN0 Slot 7: Time Stamp		XXh
13DFh			XXh
13E0h	CAN0 Slot 8: Identifier/DLC		XXh
13E1h			XXh
13E2h			XXh
13E3h			XXh
13E4h			XXh
13E5h			XXh
13E6h	CAN0 Slot 8: Data Field		XXh
13E7h			XXh
13E8h			XXh
13E9h			XXh
13EAh			XXh
13EBh			XXh
13ECh			XXh
13EDh			XXh
13EEh	CAN0 Slot 8: Time Stamp		XXh
13EFh			XXh
13F0h	CAN0 Slot 9: Identifier/DLC		XXh
13F1h			XXh
13F2h			XXh
13F3h			XXh
13F4h			XXh
13F5h			XXh
13F6h	CAN0 Slot 9: Data Field		XXh
13F7h			XXh
13F8h			XXh
13F9h			XXh
13FAh			XXh
13FBh			XXh
13FCh			XXh
13FDh			XXh
13FEh	CAN0 Slot 9: Time Stamp		XXh
13FFh			XXh

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance ⁽²⁾	R8C/22 Group	100 ⁽³⁾	–	–	times
		R8C/23 Group	1,000 ⁽³⁾	–	–	times
–	Byte program time		–	50	400	μs
–	Block erase time		–	0.4	9	s
t _d (SR-SUS)	Time delay from suspend request until erase suspend		–	–	97 + CPU clock × 6 cycle	μs
–	Interval from erase start/restart until following suspend request		650	–	–	μs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3 + CPU clock × 4 cycle	μs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	–	–	year

NOTES:

1. V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 100 or 1,000), each block can be erased n times.
For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure endurance can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

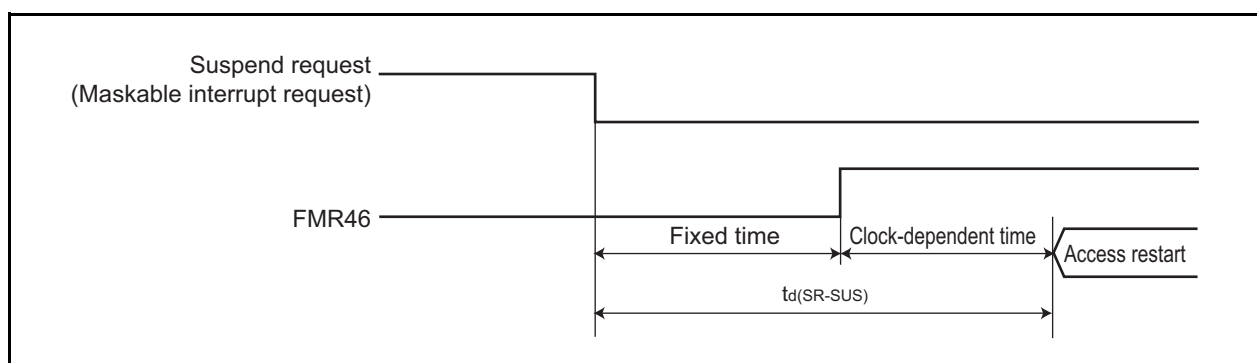


Figure 5.2 Time delay until Suspend

Table 5.6 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet1	Voltage detection level ^(3, 4)		2.70	2.85	3.00	V
td(Vdet1-A)	Voltage monitor 1 reset generation time ⁽⁵⁾		–	40	200	μs
–	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	–	0.6	–	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽²⁾		–	–	100	μs
Vccmin	MCU operating voltage minimum value		2.70	–	–	V

NOTES:

1. The measurement condition is Vcc = 2.7 V to 5.5 V and Topr = -40°C to 85°C (D, J version) / -40°C to 125°C (K version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
3. Hold Vdet2 > Vdet1.
4. This parameter shows the voltage detection level when the power supply drops. The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.
5. Time until the voltage monitor 1 reset is generated after the voltage passes Vdet1 when Vcc falls. When using the digital filter, its sampling time is added to td(Vdet1-A). When using the voltage monitor 1 reset, maintain this time until Vcc = 2.0 V after the voltage passes Vdet1 when the power supply falls.

Table 5.7 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet2	Voltage detection level ⁽⁴⁾		3.3	3.6	3.9	V
td(Vdet2-A)	Voltage monitor 2 reset/interrupt request generation time ^(2, 5)		–	40	200	μs
–	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0V	–	0.6	–	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		–	–	100	μs

NOTES:

1. The measurement condition is Vcc = 2.7 V to 5.5 V and Topr = -40°C to 85°C (D, J version) / -40°C to 125°C (K version).
2. Time until the voltage monitor 2 reset/interrupt request is generated since the voltage passes Vdet2.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.
4. Hold Vdet2 > Vdet1.
5. When using the digital filter, its sampling time is added to td(Vdet2-A). When using the voltage monitor 2 reset, maintain this time until Vcc = 2.0 V after the voltage passes Vdet2 when the power supply falls.

Table 5.12 Timing Requirements of Clock Synchronous Serial I/O with Chip Select⁽¹⁾

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	–	–	tcyc ⁽²⁾
t _{HI}	SSCK clock "H" width			0.4	–	0.6	tsucyc
t _{LO}	SSCK clock "L" width			0.4	–	0.6	tsucyc
trise	SSCK clock rising time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tfall	SSCK clock falling time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tsu	SSO, SSI data input setup time			100	–	–	ns
t _H	SSO, SSI data input hold time			1	–	–	tcyc ⁽²⁾
t _{LEAD}	SCS setup time	Slave		1tcyc + 50	–	–	ns
t _{LAG}	SCS hold time	Slave		1tcyc + 50	–	–	ns
t _{OD}	SSO, SSI data output delay time			–	–	1	tcyc ⁽²⁾
t _{SA}	SSI slave access time			–	–	1tcyc + 100	ns
t _{OR}	SSI slave out open time			–	–	1tcyc + 100	ns

NOTES:

1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. 1tcyc = 1/f₁(s)

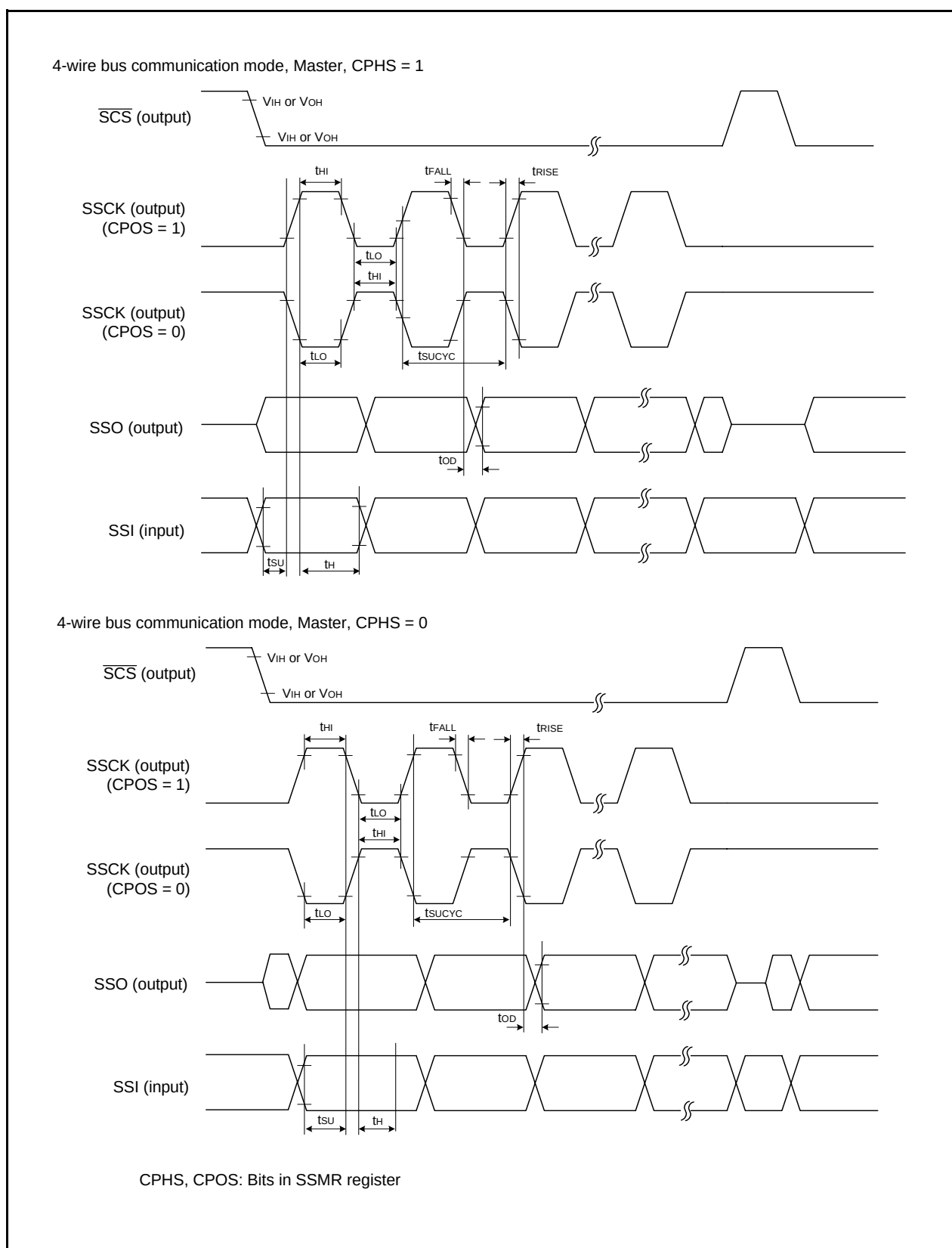


Figure 5.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

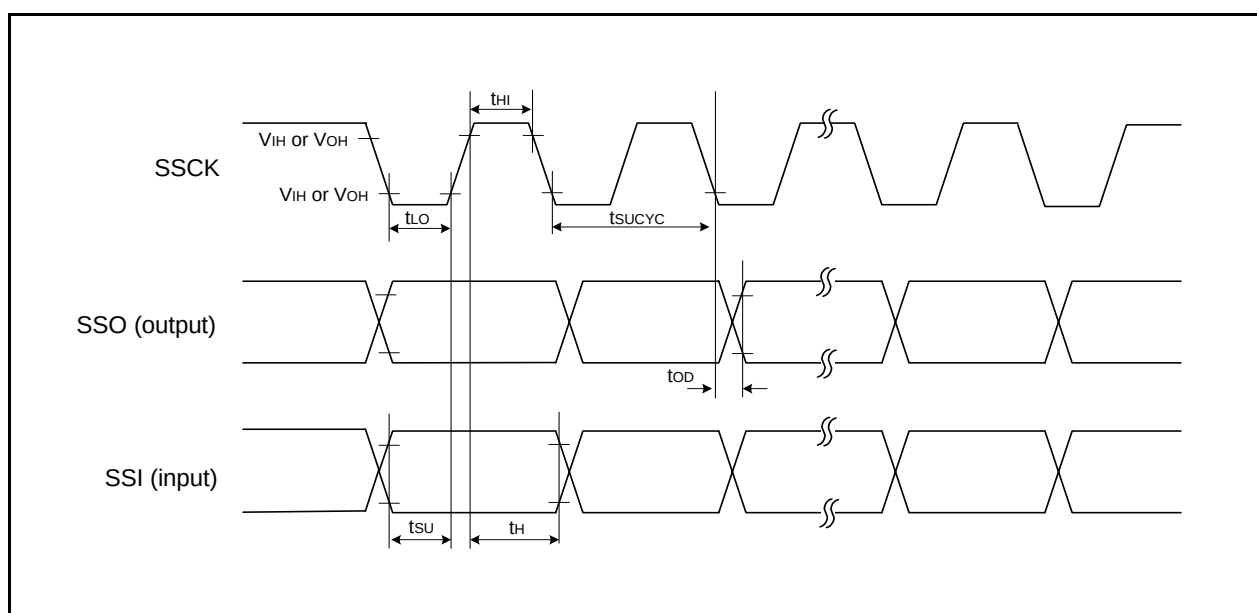


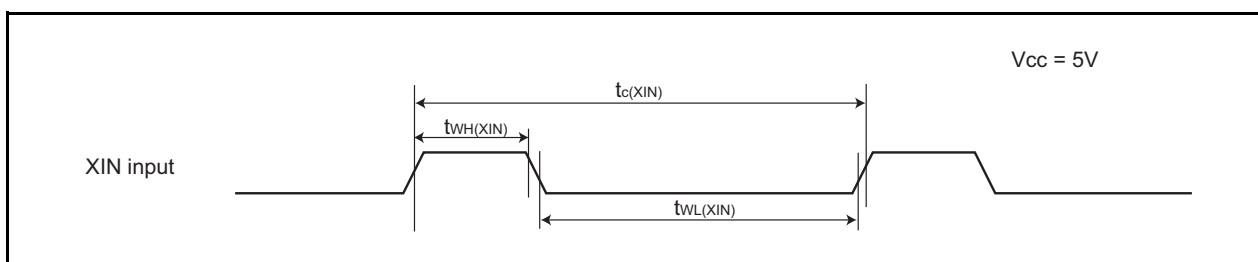
Figure 5.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

**Table 5.15 Electrical Characteristics (2) [V_{CC} = 5 V]
(Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), Unless Otherwise Specified.)**

Symbol	Parameter	Condition	Standard			Unit	
			Min.	Typ.	Max.		
Icc	Power supply current (Vcc = 3.3 to 5.5 V) In single-chip mode, the output pins are open and other pins are Vss	High-clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	12.5	25.0	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	10.0	20.0	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6.5	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	6.5	–	mA
			XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	5.0	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	6.5	13.0	mA
			XIN clock off High-speed on-chip oscillator on fOCO= 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.2	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 FMR47 = 1	–	150	300	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA20 = 0 VCA26 = VCA27 = 0	–	60	120	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA20 = 0 VCA26 = VCA27 = 0	–	38	76	μA
		Stop mode Topr = 25°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	0.8	3.0	μA
		Stop mode Topr = 85°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	1.2	–	μA
		Stop mode Topr = 125°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	4.0	–	μA

Timing Requirements (Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 5\text{ V}$]**Table 5.16 XIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(\text{XIN})$	XIN input cycle time	50	–	ns
$t_{WH}(\text{XIN})$	XIN input "H" width	25	–	ns
$t_{WL}(\text{XIN})$	XIN input "L" width	25	–	ns

**Figure 5.8 XIN Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.17 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(\text{TRAIO})$	TRAIO input cycle time	100	–	ns
$t_{WH}(\text{TRAIO})$	TRAIO input "H" width	40	–	ns
$t_{WL}(\text{TRAIO})$	TRAIO input "L" width	40	–	ns

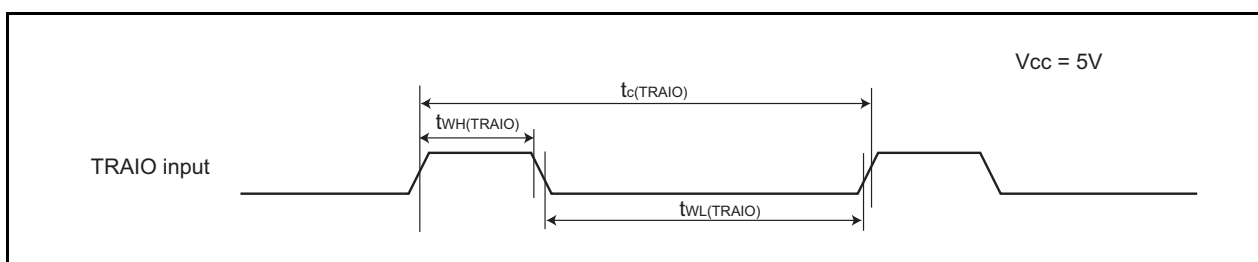
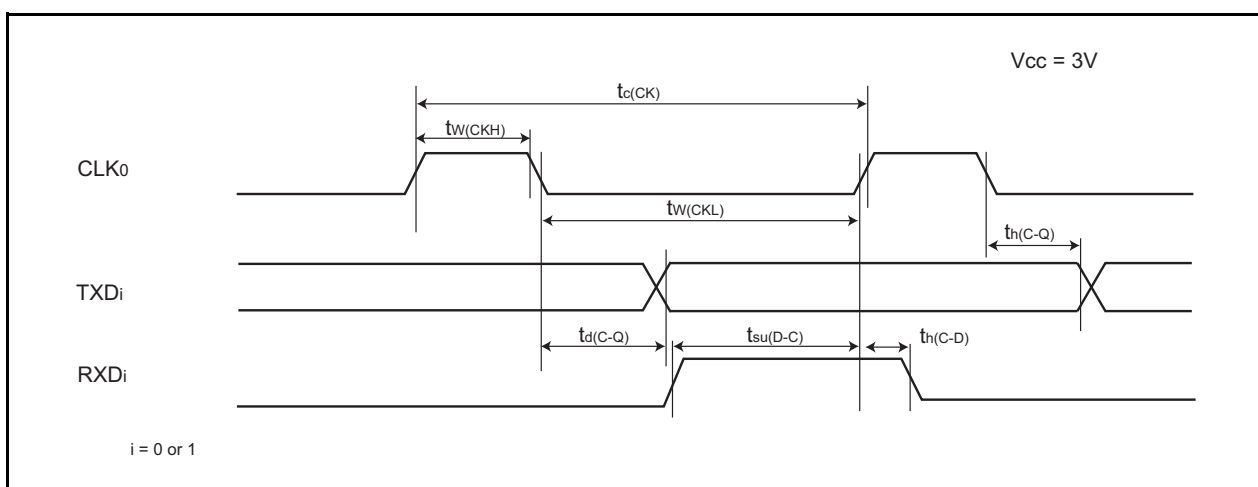
**Figure 5.9 TRAIO Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Table 5.24 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	300	—	ns
$t_{w(CKH)}$	CLK0 input "H" width	150	—	ns
$t_{w(CKL)}$	CLK0 input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

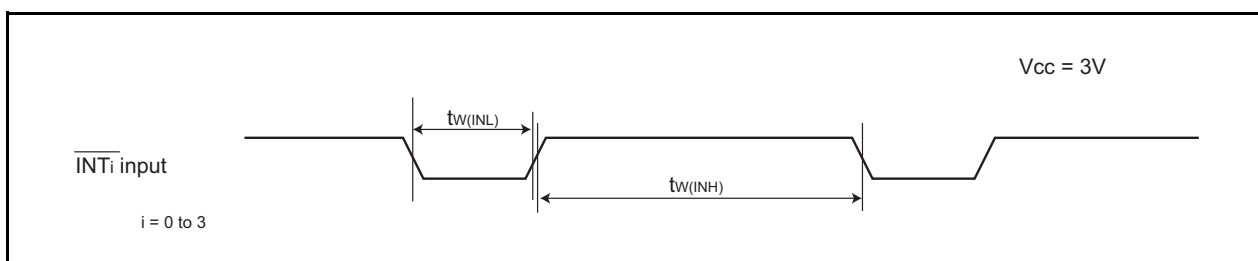
i = 0 or 1

**Figure 5.14 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.25 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width	380 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width	380 ⁽²⁾	—	ns

NOTES:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input HIGH width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input LOW width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.

**Figure 5.15 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 3 V (i = 0 to 3)**

REVISION HISTORY	R8C/22 Group, R8C/23 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
1.00	Oct 27, 2006	40	Table 5.15 Electrical Characteristics (1) [VCC = 5 V] → Table 5.14 Electrical Characteristics (1) [VCC = 5 V] revised. RAM Hold Voltage, Min.; “1.8” → “2.0” corrected.
		41	Table 5.16 Electrical Characteristics (2) [Vcc = 5 V] → Table 5.15 Electrical Characteristics (2) [Vcc = 5 V] revised. Wait mode revised.
		44	Table 5.21 Electrical Characteristics (3) [VCC = 3 V] → Table 5.20 Electrical Characteristics (3) [VCC = 3 V] revised. RAM hold voltage, Min.; “1.8” → “2.0” corrected.
		45	Table 5.22 Electrical Characteristics (4) [Vcc = 3 V] → Table 5.21 Electrical Characteristics (4) [Vcc = 3 V] revised. Wait mode revised.
1.10	Mar 16, 2007	–	D version products added. Relevant descriptions revised because of expanding products - Table 1.1 to 1.4 revised. - Figure 1.2 and 1.3 revised. - Figure 3.1 and 3.2 revised. - Table 5.1 to 5.15 revised. - Table 5.20 and 5.21 revised.
		15	Table 4.1 revised; 000Ah: “00XXX000b” → “00h”, 000Fh: “00011111b” → “00X11111b”
		42	Table 5.17 and Figure 5.9 revised; “INT1 input” deleted
		43	Table 5.19 and Figure 5.11 revised; “i = 0, 2, 3” → “i = 0 to 3”
		46	Table 5.23 and Figure 5.13 revised; “INT1 input” deleted
		47	Table 5.25 and Figure 5.15 revised; “i = 0, 2, 3” → “i = 0 to 3”
2.00	Aug 20, 2008	–	“RENESAS TECHNICAL UPDATE” reflected: TN-16C-A172A/E
		5, 6	Table 1.3, Table 1.4 revised Figure 1.2, Figure 1.3; ROM number “XXX” added
		13, 14	Figure 3.1, Figure 3.2; “Expanding area” deleted
		23	Table 4.9 135Fh Address “XXXX0000b” → “00h”
		28	Table 5.2; NOTE2 revised
		30	Table 5.4; NOTE2 and NOTE4 revised
		31	Table 5.5; NOTE2 and NOTE5 revised
		32	Table 5.6; “td(Vdet1-A)” added, NOTE5 added Table 5.7; “td(Vdet2-A)” and NOTE2 revised, NOTE5 added
		33	Table 5.8; “trth” and NOTE2 revised, Figure 5.3 revised

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