Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21228kfp-u1

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

Table 1.2 Functions and Specifications for R8C/23 Group

Item		Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to **Table 1.4 Product Information for R8C/23 Group**
Peripheral Function	Ports	I/O ports: 41 pins, Input port: 3 pins
	Timers	Timer RA: 8 bits x 1 channel, Timer RB: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer RD: 16 bits x 2 channel (Circuits of input capture and output compare) Timer RE: With compare match function
	Serial interface	1 channel (UART0) Clock synchronous I/O, UART 1 channel (UART1) UART
	Clock synchronous serial interface	1 channel I^2C bus interface(2), Clock synchronous serial I/O with chip select
	LIN module	Hardware LIN: 1 channel (Timer RA, UART0)
	CAN module	1 channel with 2.0B specification: 16 slots
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer	15 bits x 1 channel (with prescaler) Reset start selectable
	Interrupts	Internal: 14 sources, External: 6 sources, Software: 4 sources, Priority level: 7 levels
	Clock generation circuits	2 circuits XIN clock generation circuit (with on-chip feedback resistor) On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has frequency adjustment function.
	Oscillation stop detection function	Stop detection of XIN clock oscillation
	Voltage detection circuit	On-chip
	Power-on reset circuit include	On-chip
Electric Characteristics	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz)(D, J version) VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz)(K version) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)
	Current consumption	Typ. 12.5 mA (VCC = 5 V, f(XIN) = 20 MHz, High-speed on-chip oscillator stopping) Typ. 6.0 mA (VCC = 5 V, f(XIN) = 10 MHz, High-speed on-chip oscillator stopping)
Flash Memory	Programming and erasure voltage	VCC = 2.7 to 5.5 V
	Programming and erasure endurance	10,000 times (data flash)
		1,000 times (program ROM)
Operating Ambient Temperature		-40 to 85°C
		-40 to 125°C (option(1))
Package		48-pin mold-plastic LQFP

NOTES:
1. When using options, be sure to inquire about the specification.
2. I^2C bus is a registered trademark of Koninklijke Philips Electronics N.V.

Table 1.4 Product Information for R8C/23 Group **Current of Aug. 2008**

Type No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data Flash				
R5F21236DFP	32 Kbytes	1 Kbyte X 2	2 Kbytes	PLQP0048KB-A	D version	Flash memory version
R5F21237DFP	48 Kbytes	1 Kbyte X 2	2.5 Kbytes	PLQP0048KB-A		
R5F21238DFP	64 Kbytes	1 Kbyte X 2	3 Kbytes	PLQP0048KB-A		
R5F21236JFP	32 Kbytes	1 Kbyte X 2	2 Kbytes	PLQP0048KB-A	J version	
R5F21237JFP	48 Kbytes	1 Kbyte X 2	2.5 Kbytes	PLQP0048KB-A		
R5F21238JFP	64 Kbytes	1 Kbyte X 2	3 Kbytes	PLQP0048KB-A		
R5F2123AJFP	96 Kbytes	1 Kbyte X 2	5 Kbytes	PLQP0048KB-A		
R5F2123CJFP	128 Kbytes(1)	1 Kbyte X 2	6 Kbytes	PLQP0048KB-A		
R5F21236KFP	32 Kbytes	1 Kbyte X 2	2 Kbytes	PLQP0048KB-A	K version	
R5F21237KFP	48 Kbytes	1 Kbyte X 2	2.5 Kbytes	PLQP0048KB-A		
R5F21238KFP	64 Kbytes	1 Kbyte X 2	3 Kbytes	PLQP0048KB-A		
R5F2123AKFP	96 Kbytes	1 Kbyte X 2	5 Kbytes	PLQP0048KB-A		
R5F2123CKFP	128 Kbytes(1)	1 Kbyte X 2	6 Kbytes	PLQP0048KB-A		

NOTE:
1. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **24. Notes on Emulator Debugger** of Hardware Manual.

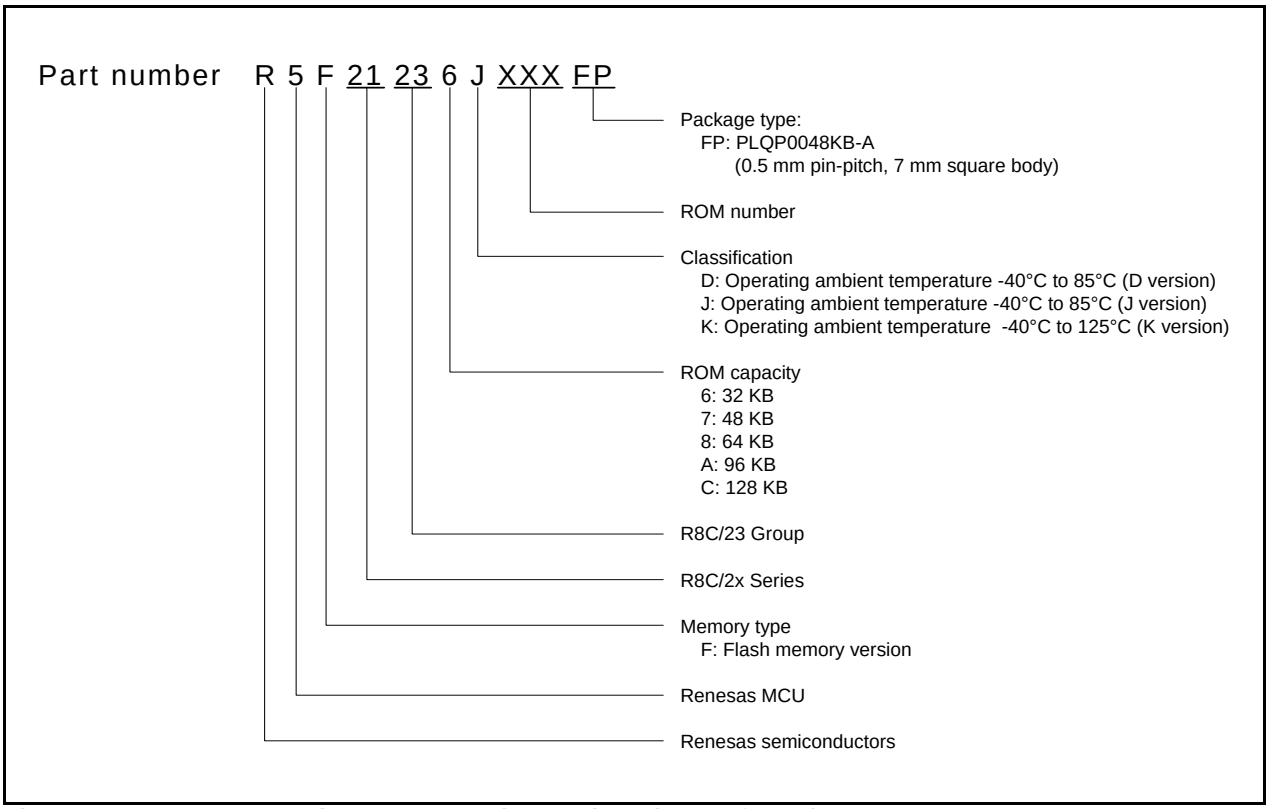
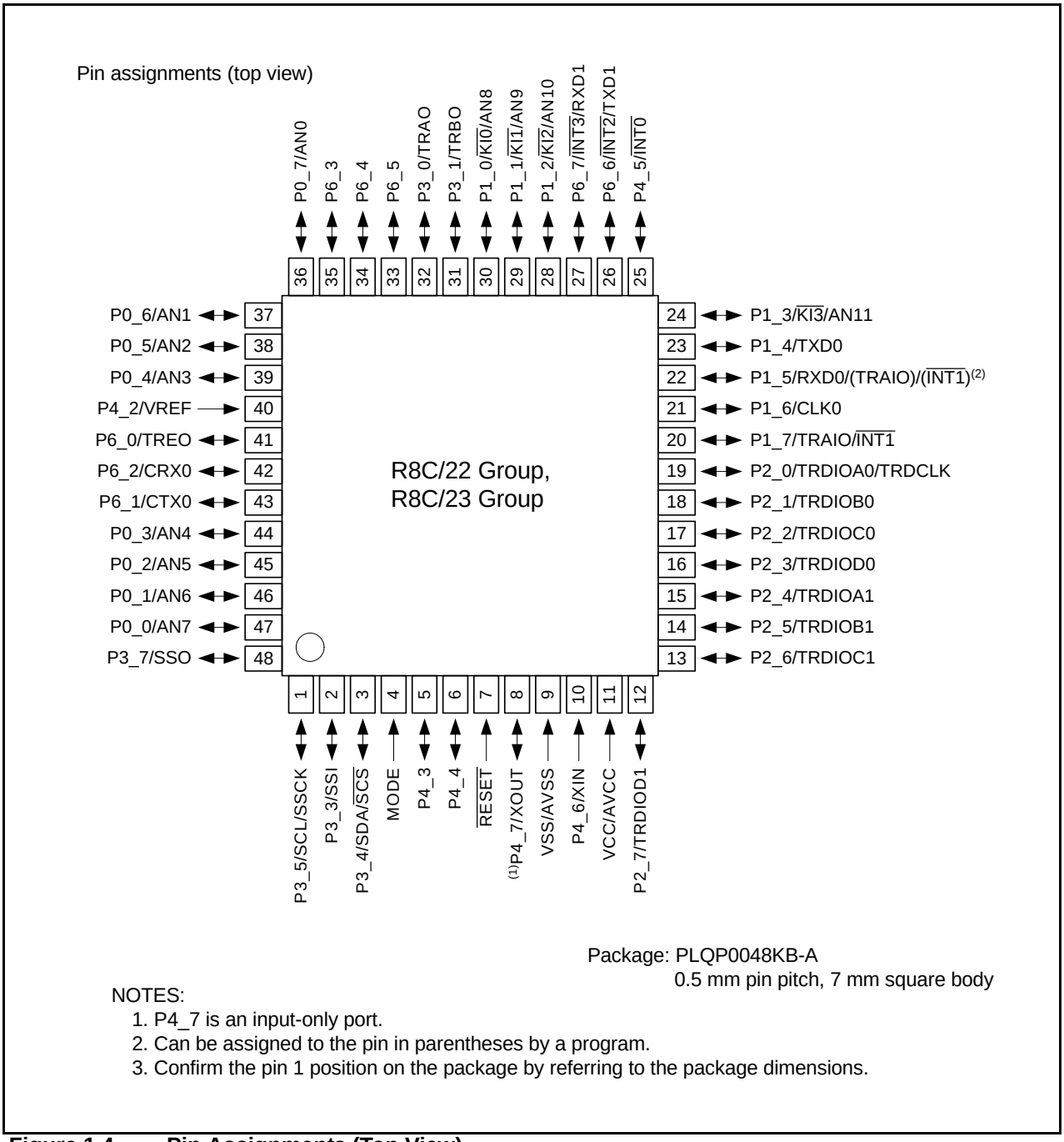


Figure 1.3 Type Number, Memory Size, and Package of R8C/23 Group

1.5 Pin Assignments

Figure 1.4 shows Pin Assignments (Top View).



NOTES:
1. P4_7 is an input-only port.
2. Can be assigned to the pin in parentheses by a program.
3. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.4 Pin Assignments (Top View)

Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules						
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I^2C Bus Interface	CAN Module	A/D Converter
1		P3_5				SSCK	SCL		
2		P3_3				SSI			
3		P3_4				$\overline{SCS}$	SDA		
4	MODE								
5		P4_3							
6		P4_4							
7	$\overline{RESET}$								
8	XOUT	P4_7							
9	VSS/AVSS								
10	XIN	P4_6							
11	VCC/AVCC								
12		P2_7		TRDIOD1					
13		P2_6		TRDIOC1					
14		P2_5		TRDIOB1					
15		P2_4		TRDIOA1					
16		P2_3		TRDIOD0					
17		P2_2		TRDIOC0					
18		P2_1		TRDIOB0					
19		P2_0		TRDIOA0/TRDCLK					
20		P1_7	$\overline{INT1}$	TRAIO					
21		P1_6			CLK0				
22		P1_5	($\overline{INT1}$)(1)	(TRAIO)(1)	RXD0				
23		P1_4			TXD0				
24		P1_3	$\overline{KI3}$						AN11
25		P4_5	$\overline{INT0}$	$\overline{INT0}$					
26		P6_6	$\overline{INT2}$		TXD1				
27		P6_7	$\overline{INT3}$		RXD1				
28		P1_2	$\overline{KI2}$						AN10
29		P1_1	$\overline{KI1}$						AN9
30		P1_0	$\overline{KI0}$						AN8
31		P3_1		TRBO					
32		P3_0		TRAO					
33		P6_5							
34		P6_4							
35		P6_3							
36		P0_7							AN0
37		P0_6							AN1
38		P0_5							AN2
39		P0_4							AN3
40	VREF	P4_2							
41		P6_0		TREO					
42		P6_2						CRX0	
43		P6_1						CTX0	
44		P0_3							AN4
45		P0_2							AN5
46		P0_1							AN6
47		P0_0							AN7
48		P3_7				SSO			

NOTE:
1. Can be assigned to the pin in parentheses by a program.

Table 4.4 SFR Information (4)(1)

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h			XXh
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Control Register 2	ADCON2	00h
00D5h			
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h	UART1 Function Select Register	U1SR	XXh
00F6h			
00F7h			
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	XX00XX00b
00FEh			
00FFh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.9 SFR Information (9)(1)

Address	Register	Symbol	After reset
1340h			
1341h			
1342h	CAN0 Acceptance Filter Support Register	C0AFS	XXh
1343h			XXh
1344h			
1345h			
1346h			
1347h			
1348h			
1349h			
134Ah			
134Bh			
134Ch			
134Dh			
134Eh			
134Fh			
1350h			
1351h			
1352h			
1353h			
1354h			
1355h			
1356h			
1357h			
1358h			
1359h			
135Ah			
135Bh			
135Ch			
135Dh			
135Eh			
135Fh	CAN0 Clock Select Register	CCLKR	00h
1360h	CAN0 Slot 0: Identifier/DLC		XXh
1361h			XXh
1362h			XXh
1363h			XXh
1364h			XXh
1365h			XXh
1366h	CAN0 Slot 0: Data Field		XXh
1367h			XXh
1368h			XXh
1369h			XXh
136Ah			XXh
136Bh			XXh
136Ch			XXh
136Dh			XXh
136Eh	CAN0 Slot 0: Time Stamp		XXh
136Fh			XXh
1370h	CAN0 Slot 1: Identifier/DLC		XXh
1371h			XXh
1372h			XXh
1373h			XXh
1374h			XXh
1375h			XXh
1376h	CAN0 Slot 1: Data Field		XXh
1377h			XXh
1378h			XXh
1379h			XXh
137Ah			XXh
137Bh			XXh
137Ch			XXh
137Dh			XXh
137Eh	CAN0 Slot 1: Time Stamp		XXh
137Fh			XXh

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.10 SFR Information (10)(1)

Address	Register	Symbol	After reset
1380h	CAN0 Slot 2: Identifier/DLC		XXh
1381h			XXh
1382h			XXh
1383h			XXh
1384h			XXh
1385h			XXh
1386h	CAN0 Slot 2: Data Field		XXh
1387h			XXh
1388h			XXh
1389h			XXh
138Ah			XXh
138Bh			XXh
138Ch			XXh
138Dh			XXh
138Eh	CAN0 Slot 2: Time Stamp		XXh
138Fh			XXh
1390h	CAN0 Slot 3: Identifier/DLC		XXh
1391h			XXh
1392h			XXh
1393h			XXh
1394h			XXh
1395h			XXh
1396h	CAN0 Slot 3: Data Field		XXh
1397h			XXh
1398h			XXh
1399h			XXh
139Ah			XXh
139Bh			XXh
139Ch			XXh
139Dh			XXh
139Eh	CAN0 Slot 3: Time Stamp		XXh
139Fh			XXh
13A0h	CAN0 Slot 4: Identifier/DLC		XXh
13A1h			XXh
13A2h			XXh
13A3h			XXh
13A4h			XXh
13A5h			XXh
13A6h	CAN0 Slot 4: Data Field		XXh
13A7h			XXh
13A8h			XXh
13A9h			XXh
13AAh			XXh
13ABh			XXh
13ACh			XXh
13ADh			XXh
13AEh	CAN0 Slot 4: Time Stamp		XXh
13AFh			XXh
13B0h	CAN0 Slot 5: Identifier/DLC		XXh
13B1h			XXh
13B2h			XXh
13B3h			XXh
13B4h			XXh
13B5h			XXh
13B6h	CAN0 Slot 5: Data Field		XXh
13B7h			XXh
13B8h			XXh
13B9h			XXh
13BAh			XXh
13BBh			XXh
13BCh			XXh
13BDh			XXh
13BEh	CAN0 Slot 5: Time Stamp		XXh
13BFh			XXh

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.12 SFR Information (12)(1)

Address	Register	Symbol	After reset
1400h	CAN0 Slot 10: Identifier/DLC		XXh
1401h			XXh
1402h			XXh
1403h			XXh
1404h			XXh
1405h			XXh
1406h	CAN0 Slot 10: Data Field		XXh
1407h			XXh
1408h			XXh
1409h			XXh
140Ah			XXh
140Bh			XXh
140Ch			XXh
140Dh			XXh
140Eh	CAN0 Slot 10: Time Stamp		XXh
140Fh			XXh
1410h	CAN0 Slot 11: Identifier/DLC		XXh
1411h			XXh
1412h			XXh
1413h			XXh
1414h			XXh
1415h			XXh
1416h	CAN0 Slot 11: Data Field		XXh
1417h			XXh
1418h			XXh
1419h			XXh
141Ah			XXh
141Bh			XXh
141Ch			XXh
141Dh			XXh
141Eh	CAN0 Slot 11: Time Stamp		XXh
141Fh			XXh
1420h	CAN0 Slot 12: Identifier/DLC		XXh
1421h			XXh
1422h			XXh
1423h			XXh
1424h			XXh
1425h			XXh
1426h	CAN0 Slot 12: Data Field		XXh
1427h			XXh
1428h			XXh
1429h			XXh
142Ah			XXh
142Bh			XXh
142Ch			XXh
142Dh			XXh
142Eh	CAN0 Slot 12: Time Stamp		XXh
142Fh			XXh
1430h	CAN0 Slot 13: Identifier/DLC		XXh
1431h			XXh
1432h			XXh
1433h			XXh
1434h			XXh
1435h			XXh
1436h	CAN0 Slot 13: Data Field		XXh
1437h			XXh
1438h			XXh
1439h			XXh
143Ah			XXh
143Bh			XXh
143Ch			XXh
143Dh			XXh
143Eh	CAN0 Slot 13: Time Stamp		XXh
143Fh			XXh

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.13 SFR Information (13)(1)

Address	Register	Symbol	After reset
1440h	CAN0 Slot 14: Identifier/DLC		XXh
1441h			XXh
1442h			XXh
1443h			XXh
1444h			XXh
1445h			XXh
1446h	CAN0 Slot 14: Data Field		XXh
1447h			XXh
1448h			XXh
1449h			XXh
144Ah			XXh
144Bh			XXh
144Ch			XXh
144Dh			XXh
144Eh	CAN0 Slot 14: Time Stamp		XXh
144Fh			XXh
1450h	CAN0 Slot 15: Identifier/DLC		XXh
1451h			XXh
1452h			XXh
1453h			XXh
1454h			XXh
1455h			XXh
1456h	CAN0 Slot 15: Data Field		XXh
1457h			XXh
1458h			XXh
1459h			XXh
145Ah			XXh
145Bh			XXh
145Ch			XXh
145Dh			XXh
145Eh	CAN0 Slot 15: Time Stamp		XXh
145Fh			XXh
1460h	CAN0 Global Mask Register	C0GMR	XXh
1461h			XXh
1462h			XXh
1463h			XXh
1464h			XXh
1465h			XXh
1466h	CAN0 Local Mask A Register	C0LMAR	XXh
1467h			XXh
1468h			XXh
1469h			XXh
146Ah			XXh
146Bh			XXh
146Ch	CAN0 Local Mask B Register	C0LMBR	XXh
146Dh			XXh
146Eh			XXh
146Fh			XXh
1470h			XXh
1471h			XXh
1472h			
1473h			
1474h			
1475h			

FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)	R8C/22 Group	100(3)	–	–	times
		R8C/23 Group	1,000(3)	–	–	times
–	Byte program time		–	50	400	µs
–	Block erase time		–	0.4	9	s
$t_{d(SR-SUS)}$	Time delay from suspend request until erase suspend		–	–	97 + CPU clock × 6 cycle	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3 + CPU clock × 4 cycle	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time(7)	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 1,000), each block can be erased n times.
   For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure endurance can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.5 Flash Memory (Data Flash Block A, Block B) Electrical Characteristics(4)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)		10,000(3)	–	–	times
–	Byte program time (Program/erase endurance ≤ 1,000 times)		–	50	400	µs
–	Byte program time (Program/erase endurance > 1,000 times)		–	65	–	µs
–	Block erase time (Program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (Program/erase endurance > 1,000 times)		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until erase suspend		–	–	97 + CPU clock × 6 cycle	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3 + CPU clock × 4 cycle	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		-40	–	85(8)	°C
–	Data hold time(9)	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times.
   For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Minimum endurance to guarantee all electrical characteristics after program and erase (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times are the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure endurance can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
6. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. 125°C for K version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

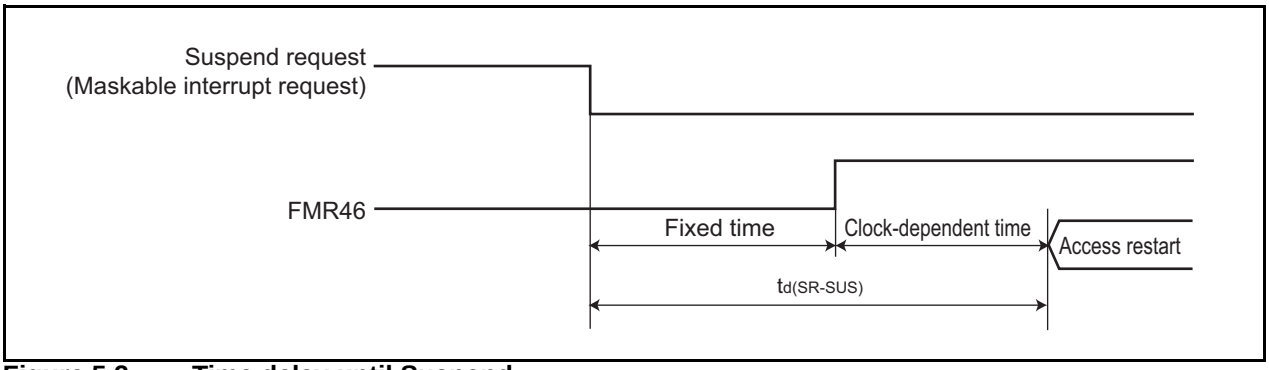


Figure 5.2 Time delay until Suspend

Table 5.6 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level(3, 4)		2.70	2.85	3.00	V
$t_{d(Vdet1-A)}$	Voltage monitor 1 reset generation time(5)		–	40	200	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(2)		–	–	100	µs
Vccmin	MCU operating voltage minimum value		2.70	–	–	V

NOTES:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and Topr = -40°C to 85°C (D, J version) / -40°C to 125°C (K version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
3. Hold $V_{det2} > V_{det1}$.
4. This parameter shows the voltage detection level when the power supply drops. The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.
5. Time until the voltage monitor 1 reset is generated after the voltage passes V_{det1} when V_{CC} falls. When using the digital filter, its sampling time is added to $t_{d(Vdet1-A)}$. When using the voltage monitor 1 reset, maintain this time until V_{CC} = 2.0 V after the voltage passes V_{det1} when the power supply falls.

Table 5.7 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level(4)		3.3	3.6	3.9	V
$t_{d(Vdet2-A)}$	Voltage monitor 2 reset/interrupt request generation time(2, 5)		–	40	200	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and Topr = -40°C to 85°C (D, J version) / -40°C to 125°C (K version).
2. Time until the voltage monitor 2 reset/interrupt request is generated since the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.
4. Hold $V_{det2} > V_{det1}$.
5. When using the digital filter, its sampling time is added to $t_{d(Vdet2-A)}$. When using the voltage monitor 2 reset, maintain this time until V_{CC} = 2.0 V after the voltage passes V_{det2} when the power supply falls.

Table 5.12 Timing Requirements of Clock Synchronous Serial I/O with Chip Select(1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	–	t_{CYC}(2)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_H	SSO, SSI data input hold time			1	–	–	t_{CYC}(2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1	t_{CYC}(2)
t_{SA}	SSI slave access time			–	–	1t_{CYC} + 100	ns
t_{OR}	SSI slave out open time			–	–	1t_{CYC} + 100	ns

NOTES:
1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. 1t_{CYC} = 1/f1(s)

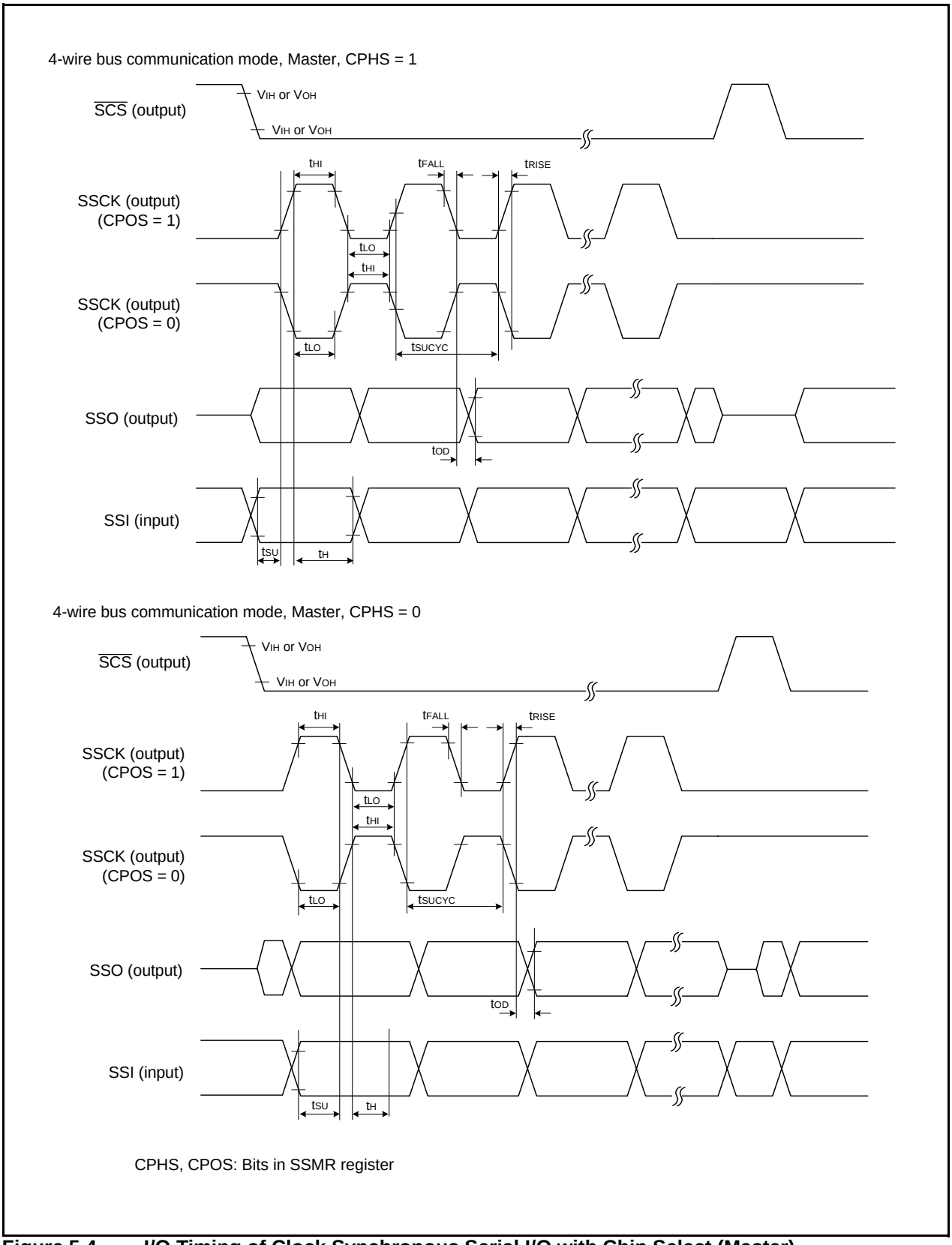


Figure 5.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

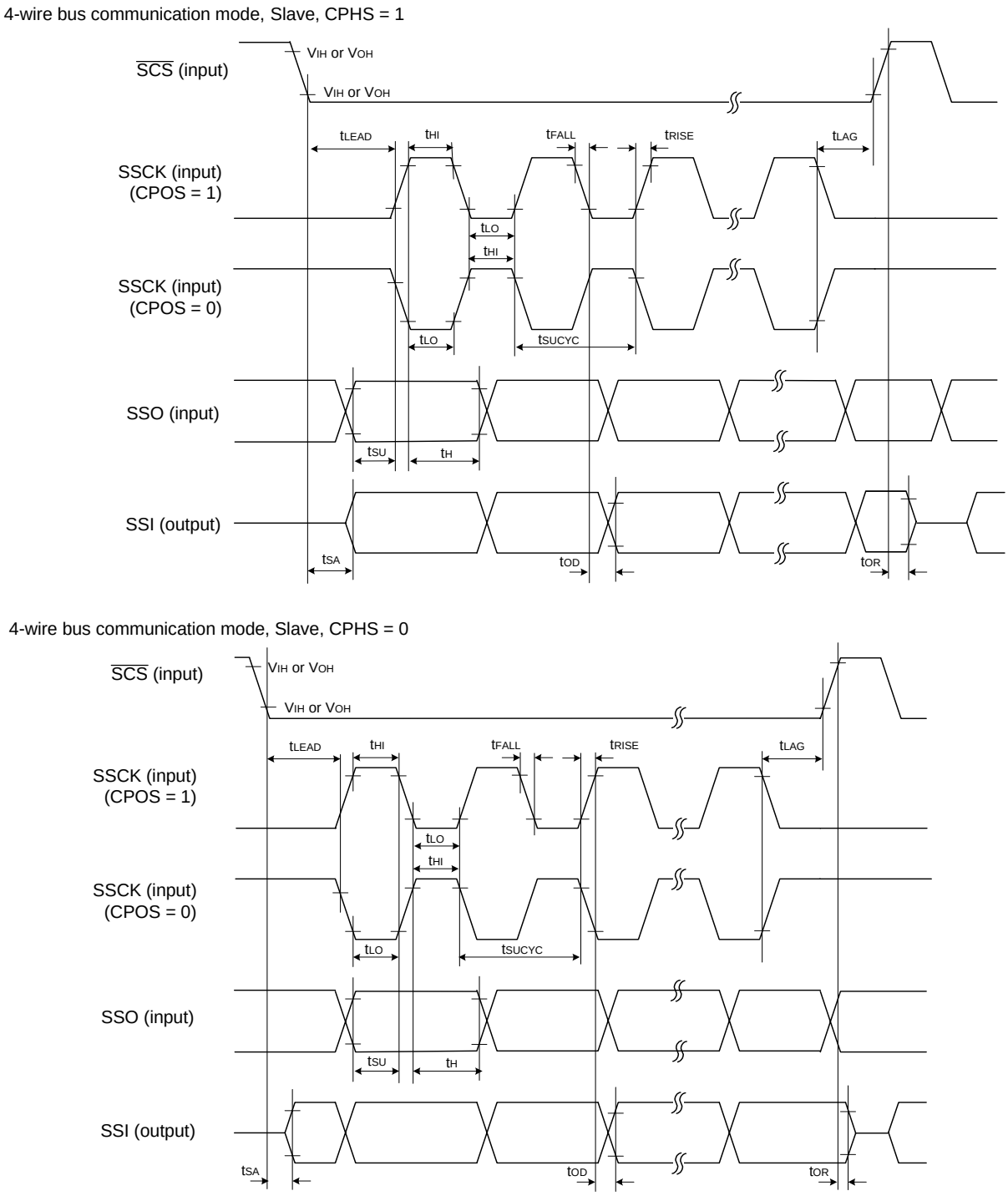


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

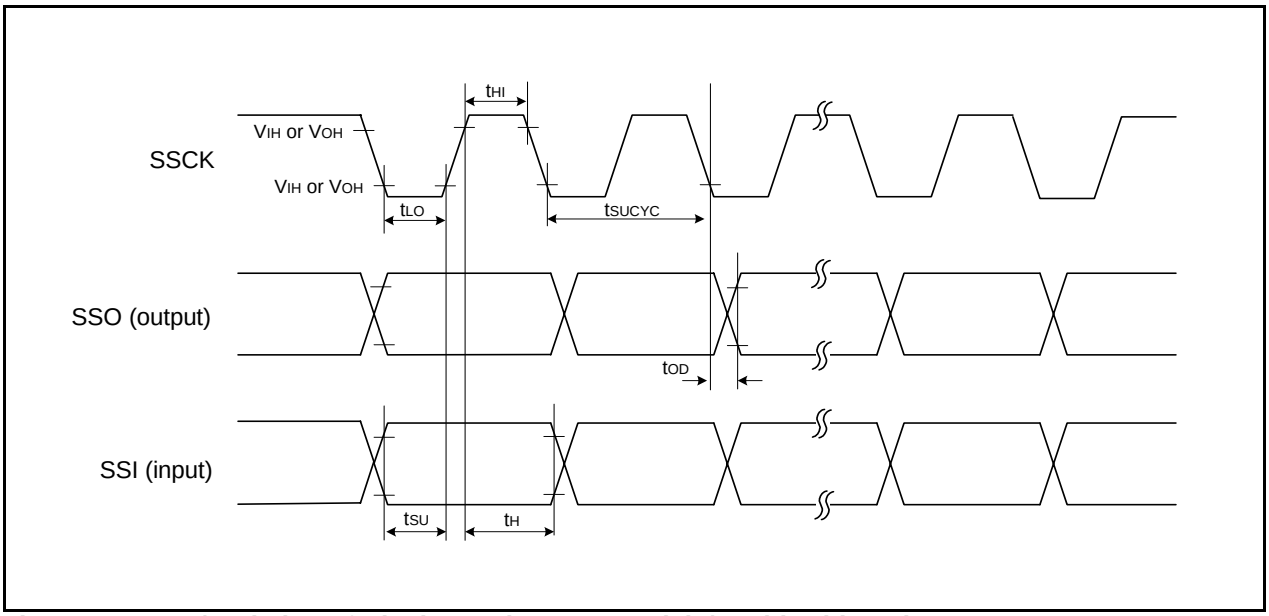
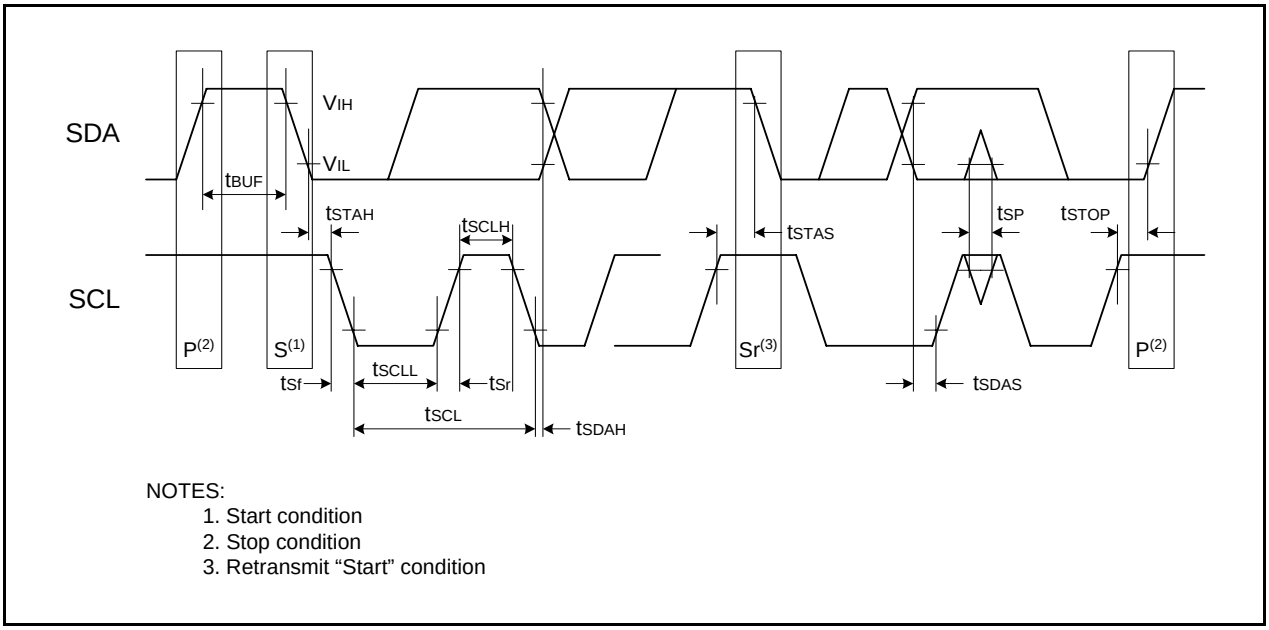


Figure 5.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

Table 5.13 Timing Requirements of I²C Bus Interface(1)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC}$ + 600(2)	–	–	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC}$ + 300(2)	–	–	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC}$ + 500(2)	–	–	ns
t_{sf}	SCL, SDA input falling time		–	–	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		–	–	$1t_{CYC}$(2)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$(2)	–	–	ns
t_{STAH}	Start condition input hole time		$3t_{CYC}$(2)	–	–	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{SOAS}	Data input setup time		$1t_{CYC}$ + 20(2)	–	–	ns
t_{SDAH}	Data input hold time		0	–	–	ns

NOTES:
1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. $1t_{CYC}$ = 1/f1(s)



NOTES:
1. Start condition
2. Stop condition
3. Retransmit “Start” condition

Figure 5.7 I/O Timing of I²C Bus Interface

Timing Requirements (Unless Otherwise Specified: Vcc = 3 V, Vss = 0V at Topr = 25°C) [Vcc = 3 V]

Table 5.22 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns

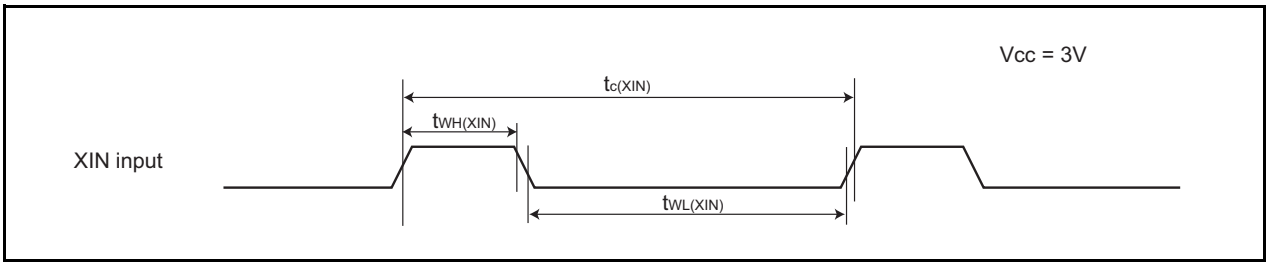


Figure 5.12 XIN Input Timing Diagram when Vcc = 3 V

Table 5.23 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input Cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

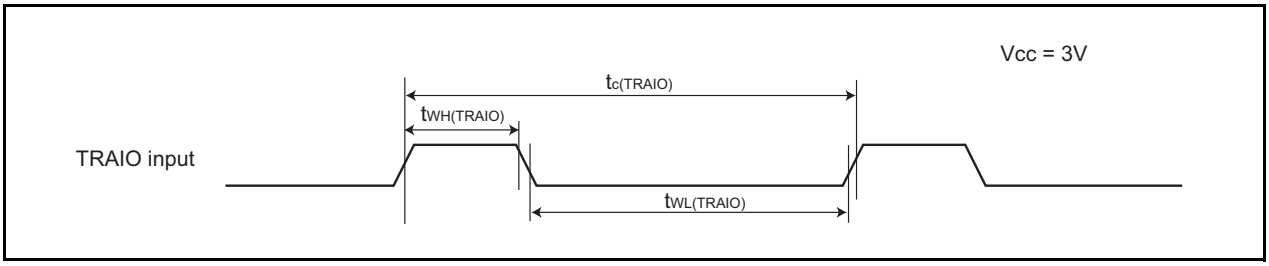


Figure 5.13 TRAIO Input Timing Diagram when Vcc = 3 V

REVISION HISTORY	R8C/22 Group, R8C/23 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.20	Sep 29, 2005	20	Table 4.6 SFR Information (6) revised - 0145h: POCR0 → TRDPOCR0 - 0146h, 0147h: TRDCNT0 → TRD0 - 0148h, 0149h: GRA0 → TRDGRA0 - 014Ah, 014Bh: GRB0 → TRDGRB0 - 014Ch, 014Dh: GRC0 → TRDGRC0 - 014Eh, 014Fh: GRD0 → TRDGRD0 - 0155h: POCR1 -> TRDPOCR1 - 0156h, 0157h: TRDCNT1 → TRD1 - 0158h, 0159h: GRA1 → TRDGRA1 - 015Ah, 015Bh: GRB1 → TRDGRB1 - 015Ch, 015Dh: GRC1 → TRDGRC1 - 015Eh, 015Fh: GRD1 → TRDGRD1
		28	5. Electrical Characteristics added
1.00	Oct 27, 2006	All pages	"Preliminary" and "Under development" deleted
		2	Table 1.1 Functions and Specifications for R8C/22 Group revised. NOTE1 deleted.
		3	Table 1.2 Functions and Specifications for R8C/23 Group revised. NOTE1 deleted.
		5	Table 1.3 Product Information for R8C/22 Group; "R5F2122AJFP (D)", "R5F2122CJFP (D)", "R5F2122AKFP (D)", "R5F2122CKFP (D)", and NOTE added. Figure 1.2 Type Number, Memory Size, and Package of R8C/22 Group; "A: 96 KB" and "C: 128 KB" added.
		6	Table 1.4 Product Information for R8C/23 Group; "R5F2123AJFP (D)", "R5F2123CJFP (D)", "R5F2123AKFP (D)", "R5F2123CKFP (D)", and NOTE added. Figure 1.3 Type Number, Memory Size, and Package of R8C/23 Group; "A: 96 KB" and "C: 128 KB" added.
		13	Figure 3.1 Memory Map of R8C/22 Group revised.
		14	Figure 3.2 Memory Map of R8C/23 Group revised.
		15	Table 4.1 SFR Information (1)(1); NOTE8; "The CSPROINI bit in the OFS register is set to 0." → "The CSPROINI bit in the OFS register is 0." revised.
		28	Table 5.1 Absolute Maximum Ratings; Power dissipation revised. Table 5.2 Recommended Operating Conditions; System clock revised.
		33	Table 5.8 Voltage Monitor 1 Reset Circuit Electrical Characteristics → Table 5.8 Power-on Reset Circuit, Voltage Monitor 1 Reset Circuit Electrical Characteristics(1) replaced. Table 5.8 revised. NOTE3 added. Table 5.9 Power-on Reset Circuit Electrical Characteristics deleted. Figure 5.3 Power-on Reset Circuit Electrical Characteristics revised.
		34	Table 5.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics → Table 5.9 High-Speed On-Chip Oscillator Circuit Electrical Characteristics revised.