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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21236jfp-u1

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

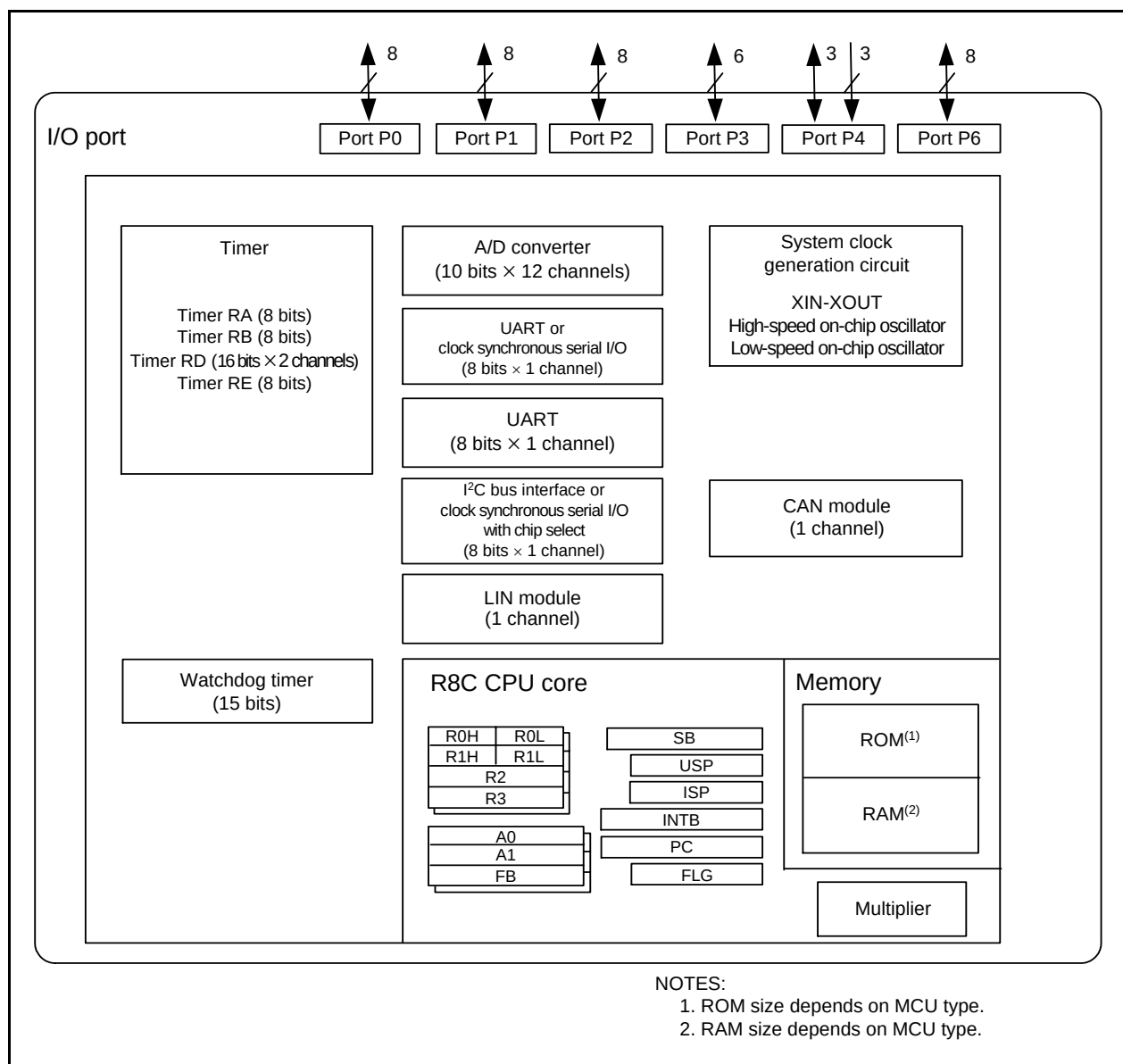


Figure 1.1 Block Diagram

Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules						
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I ² C Bus Interface	CAN Module	A/D Converter
1		P3_5				SSCK	SCL		
2		P3_3				SSI			
3		P3_4				SCS	SDA		
4	MODE								
5		P4_3							
6		P4_4							
7	RESET								
8	XOUT	P4_7							
9	VSS/AVSS								
10	XIN	P4_6							
11	VCC/AVCC								
12		P2_7		TRDIOD1					
13		P2_6		TRDIOD1					
14		P2_5		TRDIOD1					
15		P2_4		TRDIOD1					
16		P2_3		TRDIOD0					
17		P2_2		TRDIOD0					
18		P2_1		TRDIOD0					
19		P2_0		TRDIOD0/TRDCLK					
20		P1_7	INT1	TRAIO					
21		P1_6			CLK0				
22		P1_5	(INT1) ⁽¹⁾	(TRAIO) ⁽¹⁾	RXD0				
23		P1_4			TXD0				
24		P1_3	KI3						AN11
25		P4_5	INT0	INT0					
26		P6_6	INT2		TXD1				
27		P6_7	INT3		RXD1				
28		P1_2	KI2						AN10
29		P1_1	KI1						AN9
30		P1_0	KI0						AN8
31		P3_1		TRBO					
32		P3_0		TRAIO					
33		P6_5							
34		P6_4							
35		P6_3							
36		P0_7							AN0
37		P0_6							AN1
38		P0_5							AN2
39		P0_4							AN3
40	VREF	P4_2							
41		P6_0		TREO					
42		P6_2						CRX0	
43		P6_1						CTX0	
44		P0_3							AN4
45		P0_2							AN5
46		P0_1							AN6
47		P0_0							AN7
48		P3_7				SSO			

NOTE:

1. Can be assigned to the pin in parentheses by a program.

Table 4.4 SFR Information (4)⁽¹⁾

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h			XXh
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Control Register 2	ADCON2	00h
00D5h			
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h	UART1 Function Select Register	U1SR	XXh
00F6h			
00F7h			
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	XX00XX00b
00FEh			
00FFh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.6 SFR Information (6)⁽¹⁾

Address	Register	Symbol	After reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIOA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIOC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIOA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIOC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.8 SFR Information (8)⁽¹⁾

Address	Register	Symbol	After reset
1300h	CAN0 Message Control Register 0	C0MCTL0	00h
1301h	CAN0 Message Control Register 1	C0MCTL1	00h
1302h	CAN0 Message Control Register 2	C0MCTL2	00h
1303h	CAN0 Message Control Register 3	C0MCTL3	00h
1304h	CAN0 Message Control Register 4	C0MCTL4	00h
1305h	CAN0 Message Control Register 5	C0MCTL5	00h
1306h	CAN0 Message Control Register 6	C0MCTL6	00h
1307h	CAN0 Message Control Register 7	C0MCTL7	00h
1308h	CAN0 Message Control Register 8	C0MCTL8	00h
1309h	CAN0 Message Control Register 9	C0MCTL9	00h
130Ah	CAN0 Message Control Register 10	C0MCTL10	00h
130Bh	CAN0 Message Control Register 11	C0MCTL11	00h
130Ch	CAN0 Message Control Register 12	C0MCTL12	00h
130Dh	CAN0 Message Control Register 13	C0MCTL13	00h
130Eh	CAN0 Message Control Register 14	C0MCTL14	00h
130Fh	CAN0 Message Control Register 15	C0MCTL15	00h
1310h	CAN0 Control Register	C0CTLR	X0000001b
1311h			XX0X0000b
1312h	CAN0 Status Register	C0STR	00h
1313h			X0000001b
1314h	CAN0 Slot Status Register	C0SSTR	00h
1315h			00h
1316h	CAN0 Interrupt Control Register	C0ICR	00h
1317h			00h
1318h	CAN0 Extended ID Register	C0IDR	00h
1319h			00h
131Ah	CAN0 Configuration Register	C0CONR	XXh
131Bh			XXh
131Ch	CAN0 Receive Error Count Register	C0RECR	00h
131Dh	CAN0 Transmit Error Count Register	C0TECR	00h
131Eh			
131Fh			
1320h			
1321h			
1322h			
1323h			
1324h			
1325h			
1326h			
1327h			
1328h			
1329h			
132Ah			
132Bh			
132Ch			
132Dh			
132Eh			
132Fh			
1330h			
1331h			
1332h			
1333h			
1334h			
1335h			
1336h			
1337h			
1338h			
1339h			
133Ah			
133Bh			
133Ch			
133Dh			
133Eh			
133Fh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.9 SFR Information (9)⁽¹⁾

Address	Register	Symbol	After reset
1340h			
1341h			
1342h	CAN0 Acceptance Filter Support Register	C0AFS	XXh
1343h			XXh
1344h			
1345h			
1346h			
1347h			
1348h			
1349h			
134Ah			
134Bh			
134Ch			
134Dh			
134Eh			
134Fh			
1350h			
1351h			
1352h			
1353h			
1354h			
1355h			
1356h			
1357h			
1358h			
1359h			
135Ah			
135Bh			
135Ch			
135Dh			
135Eh			
135Fh	CAN0 Clock Select Register	CCLKR	00h
1360h	CAN0 Slot 0: Identifier/DLC		XXh
1361h			XXh
1362h			XXh
1363h			XXh
1364h			XXh
1365h			XXh
1366h	CAN0 Slot 0: Data Field		XXh
1367h			XXh
1368h			XXh
1369h			XXh
136Ah			XXh
136Bh			XXh
136Ch			XXh
136Dh			XXh
136Eh	CAN0 Slot 0: Time Stamp		XXh
136Fh			XXh
1370h	CAN0 Slot 1: Identifier/DLC		XXh
1371h			XXh
1372h			XXh
1373h			XXh
1374h			XXh
1375h			XXh
1376h	CAN0 Slot 1: Data Field		XXh
1377h			XXh
1378h			XXh
1379h			XXh
137Ah			XXh
137Bh			XXh
137Ch			XXh
137Dh			XXh
137Eh	CAN0 Slot 1: Time Stamp		XXh
137Fh			XXh

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.12 SFR Information (12)⁽¹⁾

Address	Register	Symbol	After reset
1400h	CAN0 Slot 10: Identifier/DLC		XXh
1401h			XXh
1402h			XXh
1403h			XXh
1404h			XXh
1405h			XXh
1406h	CAN0 Slot 10: Data Field		XXh
1407h			XXh
1408h			XXh
1409h			XXh
140Ah			XXh
140Bh			XXh
140Ch			XXh
140Dh			XXh
140Eh	CAN0 Slot 10: Time Stamp		XXh
140Fh			XXh
1410h	CAN0 Slot 11: Identifier/DLC		XXh
1411h			XXh
1412h			XXh
1413h			XXh
1414h			XXh
1415h			XXh
1416h	CAN0 Slot 11: Data Field		XXh
1417h			XXh
1418h			XXh
1419h			XXh
141Ah			XXh
141Bh			XXh
141Ch			XXh
141Dh			XXh
141Eh	CAN0 Slot 11: Time Stamp		XXh
141Fh			XXh
1420h	CAN0 Slot 12: Identifier/DLC		XXh
1421h			XXh
1422h			XXh
1423h			XXh
1424h			XXh
1425h			XXh
1426h	CAN0 Slot 12: Data Field		XXh
1427h			XXh
1428h			XXh
1429h			XXh
142Ah			XXh
142Bh			XXh
142Ch			XXh
142Dh			XXh
142Eh	CAN0 Slot 12: Time Stamp		XXh
142Fh			XXh
1430h	CAN0 Slot 13: Identifier/DLC		XXh
1431h			XXh
1432h			XXh
1433h			XXh
1434h			XXh
1435h			XXh
1436h	CAN0 Slot 13: Data Field		XXh
1437h			XXh
1438h			XXh
1439h			XXh
143Ah			XXh
143Bh			XXh
143Ch			XXh
143Dh			XXh
143Eh	CAN0 Slot 13: Time Stamp		XXh
143Fh			XXh

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.13 SFR Information (13)⁽¹⁾

Address	Register	Symbol	After reset
1440h	CAN0 Slot 14: Identifier/DLC		XXh
1441h			XXh
1442h			XXh
1443h			XXh
1444h			XXh
1445h			XXh
1446h	CAN0 Slot 14: Data Field		XXh
1447h			XXh
1448h			XXh
1449h			XXh
144Ah			XXh
144Bh			XXh
144Ch			XXh
144Dh			XXh
144Eh	CAN0 Slot 14: Time Stamp		XXh
144Fh			XXh
1450h	CAN0 Slot 15: Identifier/DLC		XXh
1451h			XXh
1452h			XXh
1453h			XXh
1454h			XXh
1455h			XXh
1456h	CAN0 Slot 15: Data Field		XXh
1457h			XXh
1458h			XXh
1459h			XXh
145Ah			XXh
145Bh			XXh
145Ch			XXh
145Dh			XXh
145Eh	CAN0 Slot 15: Time Stamp		XXh
145Fh			XXh
1460h	CAN0 Global Mask Register	C0GMR	XXh
1461h			XXh
1462h			XXh
1463h			XXh
1464h			XXh
1465h			XXh
1466h	CAN0 Local Mask A Register	C0LMAR	XXh
1467h			XXh
1468h			XXh
1469h			XXh
146Ah			XXh
146Bh			XXh
146Ch	CAN0 Local Mask B Register	C0LMBR	XXh
146Dh			XXh
146Eh			XXh
146Fh			XXh
1470h			XXh
1471h			XXh
1472h			
1473h			
1474h			
1475h			
FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

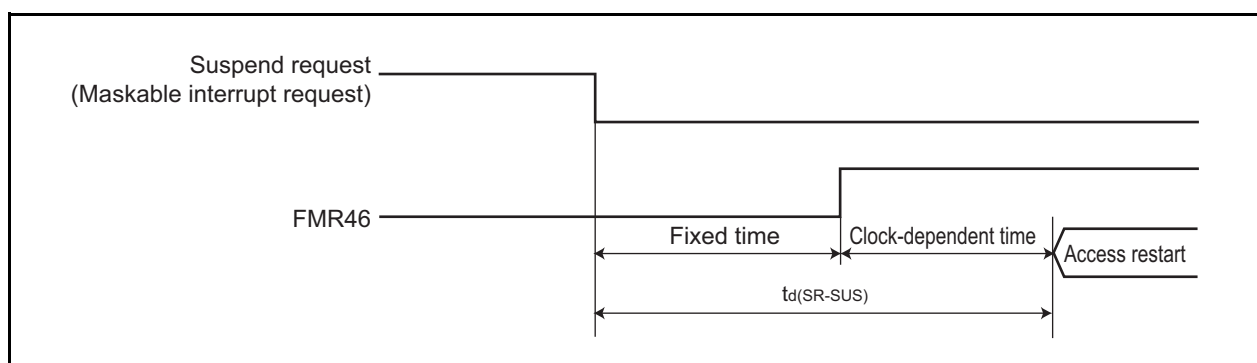


Figure 5.2 Time delay until Suspend

Table 5.6 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet1	Voltage detection level ^(3, 4)		2.70	2.85	3.00	V
td(Vdet1-A)	Voltage monitor 1 reset generation time ⁽⁵⁾		–	40	200	μs
–	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	–	0.6	–	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽²⁾		–	–	100	μs
Vccmin	MCU operating voltage minimum value		2.70	–	–	V

NOTES:

1. The measurement condition is Vcc = 2.7 V to 5.5 V and Topr = -40°C to 85°C (D, J version) / -40°C to 125°C (K version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
3. Hold Vdet2 > Vdet1.
4. This parameter shows the voltage detection level when the power supply drops. The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.
5. Time until the voltage monitor 1 reset is generated after the voltage passes Vdet1 when Vcc falls. When using the digital filter, its sampling time is added to td(Vdet1-A). When using the voltage monitor 1 reset, maintain this time until Vcc = 2.0 V after the voltage passes Vdet1 when the power supply falls.

Table 5.7 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet2	Voltage detection level ⁽⁴⁾		3.3	3.6	3.9	V
td(Vdet2-A)	Voltage monitor 2 reset/interrupt request generation time ^(2, 5)		–	40	200	μs
–	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0V	–	0.6	–	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		–	–	100	μs

NOTES:

1. The measurement condition is Vcc = 2.7 V to 5.5 V and Topr = -40°C to 85°C (D, J version) / -40°C to 125°C (K version).
2. Time until the voltage monitor 2 reset/interrupt request is generated since the voltage passes Vdet2.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.
4. Hold Vdet2 > Vdet1.
5. When using the digital filter, its sampling time is added to td(Vdet2-A). When using the voltage monitor 2 reset, maintain this time until Vcc = 2.0 V after the voltage passes Vdet2 when the power supply falls.

Table 5.8 Power-on Reset Circuit, Voltage Monitor 1 Reset Circuit Electrical Characteristics⁽³⁾

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{por1}	Power-on reset valid voltage ⁽⁴⁾		–	–	0.1	V
V _{por2}	Power-on reset or voltage monitor 1 valid voltage		0	–	V _{det1}	V
trth	External power V _{CC} rise gradient	V _{CC} ≤ 3.6 V	20 ⁽²⁾	–	–	mV/msec
		V _{CC} > 3.6 V	20 ⁽²⁾	–	2,000	mV/msec

NOTES:

1. Topr = -40°C to 85°C (D, J version) / -40°C to 125°C (K version), unless otherwise specified.
2. This condition (the minimum value of external power V_{CC} rise gradient) does not apply if V_{por2} ≥ 1.0 V.
3. To use the power-on reset function, enable voltage monitor 1 reset by setting the LVD1ON bit in the OFS register to 0, the VW1C0 and VW1C6 bits in the VW1C register to 1 respectively, and the VCA26 bit in the VCA2 register to 1.
4. t_{w(por1)} indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain t_{w(por1)} for 30s or more if -20°C ≤ Topr ≤ 125°C, maintain t_{w(por1)} for 3,000s or more if -40°C ≤ Topr < -20°C.

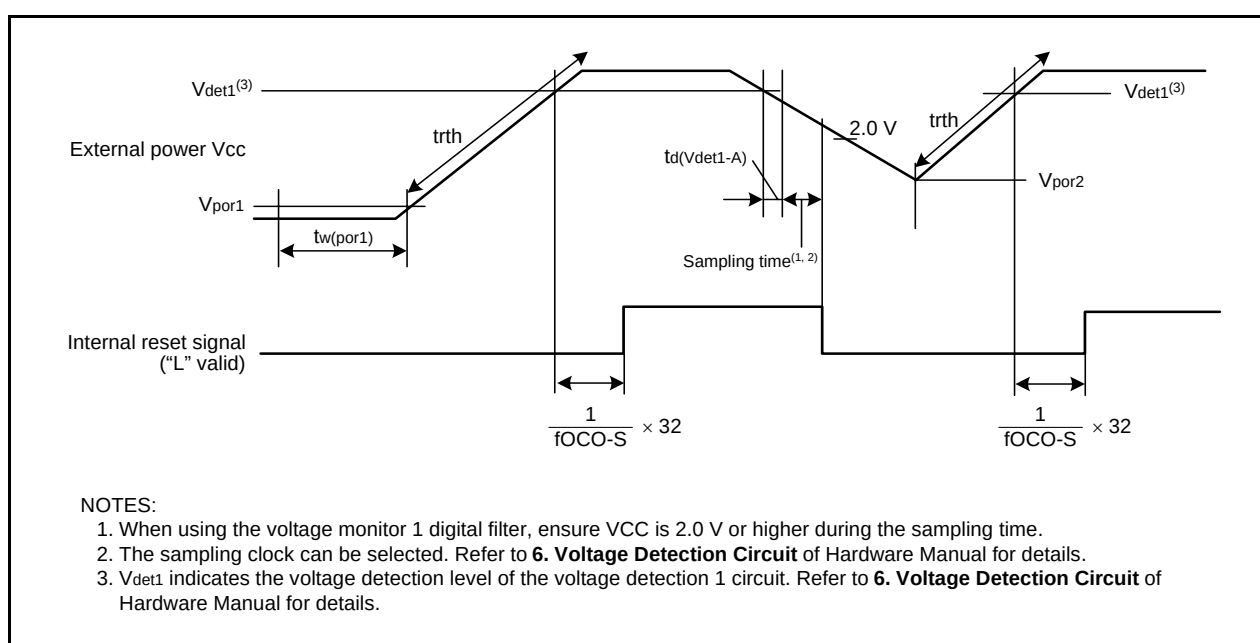
**Figure 5.3 Power-on Reset Circuit Electrical Characteristics**

Table 5.9 High-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V _{CC} = 4.75 V to 5.25 V, 0°C ≤ Topr ≤ 60°C ⁽²⁾	39.2	40	40.8	MHz
		V _{CC} = 3.0 V to 5.25 V, -20°C ≤ Topr ≤ 85°C ⁽²⁾	38.8	40	41.2	MHz
		V _{CC} = 3.0 V to 5.5 V, -40°C ≤ Topr ≤ 85°C ⁽²⁾	38.4	40	41.6	MHz
		V _{CC} = 3.0 V to 5.5 V, -40°C ≤ Topr ≤ 125°C ⁽²⁾	38.0	40	42.0	MHz
		V _{CC} = 2.7 V to 5.5 V, -40°C ≤ Topr ≤ 125°C ⁽²⁾	37.6	40	42.4	MHz
–	The value of the FRA1 register when the reset is deasserted		08h	40	F7h	–
–	High-speed on-chip oscillator adjustment range	Adjust the FRA1 register to -1 bit (the value when the reset is deasserted)	–	+ 0.3	–	MHz
–	Oscillation stability time		–	10	100	μs
–	Self power consumption when high-speed on-chip oscillator oscillating	V _{CC} = 5.0 V, Topr = 25°C	–	600	–	μA

NOTES:

1. V_{CC} = 2.7 V to 5.5 V, Topr = -40°C to 85°C (D, J version) / -40°C to 125°C (K version), unless otherwise specified.
2. The standard value shows when the reset is deasserted for the FRA1 register.

Table 5.10 Low-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		40	125	250	kHz
–	Oscillation stability time		–	10	100	μs
–	Self power consumption when low-speed on-chip oscillator oscillating	V _{CC} = 5.0 V, Topr = 25°C	–	15	–	μA

NOTE:

1. V_{CC} = 2.7 V to 5.5 V, Topr = -40°C to 85°C (D, J version) / -40°C to 125°C (K version), unless otherwise specified.

Table 5.11 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _d (P-R)	Time for internal power supply stabilization during power-on ⁽²⁾		1	–	2000	μs
t _d (R-S)	STOP exit time ⁽³⁾		–	–	150	μs

NOTES:

1. The measurement condition is V_{CC} = 2.7 to 5.5 V and Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until CPU clock supply starts since the interrupt is acknowledged to exit stop mode.

Table 5.12 Timing Requirements of Clock Synchronous Serial I/O with Chip Select⁽¹⁾

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	–	–	tcyc ⁽²⁾
t _{HI}	SSCK clock "H" width			0.4	–	0.6	tsucyc
t _{LO}	SSCK clock "L" width			0.4	–	0.6	tsucyc
trise	SSCK clock rising time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tfall	SSCK clock falling time	Master		–	–	1	tcyc ⁽²⁾
		Slave		–	–	1	μs
tsu	SSO, SSI data input setup time			100	–	–	ns
t _H	SSO, SSI data input hold time			1	–	–	tcyc ⁽²⁾
t _{LEAD}	SCS setup time	Slave		1tcyc + 50	–	–	ns
t _{LAG}	SCS hold time	Slave		1tcyc + 50	–	–	ns
t _{OD}	SSO, SSI data output delay time			–	–	1	tcyc ⁽²⁾
t _{SA}	SSI slave access time			–	–	1tcyc + 100	ns
t _{OR}	SSI slave out open time			–	–	1tcyc + 100	ns

NOTES:

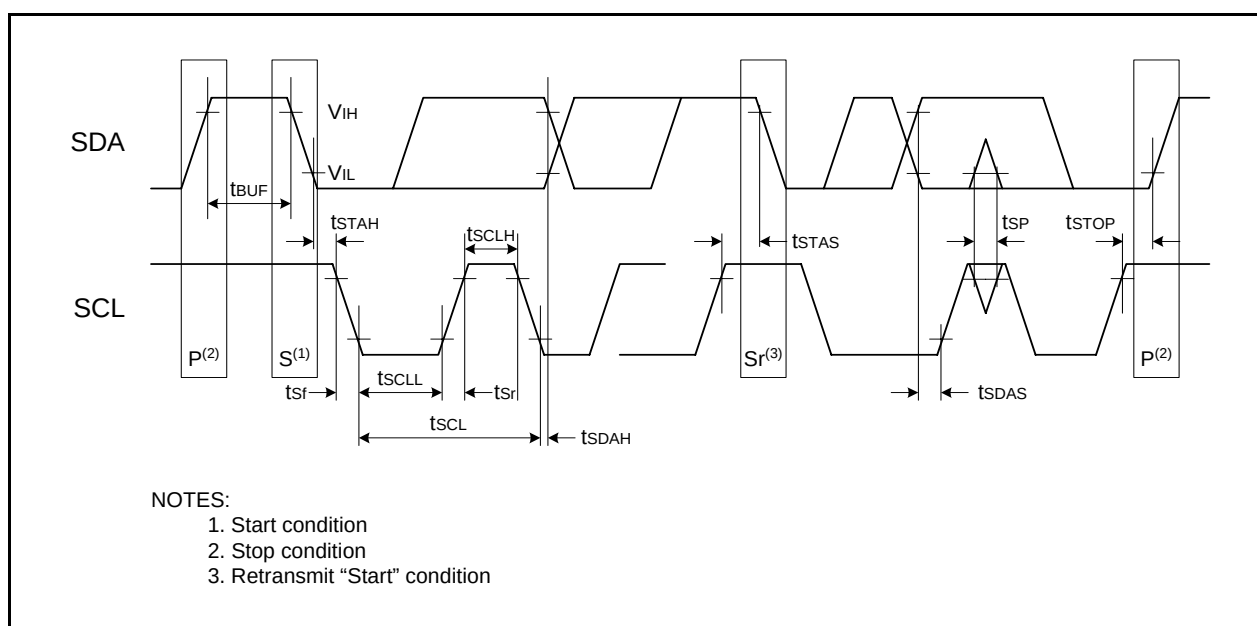
1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. 1tcyc = 1/f₁(s)

Table 5.13 Timing Requirements of I²C Bus Interface⁽¹⁾

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
t _{SCL}	SCL input cycle time		12t _{CYC} + 600 ⁽²⁾	—	—	ns
t _{SCLH}	SCL input "H" width		3t _{CYC} + 300 ⁽²⁾	—	—	ns
t _{SCLL}	SCL input "L" width		5t _{CYC} + 500 ⁽²⁾	—	—	ns
t _{sf}	SCL, SDA input falling time		—	—	300	ns
t _{SP}	SCL, SDA input spike pulse rejection time		—	—	1t _{CYC} ⁽²⁾	ns
t _{BUF}	SDA input bus-free time		5t _{CYC} ⁽²⁾	—	—	ns
t _{STAH}	Start condition input hold time		3t _{CYC} ⁽²⁾	—	—	ns
t _{STAS}	Retransmit start condition input setup time		3t _{CYC} ⁽²⁾	—	—	ns
t _{STOP}	Stop condition input setup time		3t _{CYC} ⁽²⁾	—	—	ns
t _{SOAS}	Data input setup time		1t _{CYC} + 20 ⁽²⁾	—	—	ns
t _{SDAH}	Data input hold time		0	—	—	ns

NOTES:

1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. 1t_{CYC} = 1/f₁(s)

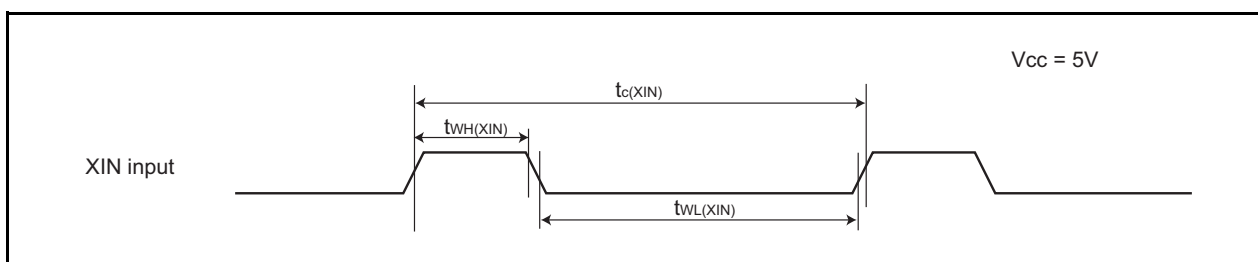
**Figure 5.7 I/O Timing of I²C Bus Interface**

**Table 5.15 Electrical Characteristics (2) [Vcc = 5 V]
(Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), Unless Otherwise Specified.)**

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) In single-chip mode, the output pins are open and other pins are Vss	High-clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	12.5	25.0	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	10.0	20.0	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6.5	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	6.5	–	mA
			XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	5.0	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	6.5	13.0	mA
			XIN clock off High-speed on-chip oscillator on fOCO= 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.2	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 FMR47 = 1	–	150	300	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA20 = 0 VCA26 = VCA27 = 0	–	60	120	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA20 = 0 VCA26 = VCA27 = 0	–	38	76	μA
		Stop mode Topr = 25°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	0.8	3.0	μA
		Stop mode Topr = 85°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	1.2	–	μA
		Stop mode Topr = 125°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	4.0	–	μA

Timing Requirements (Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^{\circ}\text{C}$) [$V_{CC} = 5\text{ V}$]**Table 5.16 XIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(\text{XIN})$	XIN input cycle time	50	–	ns
$t_{WH}(\text{XIN})$	XIN input "H" width	25	–	ns
$t_{WL}(\text{XIN})$	XIN input "L" width	25	–	ns

**Figure 5.8 XIN Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.17 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_c(\text{TRAIO})$	TRAIO input cycle time	100	–	ns
$t_{WH}(\text{TRAIO})$	TRAIO input "H" width	40	–	ns
$t_{WL}(\text{TRAIO})$	TRAIO input "L" width	40	–	ns

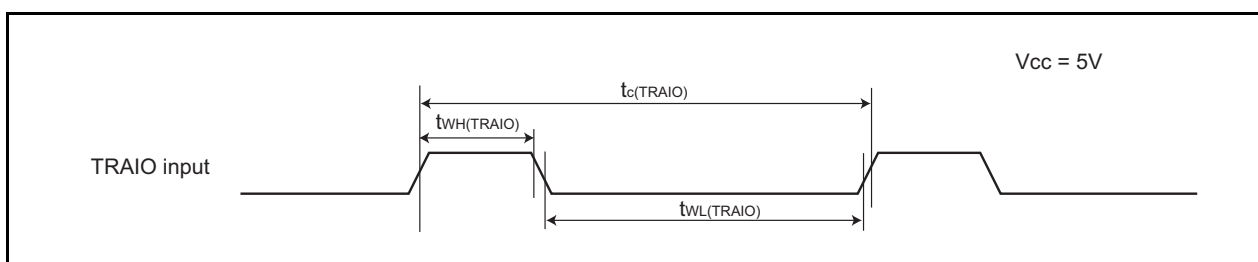
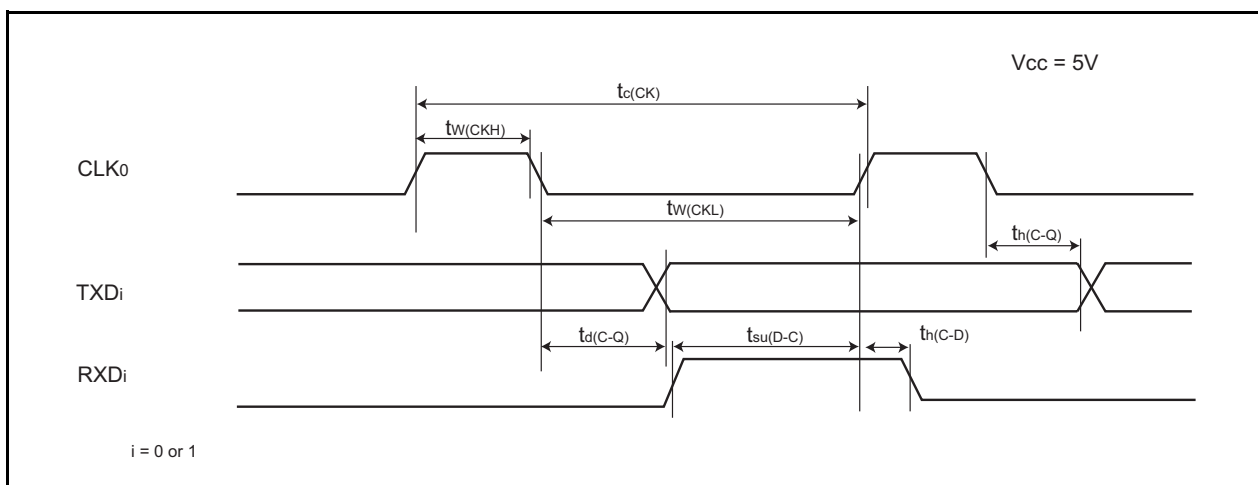
**Figure 5.9 TRAIO Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Table 5.18 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	200	—	ns
$t_{w(CKH)}$	CLK0 input "H" width	100	—	ns
$t_{w(CKL)}$	CLK0 input "L" width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

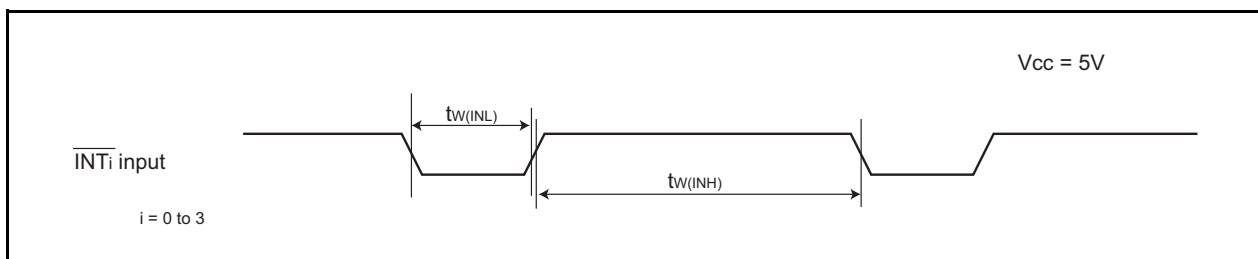
i = 0 or 1

**Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.19 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input "H" width	250 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INTi}$ input "L" width	250 ⁽²⁾	—	ns

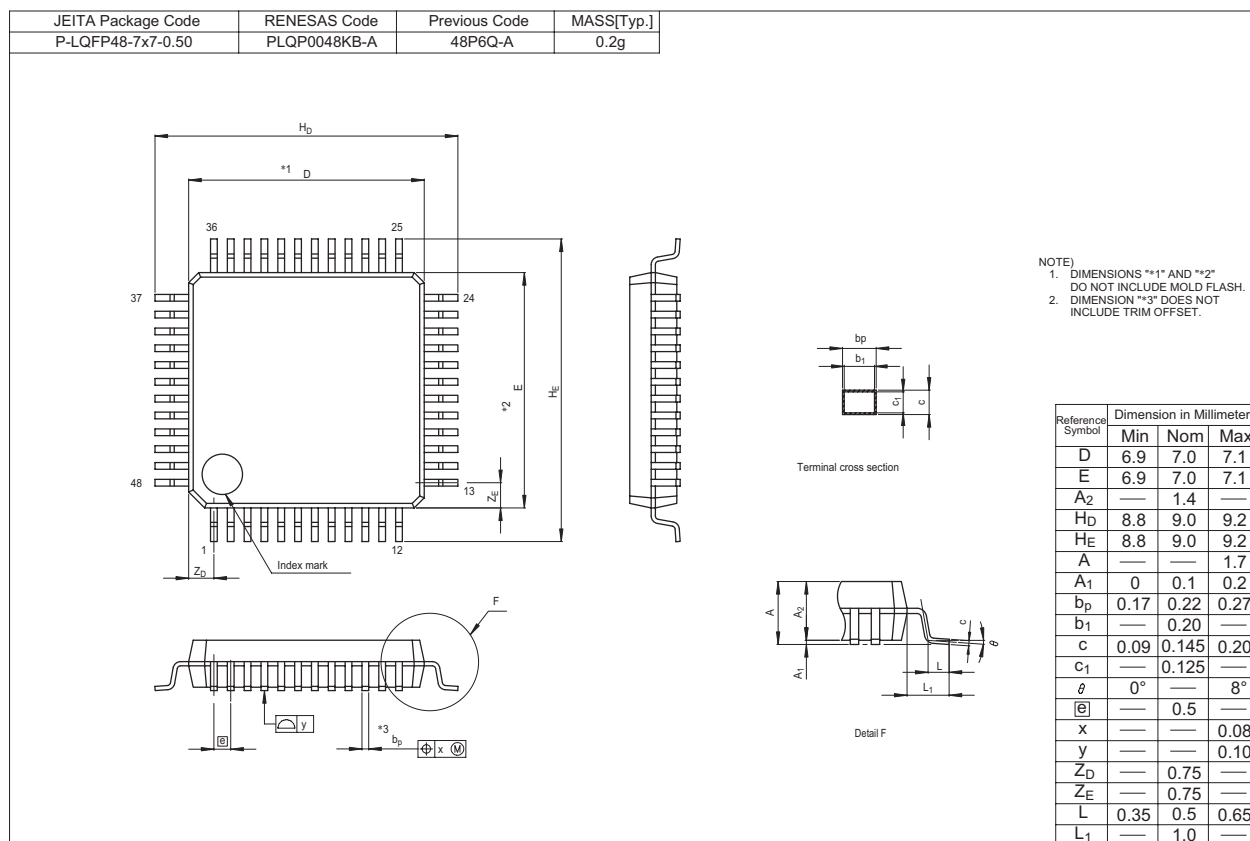
NOTES:

1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input HIGH width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input LOW width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.

**Figure 5.11 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 5 V (i = 0 to 3)**

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.



REVISION HISTORY	R8C/22 Group, R8C/23 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.10	Mar 08, 2005	–	First Edition issued
0.20	Sep 29, 2005	–	Words standardized - Clock synchronous serial interface → Clock synchronous serial I/O - Chip-select clock synchronous interface(SSU) → Clock synchronous serial I/O with chip select - I ² C bus interface(IIC) → I ² C bus interface
		2, 3	Table1.1 R8C/22 Group Performance, Table1.2 R8C/23 Group Performance Serial Interface revised: - Clock Synchronous Serial Interface: 1 channel I ² C bus Interface (3), Clock synchronous serial I/O with chip select - Power-On Reset Circuit added - Power Consumption value determined
		5, 6	Table 1.3 Product Information of R8C/22 Group, Table 1.4 Product Information of R8C/23 Group Date revised.
		7	Figure 1.4 Pin Assignment Pin name revised: - P3_5/SSCK(/SCL) → P3_5/ SCL/SSCK - P3_4/SCS(/SDA) → P3_4/ SDA /SCS - VSS → VSS/AVSS - VCC → VCC/AVCC - P1_5/RXD0/(TRAIO/INT1) → P1_5/RXD0/(TRAIO)/(INT1) - P6_6/INT2/(TXD1) → P6_6/INT2/TXD1 - P6_7/INT3/(RXD1) → P6_7/INT3/RXD1 - NOTE2 added
		8	Table 1.5 Pin Description - Analog Power Supply Input: line added - I ² C Bus Interface (IIC) → I ² C Bus Interface - SSU → Clock Synchronous Serial I/O with Chip Select
		9	Table 1.6 Pin Name Information by Pin Number revised - Pin Number 1: (SCL) → SCL - Pin Number 2: (SDA) → SDA - Pin Number 9: VSS → VSS/AVSS - Pin Number 11: VCC → VCC/AVCC - Pin Number 26: (TXD1) → TXD1 - Pin Number 27: (RXD1) → RXD1
		15	Table 4.1 SFR Information (1) revised - 0013h: XXXXXX00b → 00h
		17	Table 4.3 SFR Information (3) revised - 00BCh: 0000X000b → 00h/0000X000b
		18	Table 4.4 SFR Information (4) revised - 00D6h: 00000XXXb → 00h - 00F5h: UART1 Function Select Register added
		19	Table 4.5 SFR Information (5) revised - 0104h: TRATR → TRA

REVISION HISTORY	R8C/22 Group, R8C/23 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.20	Sep 29, 2005	20	Table 4.6 SFR Information (6) revised - 0145h: POCR0 → TRDPOCR0 - 0146h, 0147h: TRDCNT0 → TRD0 - 0148h, 0149h: GRA0 → TRDGRA0 - 014Ah, 014Bh: GRB0 → TRDGRB0 - 014Ch, 014Dh: GRC0 → TRDGRC0 - 014Eh, 014Fh: GRD0 → TRDGRD0 - 0155h: POCR1 → TRDPOCR1 - 0156h, 0157h: TRDCNT1 → TRD1 - 0158h, 0159h: GRA1 → TRDGRA1 - 015Ah, 015Bh: GRB1 → TRDGRB1 - 015Ch, 015Dh: GRC1 → TRDGRC1 - 015Eh, 015Fh: GRD1 → TRDGRD1
		28	5. Electrical Characteristics added
1.00	Oct 27, 2006	All pages	"Preliminary" and "Under development" deleted
		2	Table 1.1 Functions and Specifications for R8C/22 Group revised. NOTE1 deleted.
		3	Table 1.2 Functions and Specifications for R8C/23 Group revised. NOTE1 deleted.
		5	Table 1.3 Product Information for R8C/22 Group; "R5F2122AJFP (D)", "R5F2122CJFP (D)", "R5F2122AKFP (D)", "R5F2122CKFP (D)", and NOTE added. Figure 1.2 Type Number, Memory Size, and Package of R8C/22 Group; "A: 96 KB" and "C: 128 KB" added.
		6	Table 1.4 Product Information for R8C/23 Group; "R5F2123AJFP (D)", "R5F2123CJFP (D)", "R5F2123AKFP (D)", "R5F2123CKFP (D)", and NOTE added. Figure 1.3 Type Number, Memory Size, and Package of R8C/23 Group; "A: 96 KB" and "C: 128 KB" added.
		13	Figure 3.1 Memory Map of R8C/22 Group revised.
		14	Figure 3.2 Memory Map of R8C/23 Group revised.
		15	Table 4.1 SFR Information (1) ⁽¹⁾ ; NOTE8; "The CSPROINI bit in the OFS register is set to 0." → "The CSPROINI bit in the OFS register is 0." revised.
		28	Table 5.1 Absolute Maximum Ratings; Power dissipation revised. Table 5.2 Recommended Operating Conditions; System clock revised.
		33	Table 5.8 Voltage Monitor 1 Reset Circuit Electrical Characteristics → Table 5.8 Power-on Reset Circuit, Voltage Monitor 1 Reset Circuit Electrical Characteristics ⁽¹⁾ replaced. Table 5.8 revised. NOTE3 added. Table 5.9 Power-on Reset Circuit Electrical Characteristics deleted. Figure 5.3 Power-on Reset Circuit Electrical Characteristics revised.
		34	Table 5.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics → Table 5.9 High-Speed On-Chip Oscillator Circuit Electrical Characteristics revised.

Notes:

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