Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21236kfp-w4

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

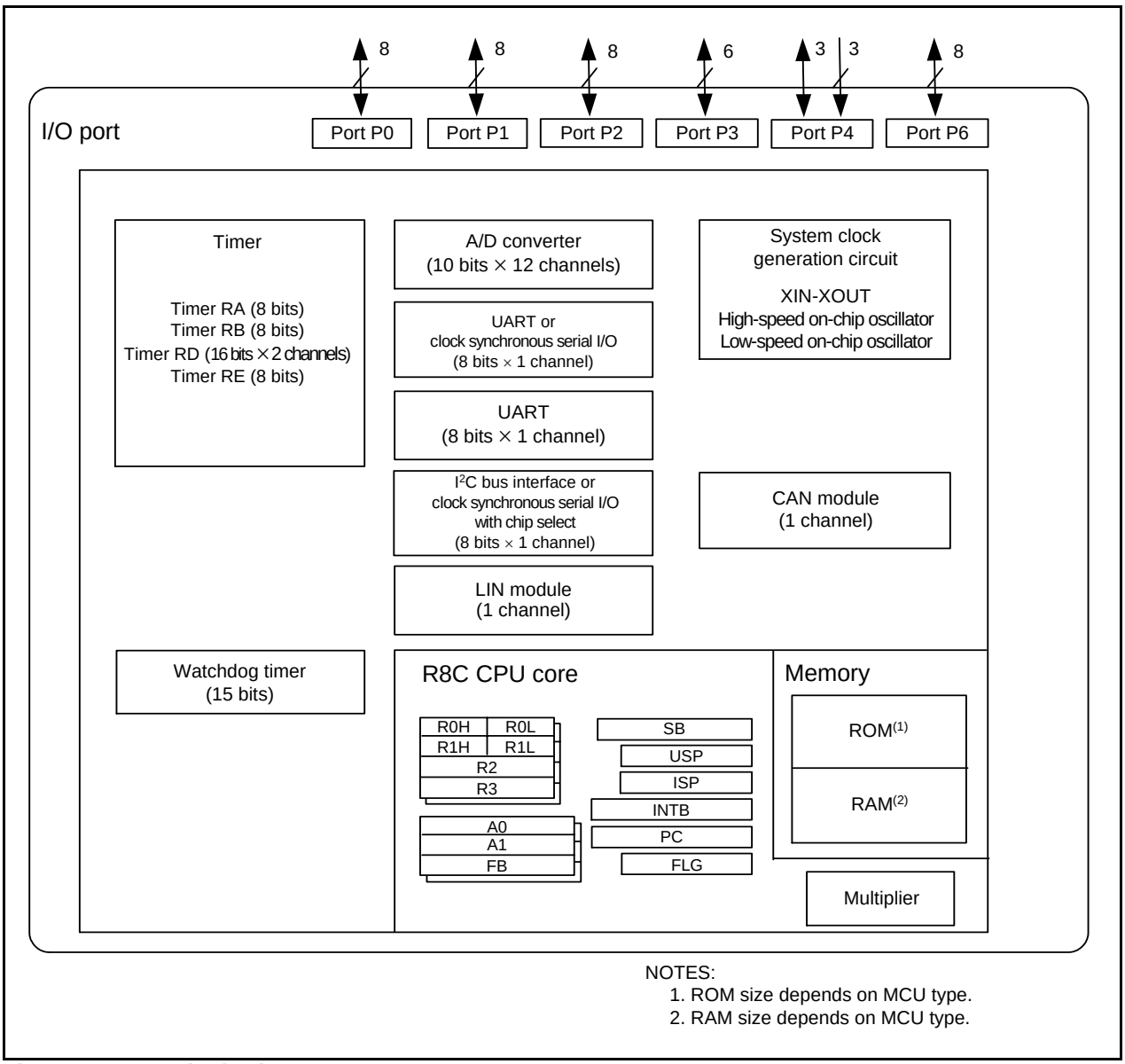
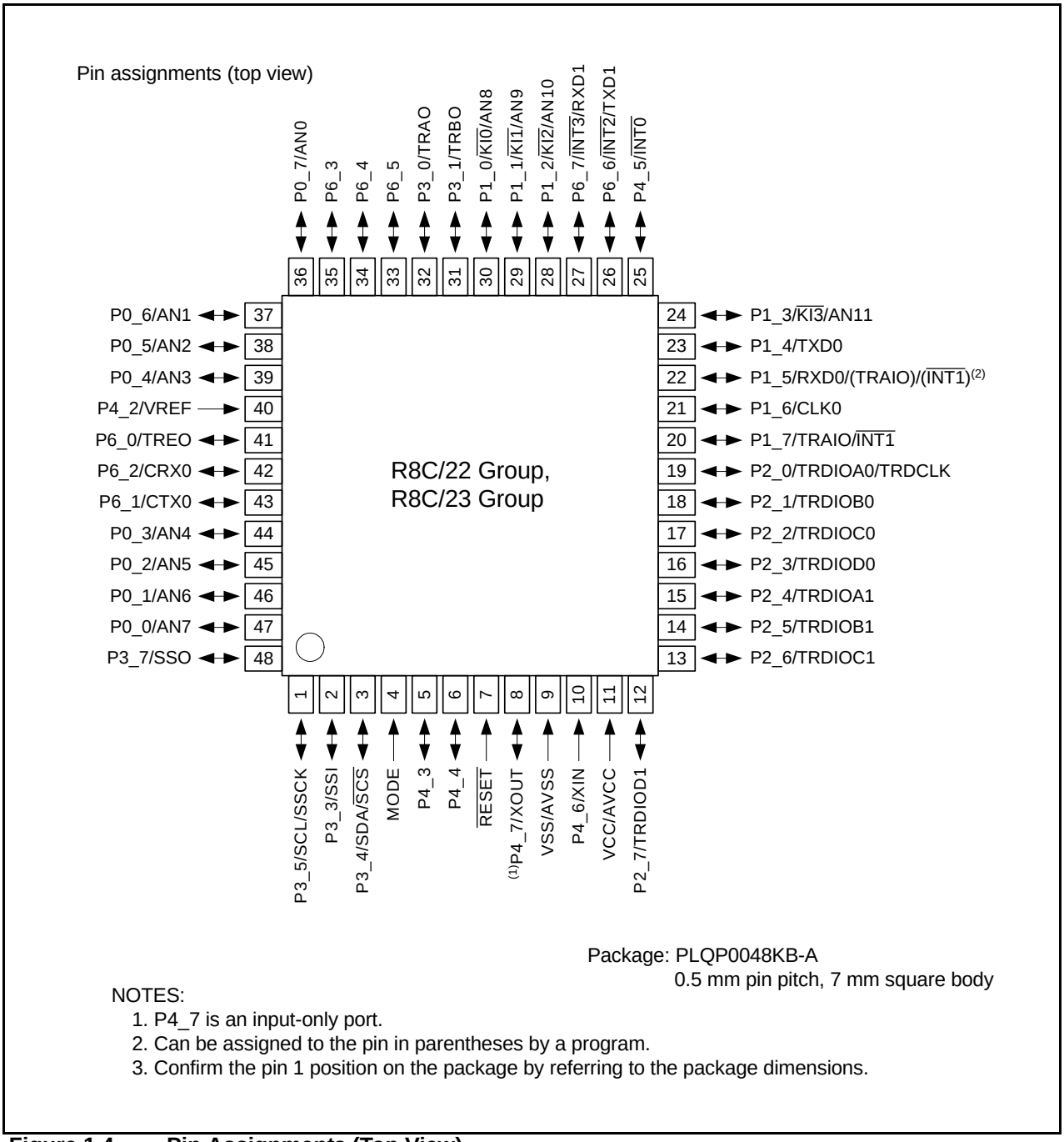


Figure 1.1 Block Diagram

1.5 Pin Assignments

Figure 1.4 shows Pin Assignments (Top View).



NOTES:
1. P4_7 is an input-only port.
2. Can be assigned to the pin in parentheses by a program.
3. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.4 Pin Assignments (Top View)

1.6 Pin Functions

Table 1.5 lists the Pin Functions and Table 1.6 lists the Pin Name Information by Pin Number.

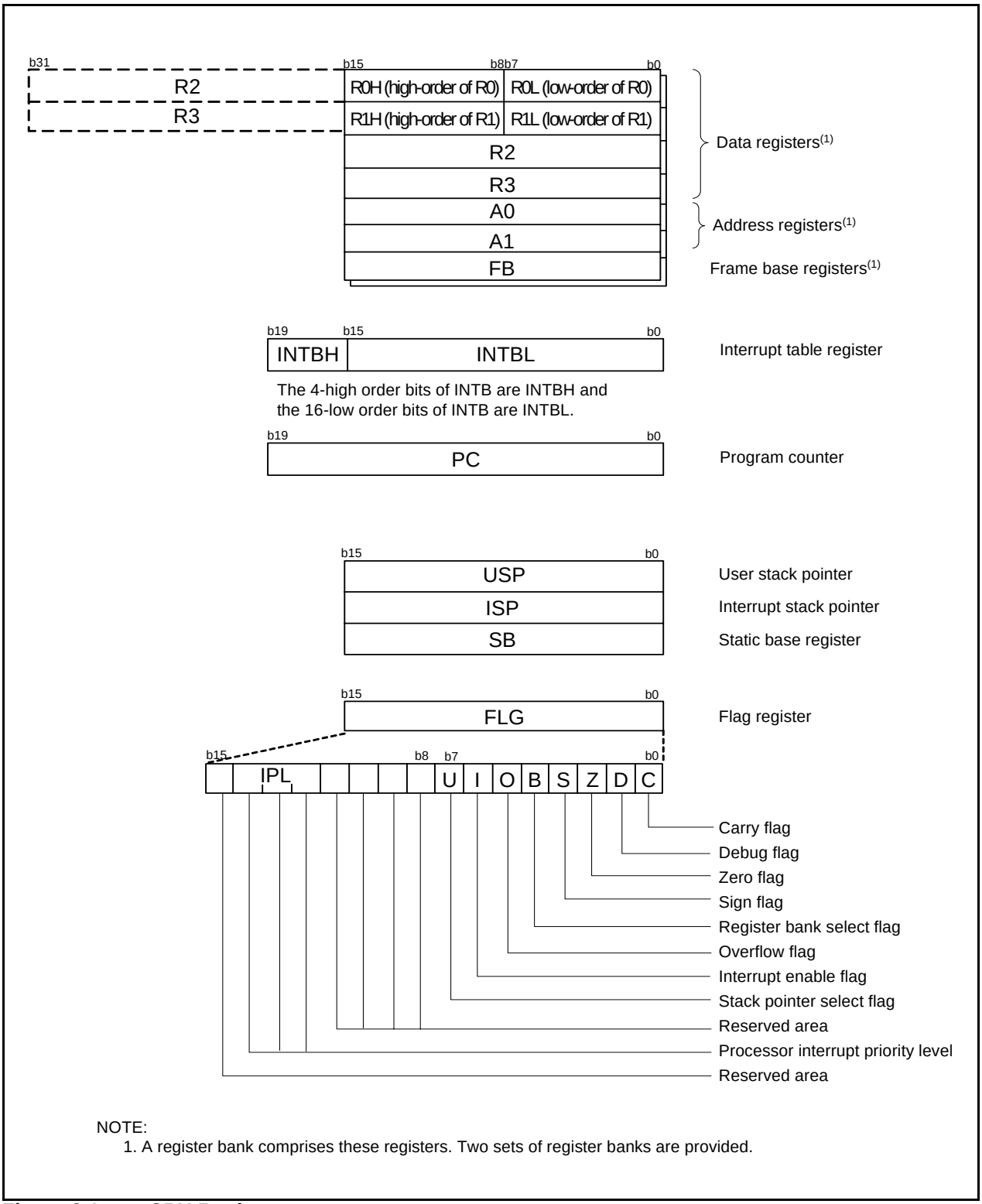
Table 1.5 Pin Functions

Type	Symbol	I/O Type	Description
Power Supply Input	VCC VSS	I	Apply 2.7 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog Power Supply Input	AVCC, AVSS	I	Applies the power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset Input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN Clock Input	XIN	I	These pins are provided for the XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
XIN Clock Output	XOUT	O	
$\overline{\text{INT}}$ Interrupt Input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ Timer RD input pins. $\overline{\text{INT1}}$ Timer RA input pins.
Key Input Interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins.
Timer RA	TRAIO	I/O	Timer RA I/O pin.
	TRAO	O	Timer RA output pin.
Timer RB	TRBO	O	Timer RB output pin.
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O ports.
	TRDCLK	I	External clock input pin.
Timer RE	TREO	O	Divided clock output pin.
Serial Interface	CLK0	I/O	Transfer clock I/O pin.
	RXD0, RXD1	I	Serial data input pins.
	TXD0, TXD1	O	Serial data output pins.
I^2C Bus Interface	SCL	I/O	Clock I/O pin.
	SDA	I/O	Data I/O pin.
Clock Synchronous Serial I/O with Chip Select	SSI	I/O	Data I/O pin.
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
CAN Module	CRX0	I	CAN data input pin.
	CTX0	O	CAN data output pin.
Reference Voltage Input	VREF	I	Reference voltage input pin to A/D converter.
A/D Converter	AN0 to AN11	I	Analog input pins to A/D converter.
I/O Port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5, P6_0 to P6_7	I/O	CMOS I/O ports. Each port contains an input/output select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by a program.
Input Port	P4_2, P4_6, P4_7	I	Input only ports.

I: Input O: Output I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. Of these, R0, R1, R2, R3, A0, A1, and FB comprise a register bank. Two sets of register banks are provided.



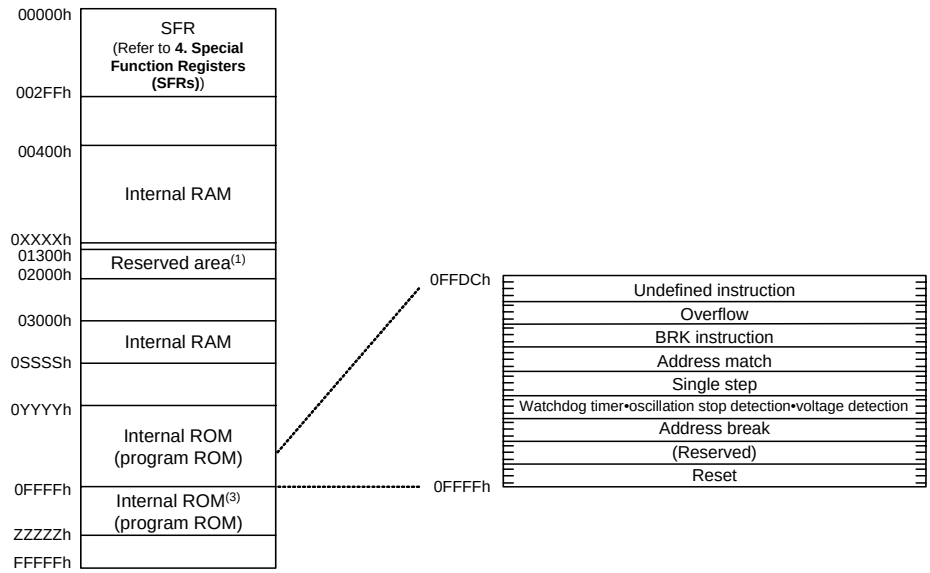
NOTE:
1. A register bank comprises these registers. Two sets of register banks are provided.

Figure 2.1 CPU Registers

3. Memory

3.1 R8C/22 Group

Figure 3.1 shows a Memory Map of R8C/22 Group. The R8C/22 Group has 1 Mbyte of address space from address 00000h to FFFFFh.
The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFR) are allocated addresses 00000h to 002FFh and 01300h to 0147Fh (SFR area for CAN). The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future user and cannot be accessed by users.



NOTES:
1. SFR area for CAN is allocated addresses 01300h to 0147Fh.
2. The blank regions are reserved. Do not access locations in these regions.
3. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **24. Notes on Emulator Debugger**.

Part Number	Internal ROM			Internal RAM		
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh	Address 0SSSSh
R5F21226DFP, R5F21226JFP, R5F21226KFP	32 Kbytes	08000h	-	2 Kbytes	00BFFh	-
R5F21227DFP, R5F21227JFP, R5F21227KFP	48 Kbytes	04000h	-	2.5 Kbytes	00DFFh	-
R5F21228DFP, R5F21228JFP, R5F21228KFP	64 Kbytes	04000h	13FFFh	3 Kbytes	00FFFh	-
R5F2122AJFP, R5F2122AKFP	96 Kbytes	04000h	1BFFFh	5 Kbytes	00FFFh	037FFh
R5F2122CJFP, R5F2122CKFP	128 Kbytes	04000h	23FFFh	6 Kbytes	00FFFh	03BFFh

Figure 3.1 Memory Map of R8C/22 Group

Table 4.4 SFR Information (4)(1)

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h			XXh
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Control Register 2	ADCON2	00h
00D5h			
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h	UART1 Function Select Register	U1SR	XXh
00F6h			
00F7h			
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	XX00XX00b
00FEh			
00FFh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.5 SFR Information (5)(1)

Address	Register	Symbol	After reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Counter Data Register	TRESEC	00h
0119h	Timer RE Compare Data Register	TREMIN	00h
011Ah			
011Bh			
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h			
0121h			
0122h			
0123h			
0124h			
0125h			
0126h			
0127h			
0128h			
0129h			
012Ah			
012Bh			
012Ch			
012Dh			
012Eh			
012Fh			
0130h			
0131h			
0132h			
0133h			
0134h			
0135h			
0136h			
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.6 SFR Information (6)(1)

Address	Register	Symbol	After reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIORA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIORA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.11 SFR Information (11)(1)

Address	Register	Symbol	After reset
13C0h	CAN0 Slot 6: Identifier/DLC		XXh
13C1h			XXh
13C2h			XXh
13C3h			XXh
13C4h			XXh
13C5h			XXh
13C6h	CAN0 Slot 6: Data Field		XXh
13C7h			XXh
13C8h			XXh
13C9h			XXh
13CAh			XXh
13CBh			XXh
13CCh			XXh
13CDh			XXh
13CEh	CAN0 Slot 6: Time Stamp		XXh
13CFh			XXh
13D0h	CAN0 Slot 7: Identifier/DLC		XXh
13D1h			XXh
13D2h			XXh
13D3h			XXh
13D4h			XXh
13D5h			XXh
13D6h	CAN0 Slot 7: Data Field		XXh
13D7h			XXh
13D8h			XXh
13D9h			XXh
13DAh			XXh
13DBh			XXh
13DCh			XXh
13DDh			XXh
13DEh	CAN0 Slot 7: Time Stamp		XXh
13DFh			XXh
13E0h	CAN0 Slot 8: Identifier/DLC		XXh
13E1h			XXh
13E2h			XXh
13E3h			XXh
13E4h			XXh
13E5h			XXh
13E6h	CAN0 Slot 8: Data Field		XXh
13E7h			XXh
13E8h			XXh
13E9h			XXh
13EAh			XXh
13EBh			XXh
13ECh			XXh
13EDh			XXh
13EEh	CAN0 Slot 8: Time Stamp		XXh
13EFh			XXh
13F0h	CAN0 Slot 9: Identifier/DLC		XXh
13F1h			XXh
13F2h			XXh
13F3h			XXh
13F4h			XXh
13F5h			XXh
13F6h	CAN0 Slot 9: Data Field		XXh
13F7h			XXh
13F8h			XXh
13F9h			XXh
13FAh			XXh
13FBh			XXh
13FCh			XXh
13FDh			XXh
13FEh	CAN0 Slot 9: Time Stamp		XXh
13FFh			XXh

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.13 SFR Information (13)(1)

Address	Register	Symbol	After reset
1440h	CAN0 Slot 14: Identifier/DLC		XXh
1441h			XXh
1442h			XXh
1443h			XXh
1444h			XXh
1445h			XXh
1446h	CAN0 Slot 14: Data Field		XXh
1447h			XXh
1448h			XXh
1449h			XXh
144Ah			XXh
144Bh			XXh
144Ch			XXh
144Dh			XXh
144Eh	CAN0 Slot 14: Time Stamp		XXh
144Fh			XXh
1450h	CAN0 Slot 15: Identifier/DLC		XXh
1451h			XXh
1452h			XXh
1453h			XXh
1454h			XXh
1455h			XXh
1456h	CAN0 Slot 15: Data Field		XXh
1457h			XXh
1458h			XXh
1459h			XXh
145Ah			XXh
145Bh			XXh
145Ch			XXh
145Dh			XXh
145Eh	CAN0 Slot 15: Time Stamp		XXh
145Fh			XXh
1460h	CAN0 Global Mask Register	C0GMR	XXh
1461h			XXh
1462h			XXh
1463h			XXh
1464h			XXh
1465h			XXh
1466h	CAN0 Local Mask A Register	C0LMAR	XXh
1467h			XXh
1468h			XXh
1469h			XXh
146Ah			XXh
146Bh			XXh
146Ch	CAN0 Local Mask B Register	C0LMBR	XXh
146Dh			XXh
146Eh			XXh
146Fh			XXh
1470h			XXh
1471h			XXh
1472h			
1473h			
1474h			
1475h			

FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V_{CC}/AV_{CC}	Supply voltage		-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC}+0.3	V
V_O	Output voltage		-0.3 to V_{CC}+0.3	V
P_d	Power dissipation	-40°C ≤ Topr ≤ 85°C	300	mW
		85°C < Topr ≤ 125°C	125	mW
T_{opr}	Operating ambient temperature		-40 to 85 (D, J version) / -40 to 125 (K version)	°C
T_{stg}	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage			2.7	–	5.5	V
V_{SS}/AV_{CC}	Supply voltage			–	0	–	V
V_{IH}	Input “H” voltage			0.8V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” voltage			0	–	0.2V_{CC}	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all Pins $I_{OH\ (peak)}$		–	–	-60	mA
$I_{OH(peak)}$	Peak output “H” current			–	–	-10	mA
$I_{OH(avg)}$	Average output “H” current			–	–	-5	mA
$I_{OL(sum)}$	Peak sum output “L” currents	Sum of all Pins $I_{OL\ (peak)}$		–	–	60	mA
$I_{OL(peak)}$	Peak output “L” currents			–	–	10	mA
$I_{OL(avg)}$	Average output “L” current			–	–	5	mA
$f_{(XIN)}$	XIN clock input oscillation frequency		3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	0	–	20	MHz
			3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 125°C	0	–	16	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
–	System clock	OCD2 = 0 When XIN clock is selected.	3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	0	–	20	MHz
			3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 125°C	0	–	16	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
		OCD2 = 1 When on-chip oscillator clock is selected.	FRA01 = 0 When low-speed on-chip oscillator clock is selected.	–	125	–	kHz
			FRA01 = 1 When high-speed on-chip oscillator clock is selected. 3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	–	–	20	MHz
			FRA01 = 1 When high-speed on-chip oscillator clock is selected.	–	–	10	MHz

NOTES:
1. V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.12 Timing Requirements of Clock Synchronous Serial I/O with Chip Select(1)

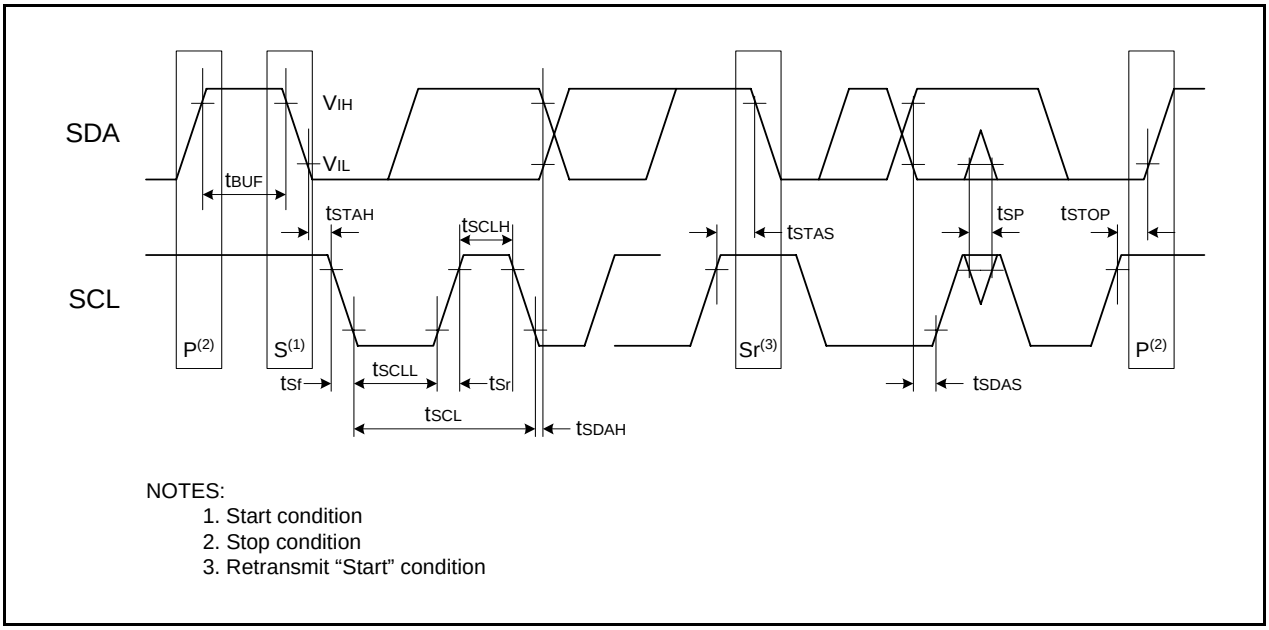
Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	–	t_{CYC}(2)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_H	SSO, SSI data input hold time			1	–	–	t_{CYC}(2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1	t_{CYC}(2)
t_{SA}	SSI slave access time			–	–	1t_{CYC} + 100	ns
t_{OR}	SSI slave out open time			–	–	1t_{CYC} + 100	ns

NOTES:
1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. 1t_{CYC} = 1/f1(s)

Table 5.13 Timing Requirements of I²C Bus Interface(1)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC}$ + 600(2)	–	–	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC}$ + 300(2)	–	–	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC}$ + 500(2)	–	–	ns
t_{sf}	SCL, SDA input falling time		–	–	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		–	–	$1t_{CYC}$(2)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$(2)	–	–	ns
t_{STAH}	Start condition input hole time		$3t_{CYC}$(2)	–	–	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{SOAS}	Data input setup time		$1t_{CYC}$ + 20(2)	–	–	ns
t_{SDAH}	Data input hold time		0	–	–	ns

NOTES:
1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. $1t_{CYC}$ = 1/f1(s)



NOTES:
1. Start condition
2. Stop condition
3. Retransmit “Start” condition

Figure 5.7 I/O Timing of I²C Bus Interface

Table 5.14 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” Voltage	Except XOUT	I_{OH} = -5 mA		Vcc – 2.0	–	Vcc	V
			I_{OH} = -200 μA		Vcc – 0.3	–	Vcc	V
		XOUT	Drive capacity HIGH	I_{OH} = -1 mA	Vcc – 2.0	–	Vcc	V
			Drive capacity LOW	I_{OH} = -500 μA	Vcc – 2.0	–	Vcc	V
V_{OL}	Output “L” Voltage	Except XOUT	I_{OL} = 5 mA		–	–	2.0	V
			I_{OL} = 200 μA		–	–	0.45	V
		XOUT	Drive capacity HIGH	I_{OL} = 1 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 500 μA	–	–	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, SSI, SCL, SDA, SSO			0.1	0.5	–	V
		$\overline{RESET}$			0.1	1.0	–	V
I_{IH}	Input “H” current		VI = 5 V, Vcc = 5 V		–	–	5.0	μA
I_{IL}	Input “L” current		VI = 0 V, Vcc = 5 V		–	–	-5.0	μA
R_{PULLUP}	Pull-Up Resistance		VI = 0 V, Vcc = 5 V		30	50	167	kΩ
R_{fXIN}	Feedback Resistance	XIN			–	1.0	–	MΩ
V_{RAM}	RAM Hold Voltage		During stop mode		2.0	–	–	V

NOTE:
1. Vcc = 4.2 to 5.5 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.21 Electrical Characteristics (4) [Vcc = 3 V]
(Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), Unless Otherwise Specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.7 to 3.3 V) In single-chip mode, the output pins are open and other pins are Vss	High-clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	11.5	23.0	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	9.5	19.0	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6.0	12.0	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	5.5	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	4.5	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	6.3	12.6	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.1	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 FMR47 = 1	–	145	290	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA20 = 0 VCA26 = VCA27 = 0	–	56	112	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA20 = 0 VCA26 = VCA27 = 0	–	35	70	µA
		Stop mode Topr = 25°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	0.7	3.0	µA
		Stop mode Topr = 85°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	1.1	–	µA
		Stop mode Topr = 125°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	3.8	–	µA

Timing Requirements (Unless Otherwise Specified: Vcc = 3 V, Vss = 0V at Topr = 25°C) [Vcc = 3 V]

Table 5.22 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns

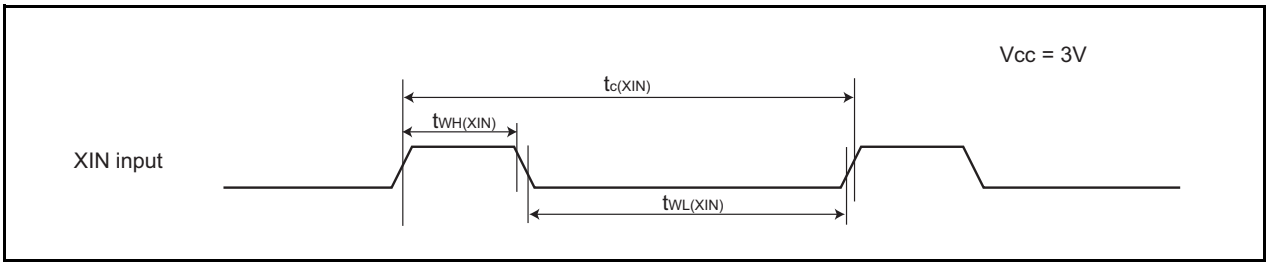


Figure 5.12 XIN Input Timing Diagram when Vcc = 3 V

Table 5.23 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input Cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

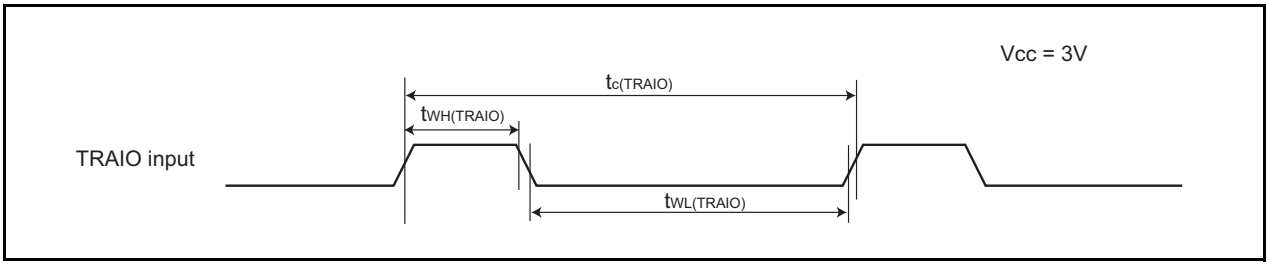


Figure 5.13 TRAIO Input Timing Diagram when Vcc = 3 V

Table 5.24 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	300	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	150	–	ns
$t_{W(CKL)}$	CLK0 input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

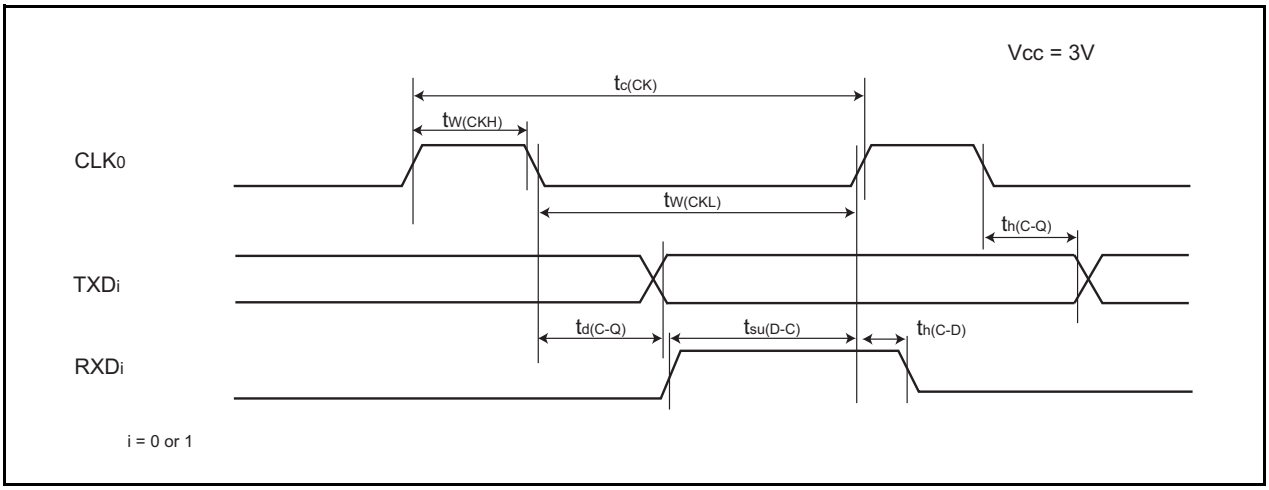


Figure 5.14 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.25 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input HIGH width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input LOW width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.

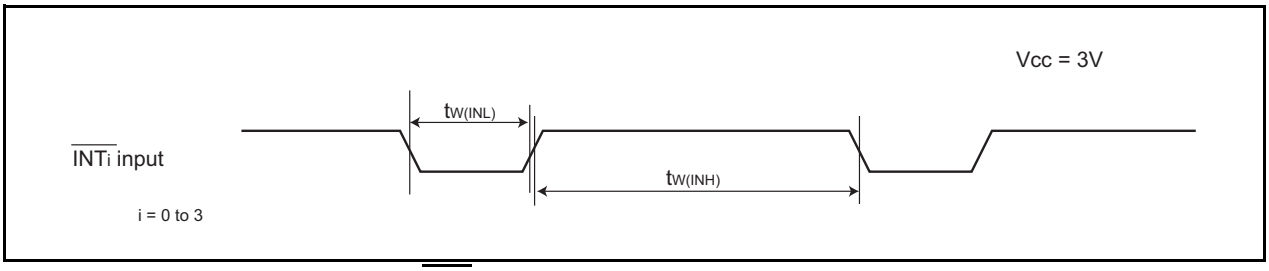
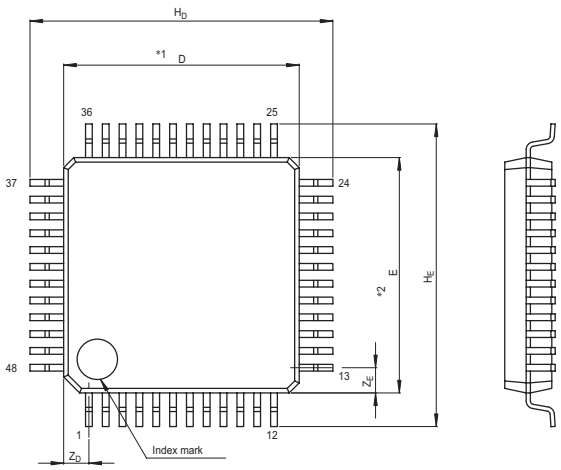


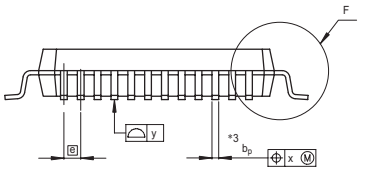
Figure 5.15 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 3 V (i = 0 to 3)

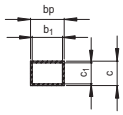
Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

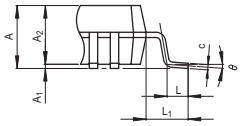
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g







Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

REVISION HISTORY	R8C/22 Group, R8C/23 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Oct 27, 2006	40	Table 5.15 Electrical Characteristics (1) [VCC = 5 V] → Table 5.14 Electrical Characteristics (1) [VCC = 5 V] revised. RAM Hold Voltage, Min.; "1.8" → "2.0" corrected.
		41	Table 5.16 Electrical Characteristics (2) [Vcc = 5 V] → Table 5.15 Electrical Characteristics (2) [Vcc = 5 V] revised. Wait mode revised.
		44	Table 5.21 Electrical Characteristics (3) [VCC = 3 V → Table 5.20 Electrical Characteristics (3) [VCC = 3 V] revised. RAM hold voltage, Min.; "1.8" → "2.0" corrected.
		45	Table 5.22 Electrical Characteristics (4) [Vcc = 3 V] → Table 5.21 Electrical Characteristics (4) [Vcc = 3 V] revised. Wait mode revised.
1.10	Mar 16, 2007	–	D version products added. Relevant descriptions revised because of expanding products - Table 1.1 to 1.4 revised. - Figure 1.2 and 1.3 revised. - Figure 3.1 and 3.2 revised. - Table 5.1 to 5.15 revised. - Table 5.20 and 5.21 revised.
		15	Table 4.1 revised; 000Ah: "00XXX000b" → "00h", 000Fh: "00011111b" → "00X11111b"
		42	Table 5.17 and Figure 5.9 revised; "$\overline{\text{INT1}}$ input" deleted
		43	Table 5.19 and Figure 5.11 revised; "i = 0, 2, 3" → "i = 0 to 3"
		46	Table 5.23 and Figure 5.13 revised; "$\overline{\text{INT1}}$ input" deleted
		47	Table 5.25 and Figure 5.15 revised; "i = 0, 2, 3" → "i = 0 to 3"
2.00	Aug 20, 2008	–	"RENESAS TECHNICAL UPDATE" reflected: TN-16C-A172A/E
		5, 6	Table 1.3, Table 1.4 revised Figure 1.2, Figure 1.3; ROM number "XXX" added
		13, 14	Figure 3.1, Figure 3.2; "Expanding area" deleted
		23	Table 4.9 135Fh Address "XXXX0000b" → "00h"
		28	Table 5.2; NOTE2 revised
		30	Table 5.4; NOTE2 and NOTE4 revised
		31	Table 5.5; NOTE2 and NOTE5 revised
		32	Table 5.6; "td(Vdet1-A)" added, NOTE5 added Table 5.7; "td(Vdet2-A)" and NOTE2 revised, NOTE5 added
		33	Table 5.8; "trth" and NOTE2 revised, Figure 5.3 revised