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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21237jfp-u1

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1. Overview

This MCU is built using the high-performance silicon gate CMOS process using the R8C CPU core and is packaged in a 48-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1 Mbyte of address space, it is capable of executing instructions at high speed. This MCU is equipped with one CAN module and suited to in-vehicle or FA networking.
Furthermore, the data flash (1 KB x 2 blocks) is embedded in the R8C/23 Group.
The difference between R8C/22 and R8C/23 Groups is only the existence of the data flash. Their peripheral functions are the same.

1.1 Applications

Automotive, etc.

1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/22 Group and Table 1.2 outlines the Functions and Specifications for R8C/23 Group.

Table 1.1 Functions and Specifications for R8C/22 Group

Item		Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to **Table 1.3 Product Information for R8C/22 Group**
Peripheral Function	Ports	I/O ports: 41 pins, Input port: 3 pins
	Timers	Timer RA: 8 bits x 1 channel, Timer RB: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer RD: 16 bits x 2 channel (Circuits of input capture and output compare) Timer RE: With compare match function
	Serial interface	1 channel (UART0) Clock synchronous I/O, UART 1 channel (UART1) UART
	Clock synchronous serial interface	1 channel I2C bus interface(2), Clock synchronous serial I/O with chip select
	LIN module	Hardware LIN: 1 channel (timer RA, UART0)
	CAN module	1 channel with 2.0B specification: 16 slots
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer	15 bits x 1 channel (with prescaler) Reset start selectable
	Interrupt	Internal: 14 sources, External: 6 sources, Software: 4 sources, Priority level: 7 levels
	Clock generation circuits	2 circuits XIN clock generation circuit (with on-chip feedback resistor) On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has frequency adjustment function.
	Oscillation stop detection function	Stop detection of XIN clock oscillation
	Voltage detection circuit	On-chip
	Power-on reset circuit include	On-chip
Electric Characteristics	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz)(D, J version) VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz)(K version) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)
	Current consumption	Typ. 12.5 mA (VCC = 5 V, f(XIN) = 20 MHz, High-speed on-chip oscillator stopping) Typ. 6.0 mA (VCC = 5 V, f(XIN) = 10 MHz, High-speed on-chip oscillator stopping)
Flash Memory	Programming and erasure voltage	VCC = 2.7 to 5.5 V
	Programming and erasure endurance	100 times
Operating Ambient Temperature		-40 to 85°C
		-40 to 125°C (option(1))
Package		48-pin mold-plastic LQFP

NOTES:
1. When using options, be sure to inquire about the specification.
2. I2C bus is a registered trademark of Koninklijke Philips Electronics N.V.

1.4 Product Information

Table 1.3 lists Product Information for R8C/22 Group and Table 1.4 lists Product Information for R8C/23 Group.

Table 1.3 Product Information for R8C/22 Group **Current of Aug. 2008**

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks	
R5F21226DFP	32 Kbytes	2 Kbytes	PLQP0048KB-A	D version	Flash memory version
R5F21227DFP	48 Kbytes	2.5 Kbytes	PLQP0048KB-A		
R5F21228DFP	64 Kbytes	3 Kbytes	PLQP0048KB-A		
R5F21226JFP	32 Kbytes	2 Kbytes	PLQP0048KB-A	J version	
R5F21227JFP	48 Kbytes	2.5 Kbytes	PLQP0048KB-A		
R5F21228JFP	64 Kbytes	3 Kbytes	PLQP0048KB-A		
R5F2122AJFP	96 Kbytes	5 Kbytes	PLQP0048KB-A		
R5F2122CJFP	128 Kbytes(1)	6 Kbytes	PLQP0048KB-A		
R5F21226KFP	32 Kbytes	2 Kbytes	PLQP0048KB-A	K version	
R5F21227KFP	48 Kbytes	2.5 Kbytes	PLQP0048KB-A		
R5F21228KFP	64 Kbytes	3 Kbytes	PLQP0048KB-A		
R5F2122AKFP	96 Kbytes	5 Kbytes	PLQP0048KB-A		
R5F2122CKFP	128 Kbytes(1)	6 Kbytes	PLQP0048KB-A		

NOTE:
1. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **24. Notes on Emulator Debugger** of Hardware Manual.

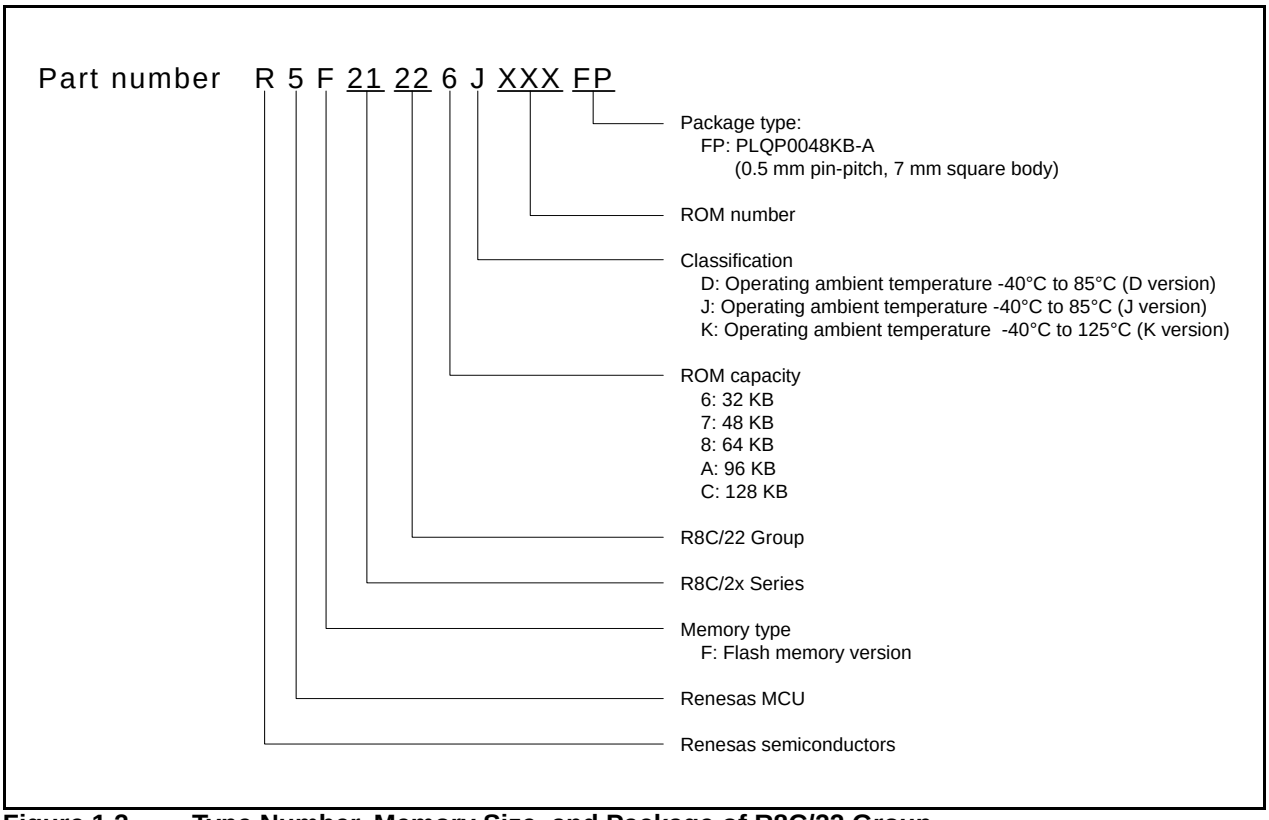


Figure 1.2 Type Number, Memory Size, and Package of R8C/22 Group

Table 1.4 Product Information for R8C/23 Group **Current of Aug. 2008**

Type No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data Flash				
R5F21236DFP	32 Kbytes	1 Kbyte X 2	2 Kbytes	PLQP0048KB-A	D version	Flash memory version
R5F21237DFP	48 Kbytes	1 Kbyte X 2	2.5 Kbytes	PLQP0048KB-A		
R5F21238DFP	64 Kbytes	1 Kbyte X 2	3 Kbytes	PLQP0048KB-A		
R5F21236JFP	32 Kbytes	1 Kbyte X 2	2 Kbytes	PLQP0048KB-A	J version	
R5F21237JFP	48 Kbytes	1 Kbyte X 2	2.5 Kbytes	PLQP0048KB-A		
R5F21238JFP	64 Kbytes	1 Kbyte X 2	3 Kbytes	PLQP0048KB-A		
R5F2123AJFP	96 Kbytes	1 Kbyte X 2	5 Kbytes	PLQP0048KB-A		
R5F2123CJFP	128 Kbytes(1)	1 Kbyte X 2	6 Kbytes	PLQP0048KB-A		
R5F21236KFP	32 Kbytes	1 Kbyte X 2	2 Kbytes	PLQP0048KB-A	K version	
R5F21237KFP	48 Kbytes	1 Kbyte X 2	2.5 Kbytes	PLQP0048KB-A		
R5F21238KFP	64 Kbytes	1 Kbyte X 2	3 Kbytes	PLQP0048KB-A		
R5F2123AKFP	96 Kbytes	1 Kbyte X 2	5 Kbytes	PLQP0048KB-A		
R5F2123CKFP	128 Kbytes(1)	1 Kbyte X 2	6 Kbytes	PLQP0048KB-A		

NOTE:
1. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **24. Notes on Emulator Debugger** of Hardware Manual.

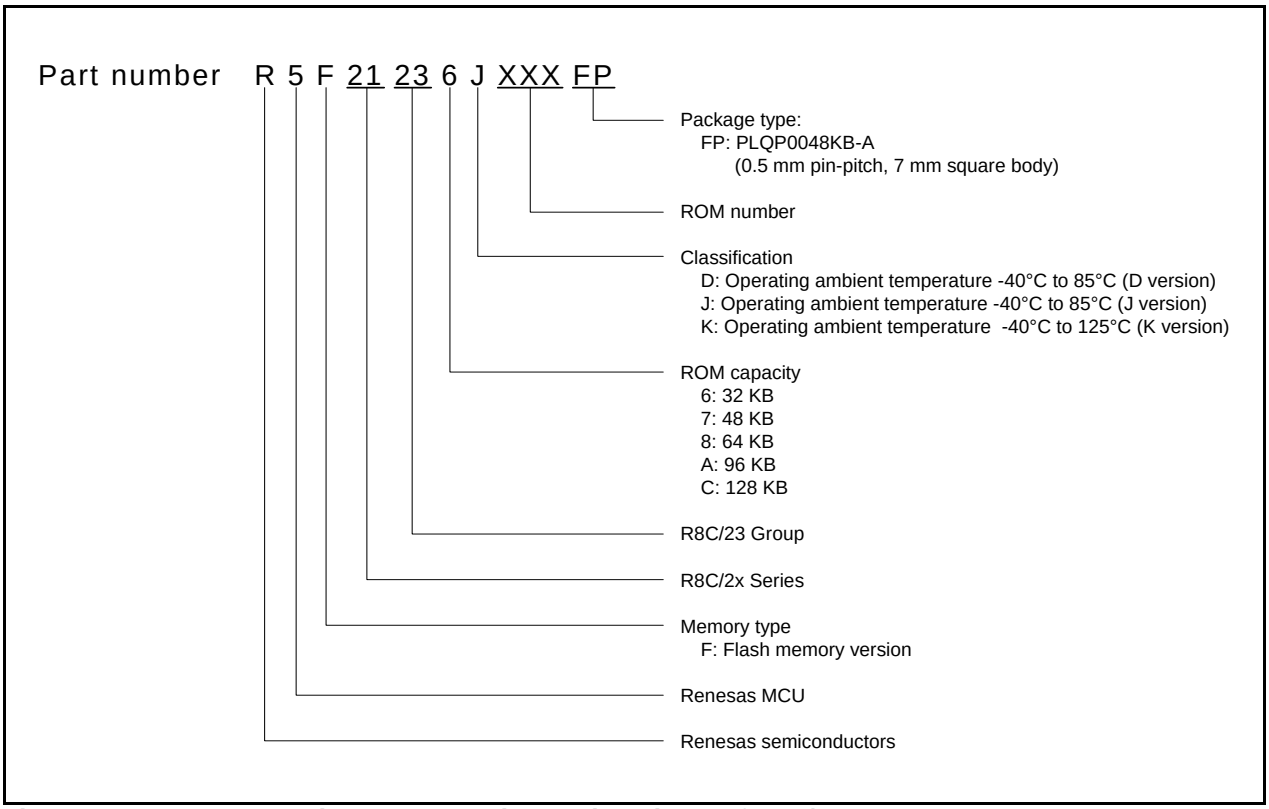


Figure 1.3 Type Number, Memory Size, and Package of R8C/23 Group

1.6 Pin Functions

Table 1.5 lists the Pin Functions and Table 1.6 lists the Pin Name Information by Pin Number.

Table 1.5 Pin Functions

Type	Symbol	I/O Type	Description
Power Supply Input	VCC VSS	I	Apply 2.7 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog Power Supply Input	AVCC, AVSS	I	Applies the power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset Input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN Clock Input	XIN	I	These pins are provided for the XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
XIN Clock Output	XOUT	O	
$\overline{\text{INT}}$ Interrupt Input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ Timer RD input pins. $\overline{\text{INT1}}$ Timer RA input pins.
Key Input Interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins.
Timer RA	TRAIO	I/O	Timer RA I/O pin.
	TRAO	O	Timer RA output pin.
Timer RB	TRBO	O	Timer RB output pin.
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O ports.
	TRDCLK	I	External clock input pin.
Timer RE	TREO	O	Divided clock output pin.
Serial Interface	CLK0	I/O	Transfer clock I/O pin.
	RXD0, RXD1	I	Serial data input pins.
	TXD0, TXD1	O	Serial data output pins.
I^2C Bus Interface	SCL	I/O	Clock I/O pin.
	SDA	I/O	Data I/O pin.
Clock Synchronous Serial I/O with Chip Select	SSI	I/O	Data I/O pin.
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
CAN Module	CRX0	I	CAN data input pin.
	CTX0	O	CAN data output pin.
Reference Voltage Input	VREF	I	Reference voltage input pin to A/D converter.
A/D Converter	AN0 to AN11	I	Analog input pins to A/D converter.
I/O Port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5, P6_0 to P6_7	I/O	CMOS I/O ports. Each port contains an input/output select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by a program.
Input Port	P4_2, P4_6, P4_7	I	Input only ports.

I: Input O: Output I/O: Input and output

Table 4.2 SFR Information (2)(1)

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h	CAN0 Wake Up Interrupt Control Register	C01WKIC	XXXXX000b
0044h	CAN0 Successful Reception Interrupt Control Register	C0RECIC	XXXXX000b
0045h	CAN0 Successful Transmission Interrupt Control Register	C0TRMIC	XXXXX000b
0046h	CAN0 State/Error Interrupt Control Register	C01ERRIC	XXXXX000b
0047h			
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register/IIC Bus Interrupt Control Register(2)	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.5 SFR Information (5)(1)

Address	Register	Symbol	After reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Counter Data Register	TRESEC	00h
0119h	Timer RE Compare Data Register	TREMIN	00h
011Ah			
011Bh			
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h			
0121h			
0122h			
0123h			
0124h			
0125h			
0126h			
0127h			
0128h			
0129h			
012Ah			
012Bh			
012Ch			
012Dh			
012Eh			
012Fh			
0130h			
0131h			
0132h			
0133h			
0134h			
0135h			
0136h			
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.7 SFR Information (7)(1)

Address	Register	Symbol	After reset
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01FDh			
01FEh			
01FFh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.10 SFR Information (10)(1)

Address	Register	Symbol	After reset
1380h	CAN0 Slot 2: Identifier/DLC		XXh
1381h			XXh
1382h			XXh
1383h			XXh
1384h			XXh
1385h			XXh
1386h	CAN0 Slot 2: Data Field		XXh
1387h			XXh
1388h			XXh
1389h			XXh
138Ah			XXh
138Bh			XXh
138Ch			XXh
138Dh			XXh
138Eh	CAN0 Slot 2: Time Stamp		XXh
138Fh			XXh
1390h	CAN0 Slot 3: Identifier/DLC		XXh
1391h			XXh
1392h			XXh
1393h			XXh
1394h			XXh
1395h			XXh
1396h	CAN0 Slot 3: Data Field		XXh
1397h			XXh
1398h			XXh
1399h			XXh
139Ah			XXh
139Bh			XXh
139Ch			XXh
139Dh			XXh
139Eh	CAN0 Slot 3: Time Stamp		XXh
139Fh			XXh
13A0h	CAN0 Slot 4: Identifier/DLC		XXh
13A1h			XXh
13A2h			XXh
13A3h			XXh
13A4h			XXh
13A5h			XXh
13A6h	CAN0 Slot 4: Data Field		XXh
13A7h			XXh
13A8h			XXh
13A9h			XXh
13AAh			XXh
13ABh			XXh
13ACh			XXh
13ADh			XXh
13AEh	CAN0 Slot 4: Time Stamp		XXh
13AFh			XXh
13B0h	CAN0 Slot 5: Identifier/DLC		XXh
13B1h			XXh
13B2h			XXh
13B3h			XXh
13B4h			XXh
13B5h			XXh
13B6h	CAN0 Slot 5: Data Field		XXh
13B7h			XXh
13B8h			XXh
13B9h			XXh
13BAh			XXh
13BBh			XXh
13BCh			XXh
13BDh			XXh
13BEh	CAN0 Slot 5: Time Stamp		XXh
13BFh			XXh

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.12 SFR Information (12)(1)

Address	Register	Symbol	After reset
1400h	CAN0 Slot 10: Identifier/DLC		XXh
1401h			XXh
1402h			XXh
1403h			XXh
1404h			XXh
1405h			XXh
1406h	CAN0 Slot 10: Data Field		XXh
1407h			XXh
1408h			XXh
1409h			XXh
140Ah			XXh
140Bh			XXh
140Ch			XXh
140Dh			XXh
140Eh	CAN0 Slot 10: Time Stamp		XXh
140Fh			XXh
1410h	CAN0 Slot 11: Identifier/DLC		XXh
1411h			XXh
1412h			XXh
1413h			XXh
1414h			XXh
1415h			XXh
1416h	CAN0 Slot 11: Data Field		XXh
1417h			XXh
1418h			XXh
1419h			XXh
141Ah			XXh
141Bh			XXh
141Ch			XXh
141Dh			XXh
141Eh	CAN0 Slot 11: Time Stamp		XXh
141Fh			XXh
1420h	CAN0 Slot 12: Identifier/DLC		XXh
1421h			XXh
1422h			XXh
1423h			XXh
1424h			XXh
1425h			XXh
1426h	CAN0 Slot 12: Data Field		XXh
1427h			XXh
1428h			XXh
1429h			XXh
142Ah			XXh
142Bh			XXh
142Ch			XXh
142Dh			XXh
142Eh	CAN0 Slot 12: Time Stamp		XXh
142Fh			XXh
1430h	CAN0 Slot 13: Identifier/DLC		XXh
1431h			XXh
1432h			XXh
1433h			XXh
1434h			XXh
1435h			XXh
1436h	CAN0 Slot 13: Data Field		XXh
1437h			XXh
1438h			XXh
1439h			XXh
143Ah			XXh
143Bh			XXh
143Ch			XXh
143Dh			XXh
143Eh	CAN0 Slot 13: Time Stamp		XXh
143Fh			XXh

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V_{CC}/AV_{CC}	Supply voltage		-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC}+0.3	V
V_O	Output voltage		-0.3 to V_{CC}+0.3	V
P_d	Power dissipation	-40°C ≤ Topr ≤ 85°C	300	mW
		85°C < Topr ≤ 125°C	125	mW
T_{opr}	Operating ambient temperature		-40 to 85 (D, J version) / -40 to 125 (K version)	°C
T_{stg}	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage			2.7	–	5.5	V
V_{SS}/AV_{CC}	Supply voltage			–	0	–	V
V_{IH}	Input “H” voltage			0.8V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” voltage			0	–	0.2V_{CC}	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all Pins $I_{OH\ (peak)}$		–	–	-60	mA
$I_{OH(peak)}$	Peak output “H” current			–	–	-10	mA
$I_{OH(avg)}$	Average output “H” current			–	–	-5	mA
$I_{OL(sum)}$	Peak sum output “L” currents	Sum of all Pins $I_{OL\ (peak)}$		–	–	60	mA
$I_{OL(peak)}$	Peak output “L” currents			–	–	10	mA
$I_{OL(avg)}$	Average output “L” current			–	–	5	mA
$f_{(XIN)}$	XIN clock input oscillation frequency		3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	0	–	20	MHz
			3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 125°C	0	–	16	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
–	System clock	OCD2 = 0 When XIN clock is selected.	3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	0	–	20	MHz
			3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 125°C	0	–	16	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
		OCD2 = 1 When on-chip oscillator clock is selected.	FRA01 = 0 When low-speed on-chip oscillator clock is selected.	–	125	–	kHz
			FRA01 = 1 When high-speed on-chip oscillator clock is selected. 3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	–	–	20	MHz
			FRA01 = 1 When high-speed on-chip oscillator clock is selected.	–	–	10	MHz

NOTES:
1. V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		V_{ref} = AVCC	–	–	10	Bits
–	Absolute Accuracy	10-bit mode	φAD = 10 MHz, V_{ref} = AVCC = 5.0 V	–	–	±3	LSB
		8-bit mode	φAD = 10 MHz, V_{ref} = AVCC = 5.0 V	–	–	±2	LSB
		10-bit mode	φAD = 10 MHz, V_{ref} = AVCC = 3.3 V	–	–	±5	LSB
		8-bit mode	φAD = 10 MHz, V_{ref} = AVCC = 3.3 V	–	–	±2	LSB
R_{ladder}	Resistor ladder		V_{ref} = AVCC	10	–	40	kΩ
t_{conv}	Conversion time	10-bit mode	φAD = 10 MHz, V_{ref} = AVCC = 5.0 V	3.3	–	–	µs
		8-bit mode	φAD = 10 MHz, V_{ref} = AVCC = 5.0 V	2.8	–	–	µs
V_{ref}	Reference voltage			2.7	–	AVCC	V
V_{IA}	Analog input voltage(2)			0	–	AVCC	V
–	A/D operating clock frequency	Without sample & hold		0.25	–	10	MHz
		With sample & hold		1	–	10	MHz

NOTES:
1. VCC = AVCC = 2.7 to 5.5 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. When analog input voltage exceeds reference voltage, A/D conversion result is 3FFh in 10-bit mode, FFh in 8-bit mode.

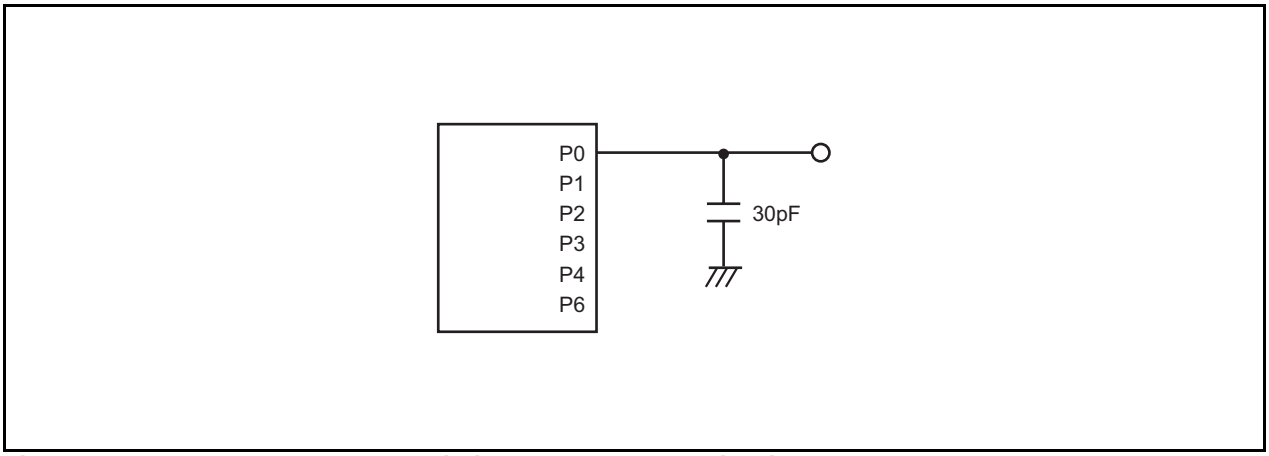


Figure 5.1 Ports P0 to P4, P6 Timing Measurement Circuit

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)	R8C/22 Group	100(3)	–	–	times
		R8C/23 Group	1,000(3)	–	–	times
–	Byte program time		–	50	400	µs
–	Block erase time		–	0.4	9	s
$t_{d(SR-SUS)}$	Time delay from suspend request until erase suspend		–	–	97 + CPU clock × 6 cycle	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3 + CPU clock × 4 cycle	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time(7)	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 1,000), each block can be erased n times.
   For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure endurance can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.9 High-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V_{CC} = 4.75 V to 5.25 V, 0°C ≤ Topr ≤ 60°C(2)	39.2	40	40.8	MHz
		V_{CC} = 3.0 V to 5.25 V, -20°C ≤ Topr ≤ 85°C(2)	38.8	40	41.2	MHz
		V_{CC} = 3.0 V to 5.5 V, -40°C ≤ Topr ≤ 85°C(2)	38.4	40	41.6	MHz
		V_{CC} = 3.0 V to 5.5 V, -40°C ≤ Topr ≤ 125°C(2)	38.0	40	42.0	MHz
		V_{CC} = 2.7 V to 5.5 V, -40°C ≤ Topr ≤ 125°C(2)	37.6	40	42.4	MHz
–	The value of the FRA1 register when the reset is deasserted		08h	40	F7h	–
–	High-speed on-chip oscillator adjustment range	Adjust the FRA1 register to -1 bit (the value when the reset is deasserted)	–	+ 0.3	–	MHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption when high-speed on-chip oscillator oscillating	V_{CC} = 5.0 V, Topr = 25°C	–	600	–	µA

NOTES:
1. V_{CC} = 2.7 V to 5.5 V, Topr = -40°C to 85°C (D, J version) / -40°C to 125°C (K version), unless otherwise specified.
2. The standard value shows when the reset is deasserted for the FRA1 register.

Table 5.10 Low-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		40	125	250	kHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption when low-speed on-chip oscillator oscillating	V_{CC} = 5.0 V, Topr = 25°C	–	15	–	µA

NOTE:
1. V_{CC} = 2.7 V to 5.5 V, Topr = -40°C to 85°C (D, J version) / -40°C to 125°C (K version), unless otherwise specified.

Table 5.11 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP exit time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = 2.7 to 5.5 V and Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until CPU clock supply starts since the interrupt is acknowledged to exit stop mode.

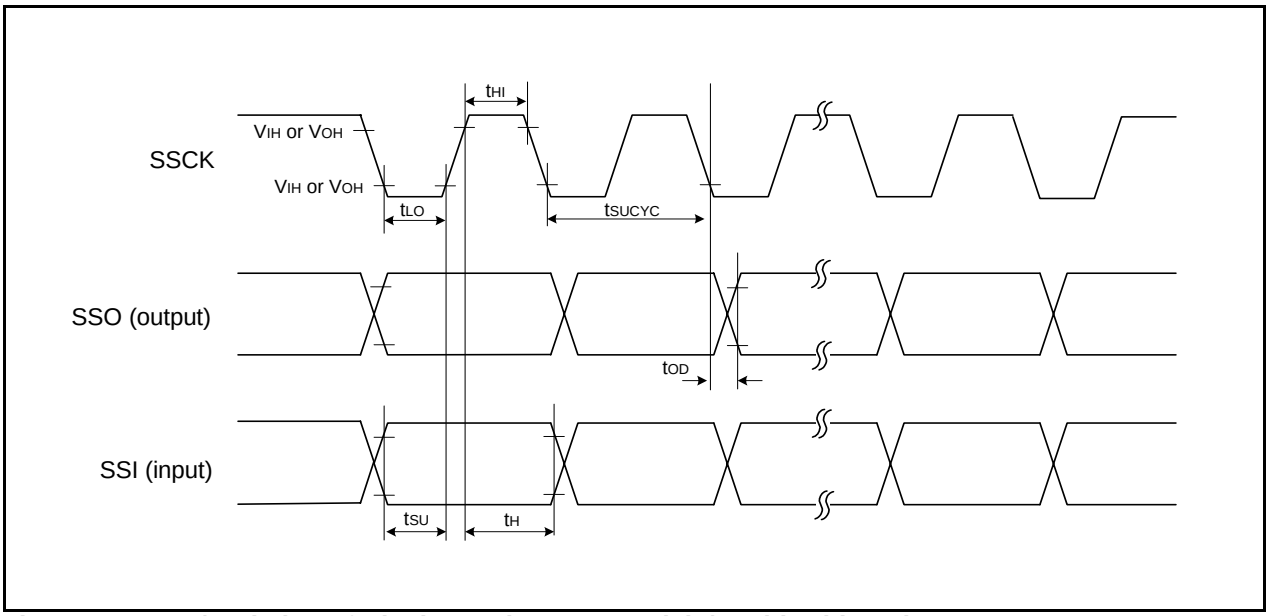
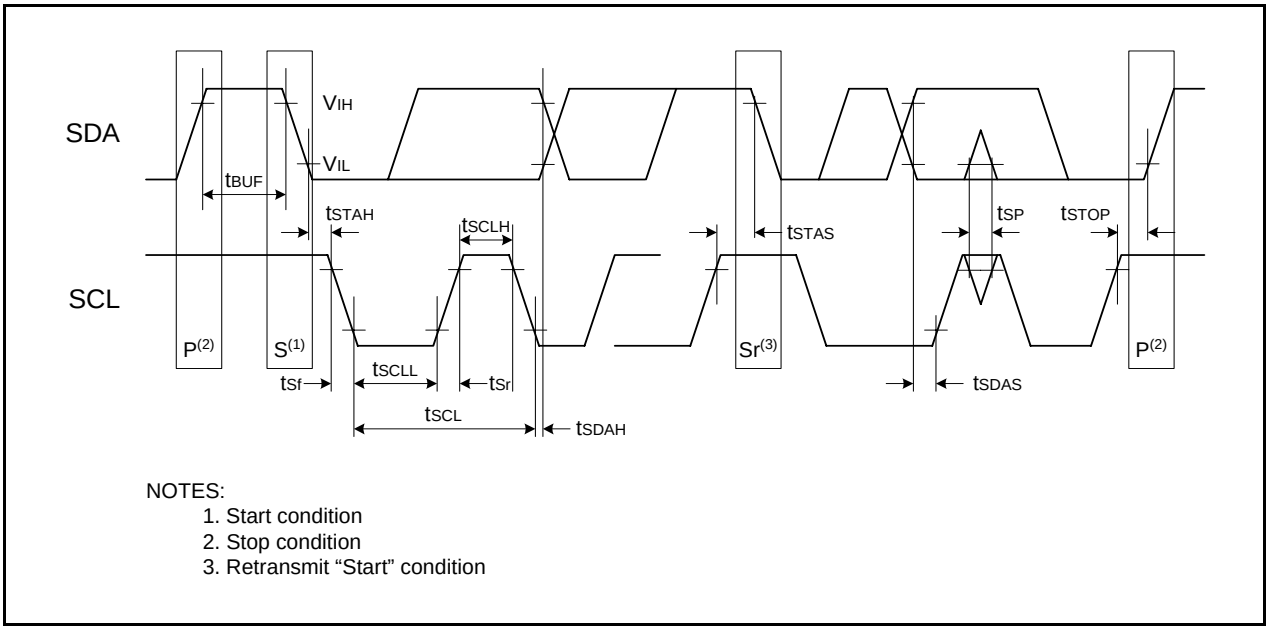


Figure 5.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

Table 5.13 Timing Requirements of I²C Bus Interface(1)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC}$ + 600(2)	–	–	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC}$ + 300(2)	–	–	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC}$ + 500(2)	–	–	ns
t_{sf}	SCL, SDA input falling time		–	–	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		–	–	$1t_{CYC}$(2)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$(2)	–	–	ns
t_{STAH}	Start condition input hole time		$3t_{CYC}$(2)	–	–	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{SOAS}	Data input setup time		$1t_{CYC}$ + 20(2)	–	–	ns
t_{SDAH}	Data input hold time		0	–	–	ns

NOTES:
1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. $1t_{CYC}$ = 1/f1(s)



NOTES:
1. Start condition
2. Stop condition
3. Retransmit “Start” condition

Figure 5.7 I/O Timing of I²C Bus Interface

Table 5.20 Electrical Characteristics (3) [Vcc = 3 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except XOUT	I_{OH} = -1 mA		V_{CC} – 0.5	–	V_{CC}	V
		XOUT	Drive capacity HIGH	I_{OH} = -0.1 mA	V_{CC} – 0.5	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -50 μA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage	Except XOUT	I_{OL} = 1 mA		–	–	0.5	V
		XOUT	Drive capacity HIGH	I_{OL} = 0.1 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 50 μA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, SSI, SCL, SDA, SSO			0.1	0.3	–	V
		$\overline{RESET}$			0.1	0.4	–	V
I_{IH}	Input “H” current		VI = 3 V, Vcc = 3 V		–	–	4.0	μA
I_{IL}	Input “L” current		VI = 0 V, Vcc = 3 V		–	–	-4.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, Vcc = 3 V		66	160	500	kΩ
R_{fXIN}	Feedback resistance	XIN			–	3.0	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		2.0	–	–	V

NOTE:
1. V_{CC} = 2.7 to 3.3 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), f(XIN) = 10 MHz, unless otherwise specified.

Table 5.24 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	300	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	150	–	ns
$t_{W(CKL)}$	CLK0 input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

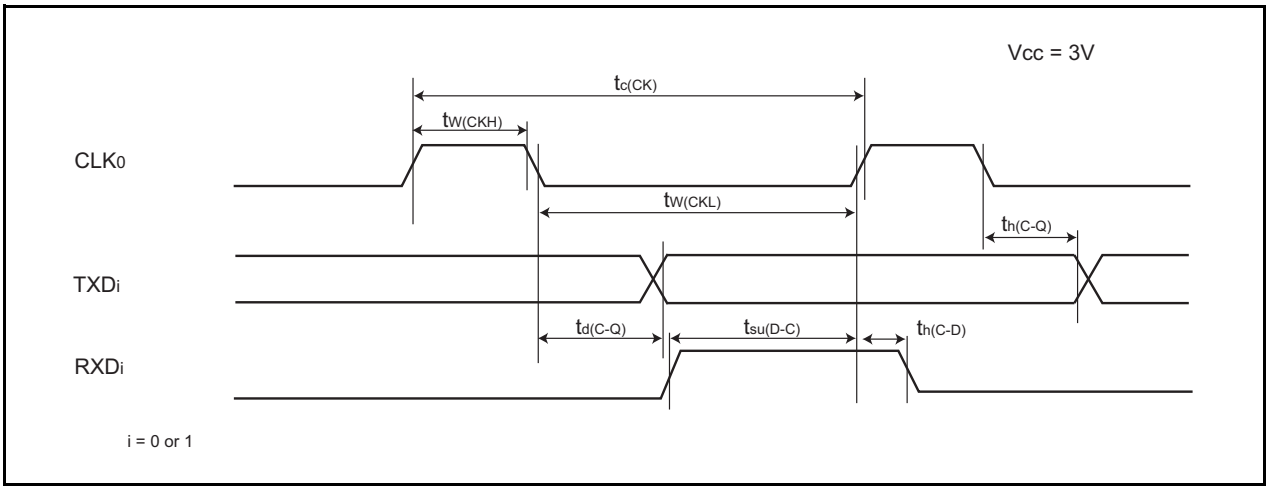


Figure 5.14 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.25 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input HIGH width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input LOW width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.

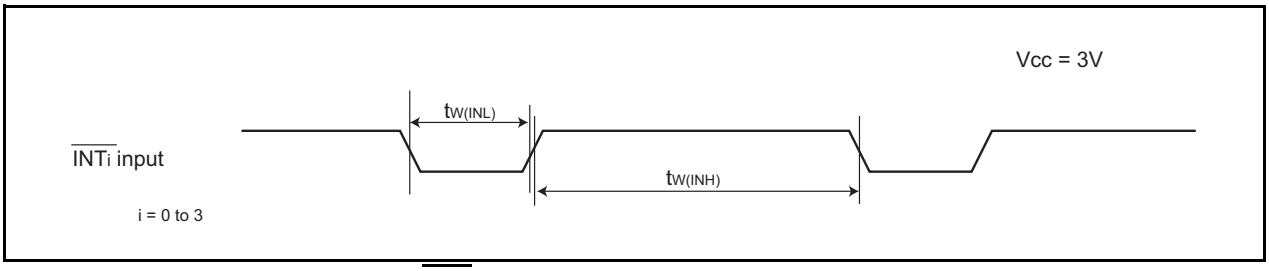


Figure 5.15 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 3 V (i = 0 to 3)

REVISION HISTORY	R8C/22 Group, R8C/23 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Mar 08, 2005	–	First Edition issued
0.20	Sep 29, 2005	–	Words standardized - Clock synchronous serial interface → Clock synchronous serial I/O - Chip-select clock synchronous interface(SSU) → Clock synchronous serial I/O with chip select - I^2C bus interface(IIC) → I^2C bus interface
		2, 3	Table1.1 R8C/22 Group Performance, Table1.2 R8C/23 Group Performance Serial Interface revised: - Clock Synchronous Serial Interface: 1 channel I^2C bus Interface (3), Clock synchronous serial I/O with chip select - Power-On Reset Circuit added - Power Consumption value determined
		5, 6	Table 1.3 Product Information of R8C/22 Group, Table 1.4 Product Information of R8C/23 Group Date revised.
		7	Figure 1.4 Pin Assignment Pin name revised: - P3_5/$\overline{\text{SSC}}$K(/SCL) → P3_5/ SCL/$\overline{\text{SSC}}$K - P3_4/$\overline{\text{SCS}}$(/SDA) → P3_4/ SDA /$\overline{\text{SCS}}$ - VSS → VSS/AVSS - VCC → VCC/AVCC - P1_5/$\overline{\text{RXD0}}$/(TRAIO/$\overline{\text{INT1}}$) → P1_5/RXD0/(TRAIO)/($\overline{\text{INT1}}$) - P6_6/$\overline{\text{INT2}}$/(TXD1) → P6_6/$\overline{\text{INT2}}$/TXD1 - P6_7/$\overline{\text{INT3}}$/(RXD1) → P6_7/$\overline{\text{INT3}}$/RXD1 - NOTE2 added
		8	Table 1.5 Pin Description - Analog Power Supply Input: line added - I^2C Bus Interface (IIC) → I^2C Bus Interface - SSU → Clock Synchronous Serial I/O with Chip Select
		9	Table 1.6 Pin Name Information by Pin Number revised - Pin Number 1: (SCL) → SCL - Pin Number 2: (SDA) → SDA - Pin Number 9: VSS → VSS/AVSS - Pin Number 11: VCC → VCC/AVCC - Pin Number 26: (TXD1) → TXD1 - Pin Number 27: (RXD1) → RXD1
		15	Table 4.1 SFR Information (1) revised - 0013h: XXXXXX00b → 00h
		17	Table 4.3 SFR Information (3) revised - 00BCh: 0000X000b → 00h/0000X000b
		18	Table 4.4 SFR Information (4) revised - 00D6h: 00000XXXb → 00h - 00F5h: UART1 Function Select Register added
		19	Table 4.5 SFR Information (5) revised - 0104h: TRATR → TRA