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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21237jfp

Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules						
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I ² C Bus Interface	CAN Module	A/D Converter
1		P3_5				SSCK	SCL		
2		P3_3				SSI			
3		P3_4				SCS	SDA		
4	MODE								
5		P4_3							
6		P4_4							
7	RESET								
8	XOUT	P4_7							
9	VSS/AVSS								
10	XIN	P4_6							
11	VCC/AVCC								
12		P2_7		TRDIOD1					
13		P2_6		TRDIOC1					
14		P2_5		TRDIOB1					
15		P2_4		TRDIOA1					
16		P2_3		TRDIOD0					
17		P2_2		TRDIOC0					
18		P2_1		TRDIOB0					
19		P2_0		TRDIOA0/TRDCLK					
20		P1_7	INT1	TRAIO					
21		P1_6			CLK0				
22		P1_5	(INT1) ⁽¹⁾	(TRAIO) ⁽¹⁾	RXD0				
23		P1_4			TXD0				
24		P1_3	KI3						AN11
25		P4_5	INT0	INT0					
26		P6_6	INT2		TXD1				
27		P6_7	INT3		RXD1				
28		P1_2	KI2						AN10
29		P1_1	KI1						AN9
30		P1_0	KI0						AN8
31		P3_1		TRBO					
32		P3_0		TRA0					
33		P6_5							
34		P6_4							
35		P6_3							
36		P0_7							AN0
37		P0_6							AN1
38		P0_5							AN2
39		P0_4							AN3
40	VREF	P4_2							
41		P6_0		TRE0					
42		P6_2						CRX0	
43		P6_1						CTX0	
44		P0_3							AN4
45		P0_2							AN5
46		P0_1							AN6
47		P0_0							AN7
48		P3_7				SSO			

NOTE:

1. Can be assigned to the pin in parentheses by a program.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. Of these, R0, R1, R2, R3, A0, A1, and FB comprise a register bank. Two sets of register banks are provided.

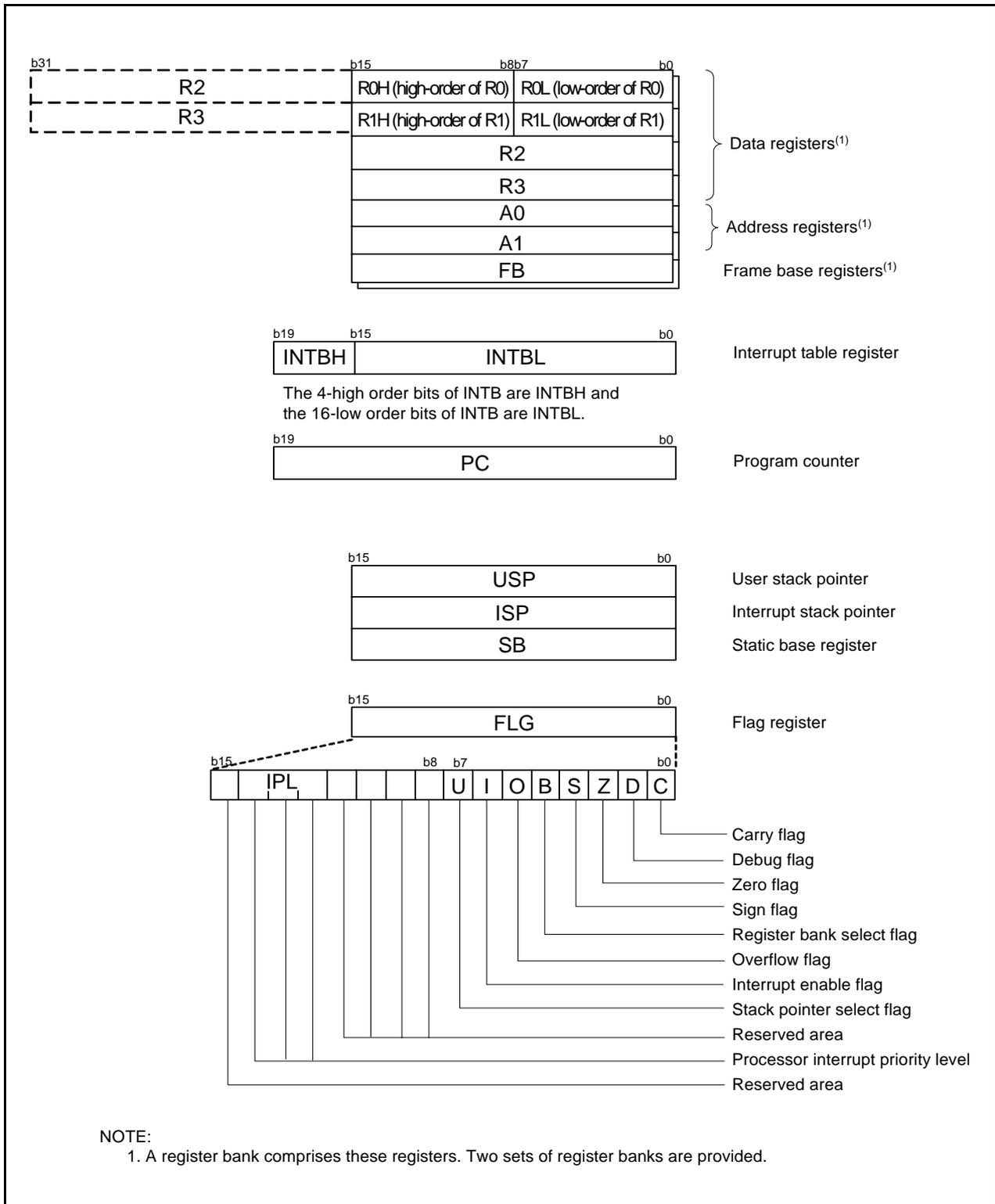


Figure 2.1 CPU Registers

2.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

An interrupt is disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3.2 R8C/23 Group

Figure 3.2 shows a Memory Map of R8C/23 Group. The R8C/23 Group has 1 Mbyte of address space from address 00000h to FFFFFh.

The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM is allocated addresses 04000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFR) are allocated addresses 00000h to 002FFh and 01300h to 0147Fh (SFR area for CAN). The peripheral function control registers are allocated them. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

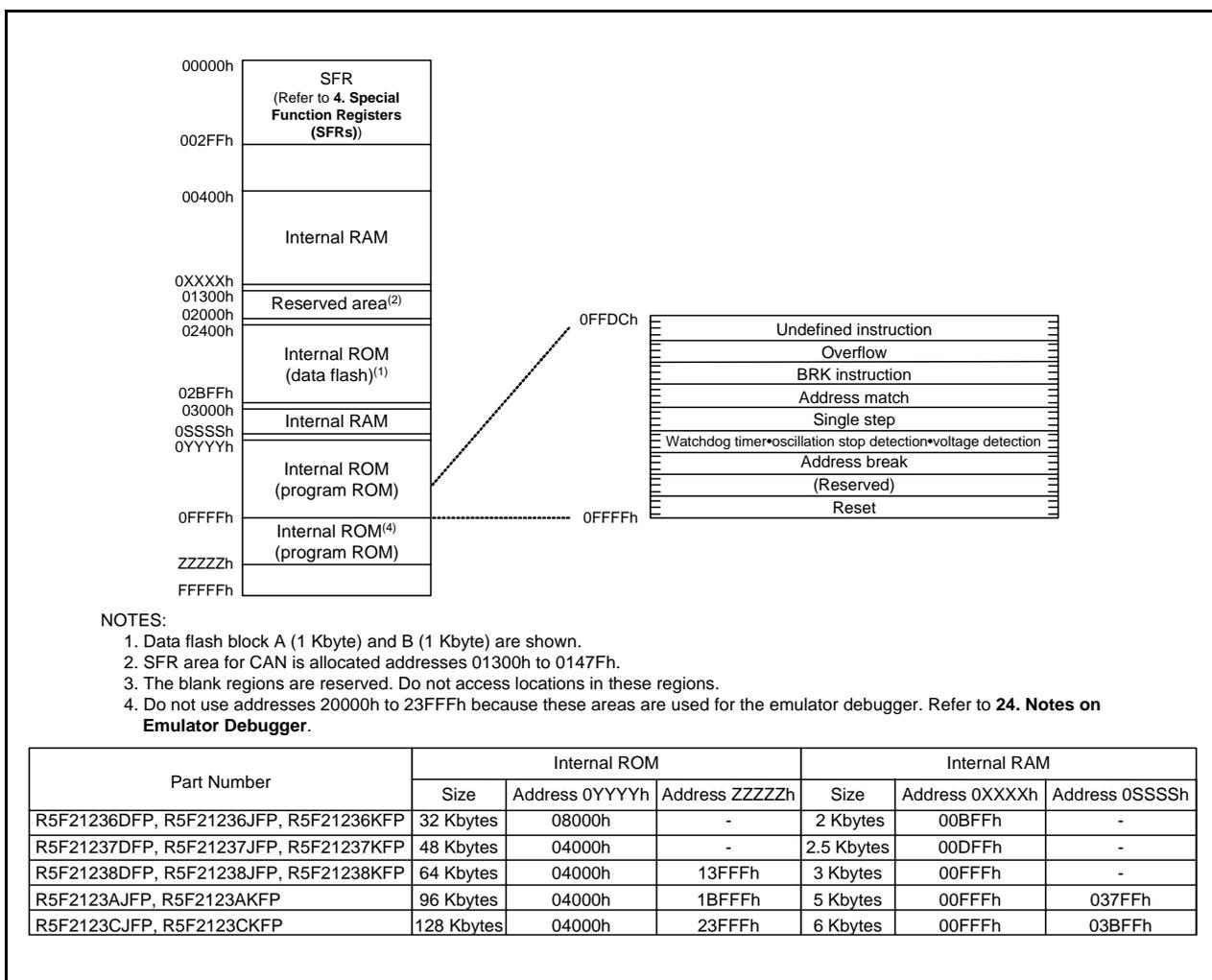


Figure 3.2 Memory Map of R8C/23 Group

Table 4.2 SFR Information (2)⁽¹⁾

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h	CAN0 Wake Up Interrupt Control Register	C01WKIC	XXXXX000b
0044h	CAN0 Successful Reception Interrupt Control Register	C0RECIC	XXXXX000b
0045h	CAN0 Successful Transmission Interrupt Control Register	C0TRMIC	XXXXX000b
0046h	CAN0 State/Error Interrupt Control Register	C01ERRIC	XXXXX000b
0047h			
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register/IIC Bus Interrupt Control Register ⁽²⁾	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.3 SFR Information (3)⁽¹⁾

Address	Register	Symbol	After reset
0080h			
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART1 Transmit/Receive Mode Register	U1MR	00h
00A9h	UART1 Bit Rate Register	U1BRG	XXh
00AAh	UART1 Transmit Buffer Register	U1TB	XXh
00ABh			XXh
00ACh	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
00ADh	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
00AEh	UART1 Receive Buffer Register	U1RB	XXh
00AFh			XXh
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h	SS Control Register H/IIC Bus Control Register 1 ⁽²⁾	SSCRH/ICCR1	00h
00B9h	SS Control Register L/IIC Bus Control Register 2 ⁽²⁾	SSCRL/ICCR2	01111101b
00BAh	SS Mode Register/IIC Bus Mode Register 1 ⁽²⁾	SSMR/ICMR	00011000b
00BBh	SS Enable Register/IIC Bus Interrupt Enable Register ⁽²⁾	SSER/ICIER	00h
00BCh	SS Status Register/IIC Bus Status Register ⁽²⁾	SSSR/ICSR	00h/0000X000b
00BDh	SS Mode Register 2/Slave Address Register ⁽²⁾	SSMR2/SAR	00h
00BEh	SS Transmit Data Register/IIC Bus Transmit Data Register ⁽²⁾	SSTD/ICDRT	FFh
00BFh	SS Receive Data Register/IIC Bus Receive Data Register ⁽²⁾	SSRDR/ICDRR	FFh

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.5 SFR Information (5)⁽¹⁾

Address	Register	Symbol	After reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRES	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Counter Data Register	TRESEC	00h
0119h	Timer RE Compare Data Register	TREMIN	00h
011Ah			
011Bh			
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h			
0121h			
0122h			
0123h			
0124h			
0125h			
0126h			
0127h			
0128h			
0129h			
012Ah			
012Bh			
012Ch			
012Dh			
012Eh			
012Fh			
0130h			
0131h			
0132h			
0133h			
0134h			
0135h			
0136h			
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.7 SFR Information (7)⁽¹⁾

Address	Register	Symbol	After reset
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01FDh			
01FEh			
01FFh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.8 SFR Information (8)⁽¹⁾

Address	Register	Symbol	After reset
1300h	CAN0 Message Control Register 0	C0MCTL0	00h
1301h	CAN0 Message Control Register 1	C0MCTL1	00h
1302h	CAN0 Message Control Register 2	C0MCTL2	00h
1303h	CAN0 Message Control Register 3	C0MCTL3	00h
1304h	CAN0 Message Control Register 4	C0MCTL4	00h
1305h	CAN0 Message Control Register 5	C0MCTL5	00h
1306h	CAN0 Message Control Register 6	C0MCTL6	00h
1307h	CAN0 Message Control Register 7	C0MCTL7	00h
1308h	CAN0 Message Control Register 8	C0MCTL8	00h
1309h	CAN0 Message Control Register 9	C0MCTL9	00h
130Ah	CAN0 Message Control Register 10	C0MCTL10	00h
130Bh	CAN0 Message Control Register 11	C0MCTL11	00h
130Ch	CAN0 Message Control Register 12	C0MCTL12	00h
130Dh	CAN0 Message Control Register 13	C0MCTL13	00h
130Eh	CAN0 Message Control Register 14	C0MCTL14	00h
130Fh	CAN0 Message Control Register 15	C0MCTL15	00h
1310h	CAN0 Control Register	C0CTLR	X0000001b
1311h			XX0X0000b
1312h	CAN0 Status Register	C0STR	00h
1313h			X0000001b
1314h	CAN0 Slot Status Register	C0SSTR	00h
1315h			00h
1316h	CAN0 Interrupt Control Register	C0ICR	00h
1317h			00h
1318h	CAN0 Extended ID Register	C0IDR	00h
1319h			00h
131Ah	CAN0 Configuration Register	C0CONR	XXh
131Bh			XXh
131Ch	CAN0 Receive Error Count Register	C0RECR	00h
131Dh	CAN0 Transmit Error Count Register	C0TECR	00h
131Eh			
131Fh			
1320h			
1321h			
1322h			
1323h			
1324h			
1325h			
1326h			
1327h			
1328h			
1329h			
132Ah			
132Bh			
132Ch			
132Dh			
132Eh			
132Fh			
1330h			
1331h			
1332h			
1333h			
1334h			
1335h			
1336h			
1337h			
1338h			
1339h			
133Ah			
133Bh			
133Ch			
133Dh			
133Eh			
133Fh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.9 SFR Information (9)⁽¹⁾

Address	Register	Symbol	After reset
1340h			
1341h			
1342h	CAN0 Acceptance Filter Support Register	C0AFS	XXh
1343h			XXh
1344h			
1345h			
1346h			
1347h			
1348h			
1349h			
134Ah			
134Bh			
134Ch			
134Dh			
134Eh			
134Fh			
1350h			
1351h			
1352h			
1353h			
1354h			
1355h			
1356h			
1357h			
1358h			
1359h			
135Ah			
135Bh			
135Ch			
135Dh			
135Eh			
135Fh	CAN0 Clock Select Register	CCLKR	00h
1360h	CAN0 Slot 0: Identifier/DLC		
1361h			XXh
1362h			XXh
1363h			XXh
1364h			XXh
1365h			XXh
1366h	CAN0 Slot 0: Data Field		XXh
1367h			XXh
1368h			XXh
1369h			XXh
136Ah			XXh
136Bh			XXh
136Ch			XXh
136Dh			XXh
136Eh	CAN0 Slot 0: Time Stamp		XXh
136Fh			XXh
1370h	CAN0 Slot 1: Identifier/DLC		XXh
1371h			XXh
1372h			XXh
1373h			XXh
1374h			XXh
1375h			XXh
1376h		CAN0 Slot 1: Data Field	
1377h			XXh
1378h			XXh
1379h			XXh
137Ah			XXh
137Bh			XXh
137Ch			XXh
137Dh			XXh
137Eh	CAN0 Slot 1: Time Stamp		XXh
137Fh			XXh

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.12 SFR Information (12)⁽¹⁾

Address	Register	Symbol	After reset
1400h	CAN0 Slot 10: Identifier/DLC		XXh
1401h			XXh
1402h			XXh
1403h			XXh
1404h			XXh
1405h			XXh
1406h	CAN0 Slot 10: Data Field		XXh
1407h			XXh
1408h			XXh
1409h			XXh
140Ah			XXh
140Bh			XXh
140Ch			XXh
140Dh			XXh
140Eh			CAN0 Slot 10: Time Stamp
140Fh	XXh		
1410h	CAN0 Slot 11: Identifier/DLC		XXh
1411h			XXh
1412h			XXh
1413h			XXh
1414h			XXh
1415h			XXh
1416h	CAN0 Slot 11: Data Field		XXh
1417h			XXh
1418h			XXh
1419h			XXh
141Ah			XXh
141Bh			XXh
141Ch			XXh
141Dh			XXh
141Eh			CAN0 Slot 11: Time Stamp
141Fh	XXh		
1420h	CAN0 Slot 12: Identifier/DLC		XXh
1421h			XXh
1422h			XXh
1423h			XXh
1424h			XXh
1425h			XXh
1426h	CAN0 Slot 12: Data Field		XXh
1427h			XXh
1428h			XXh
1429h			XXh
142Ah			XXh
142Bh			XXh
142Ch			XXh
142Dh			XXh
142Eh			CAN0 Slot 12: Time Stamp
142Fh	XXh		
1430h	CAN0 Slot 13: Identifier/DLC		XXh
1431h			XXh
1432h			XXh
1433h			XXh
1434h			XXh
1435h			XXh
1436h	CAN0 Slot 13: Data Field		XXh
1437h			XXh
1438h			XXh
1439h			XXh
143Ah			XXh
143Bh			XXh
143Ch			XXh
143Dh			XXh
143Eh			CAN0 Slot 13: Time Stamp
143Fh	XXh		

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V _{CC} /AV _{CC}	Supply voltage		-0.3 to 6.5	V
V _I	Input voltage		-0.3 to V _{CC} +0.3	V
V _O	Output voltage		-0.3 to V _{CC} +0.3	V
P _d	Power dissipation	-40°C ≤ Topr ≤ 85°C	300	mW
		85°C < Topr ≤ 125°C	125	mW
Topr	Operating ambient temperature		-40 to 85 (D, J version) / -40 to 125 (K version)	°C
T _{stg}	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit	
				Min.	Typ.	Max.		
V _{CC} /AV _{CC}	Supply voltage			2.7	–	5.5	V	
V _{SS} /AV _{CC}	Supply voltage			–	0	–	V	
V _{IH}	Input “H” voltage			0.8V _{CC}	–	V _{CC}	V	
V _{IL}	Input “L” voltage			0	–	0.2V _{CC}	V	
I _{OH(sum)}	Peak sum output “H” current	Sum of all Pins I _{OH} (peak)		–	–	-60	mA	
I _{OH(peak)}	Peak output “H” current			–	–	-10	mA	
I _{OH(ave)}	Average output “H” current			–	–	-5	mA	
I _{OL(sum)}	Peak sum output “L” currents	Sum of all Pins I _{OL} (peak)		–	–	60	mA	
I _{OL(peak)}	Peak output “L” currents			–	–	10	mA	
I _{OL(ave)}	Average output “L” current			–	–	5	mA	
f _(XIN)	XIN clock input oscillation frequency		3.0 V ≤ V _{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	0	–	20	MHz	
			3.0 V ≤ V _{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 125°C	0	–	16	MHz	
			2.7 V ≤ V _{CC} < 3.0 V	0	–	10	MHz	
–	System clock	OCD2 = 0 When XIN clock is selected.	3.0 V ≤ V _{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	0	–	20	MHz	
			3.0 V ≤ V _{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 125°C	0	–	16	MHz	
			2.7 V ≤ V _{CC} < 3.0 V	0	–	10	MHz	
		OCD2 = 1 When on-chip oscillator clock is selected.	FRA01 = 0 When low-speed on-chip oscillator clock is selected.	–	125	–	–	kHz
			FRA01 = 1 When high-speed on-chip oscillator clock is selected. 3.0 V ≤ V _{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	–	–	–	20	MHz
			FRA01 = 1 When high-speed on-chip oscillator clock is selected.	–	–	–	10	MHz

NOTES:

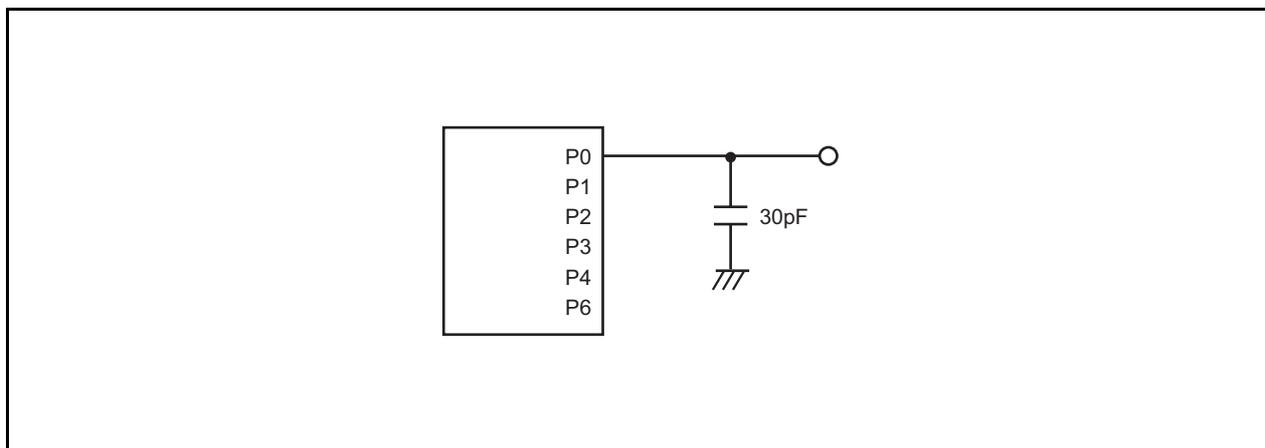
- V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
- The average output current indicates the average value of current measured during 100 ms.

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		$V_{ref} = AV_{CC}$	–	–	10	Bits
–	Absolute Accuracy	10-bit mode	$\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 5.0 \text{ V}$	–	–	± 3	LSB
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 5.0 \text{ V}$	–	–	± 2	LSB
		10-bit mode	$\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 3.3 \text{ V}$	–	–	± 5	LSB
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 3.3 \text{ V}$	–	–	± 2	LSB
R_{ladder}	Resistor ladder		$V_{ref} = AV_{CC}$	10	–	40	$k\Omega$
t_{conv}	Conversion time	10-bit mode	$\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 5.0 \text{ V}$	3.3	–	–	μs
		8-bit mode	$\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 5.0 \text{ V}$	2.8	–	–	μs
V_{ref}	Reference voltage			2.7	–	AV_{CC}	V
V_{IA}	Analog input voltage ⁽²⁾			0	–	AV_{CC}	V
–	A/D operating clock frequency	Without sample & hold		0.25	–	10	MHz
		With sample & hold		1	–	10	MHz

NOTES:

- $V_{CC} = AV_{CC} = 2.7$ to 5.5 V at $T_{opr} = -40$ to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
- When analog input voltage exceeds reference voltage, A/D conversion result is 3FFh in 10-bit mode, FFh in 8-bit mode.

**Figure 5.1 Ports P0 to P4, P6 Timing Measurement Circuit**

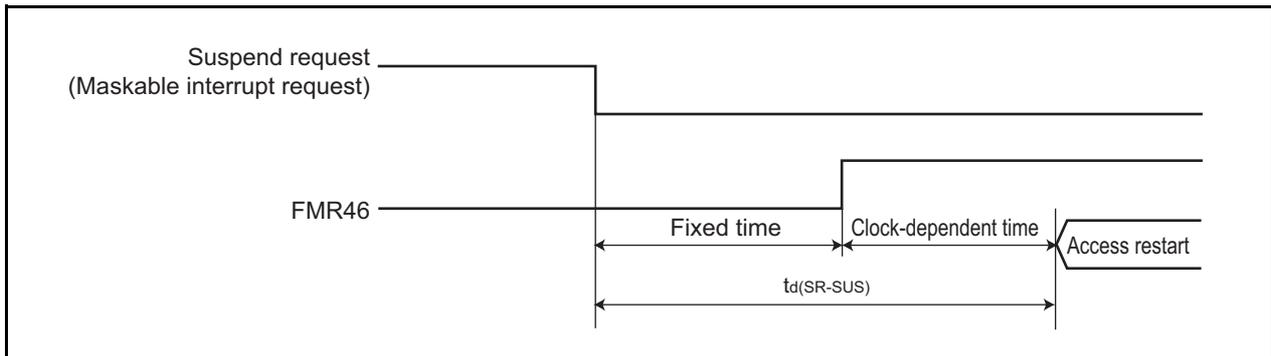


Figure 5.2 Time delay until Suspend

Table 5.6 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det1}	Voltage detection level ^(3, 4)		2.70	2.85	3.00	V
t _d (V _{det1} -A)	Voltage monitor 1 reset generation time ⁽⁵⁾		–	40	200	μs
–	Voltage detection circuit self power consumption	VCA26 = 1, V _{CC} = 5.0 V	–	0.6	–	μA
t _d (E-A)	Waiting time until voltage detection circuit operation starts ⁽²⁾		–	–	100	μs
V _{ccmin}	MCU operating voltage minimum value		2.70	–	–	V

NOTES:

1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and Topr = -40°C to 85°C (D, J version) / -40°C to 125°C (K version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
3. Hold V_{det2} > V_{det1}.
4. This parameter shows the voltage detection level when the power supply drops. The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.
5. Time until the voltage monitor 1 reset is generated after the voltage passes V_{det1} when V_{CC} falls. When using the digital filter, its sampling time is added to t_d(V_{det1}-A). When using the voltage monitor 1 reset, maintain this time until V_{CC} = 2.0 V after the voltage passes V_{det1} when the power supply falls.

Table 5.7 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det2}	Voltage detection level ⁽⁴⁾		3.3	3.6	3.9	V
t _d (V _{det2} -A)	Voltage monitor 2 reset/interrupt request generation time ^(2, 5)		–	40	200	μs
–	Voltage detection circuit self power consumption	VCA27 = 1, V _{CC} = 5.0V	–	0.6	–	μA
t _d (E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		–	–	100	μs

NOTES:

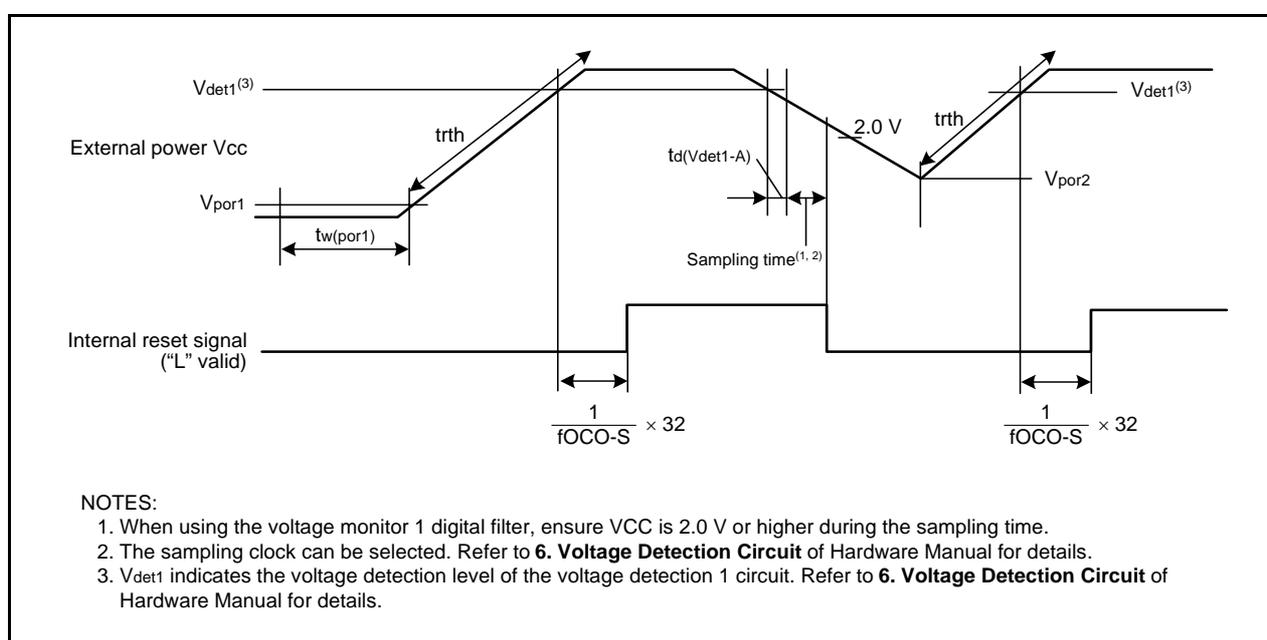
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and Topr = -40°C to 85°C (D, J version) / -40°C to 125°C (K version).
2. Time until the voltage monitor 2 reset/interrupt request is generated since the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.
4. Hold V_{det2} > V_{det1}.
5. When using the digital filter, its sampling time is added to t_d(V_{det2}-A). When using the voltage monitor 2 reset, maintain this time until V_{CC} = 2.0 V after the voltage passes V_{det2} when the power supply falls.

Table 5.8 Power-on Reset Circuit, Voltage Monitor 1 Reset Circuit Electrical Characteristics⁽³⁾

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage ⁽⁴⁾		–	–	0.1	V
V_{por2}	Power-on reset or voltage monitor 1 valid voltage		0	–	V_{det1}	V
tr_{th}	External power V_{CC} rise gradient	$V_{CC} \leq 3.6$ V	20 ⁽²⁾	–	–	mV/msec
		$V_{CC} > 3.6$ V	20 ⁽²⁾	–	2,000	mV/msec

NOTES:

1. $T_{opr} = -40^{\circ}\text{C}$ to 85°C (D, J version) / -40°C to 125°C (K version), unless otherwise specified.
2. This condition (the minimum value of external power V_{CC} rise gradient) does not apply if $V_{por2} \geq 1.0$ V.
3. To use the power-on reset function, enable voltage monitor 1 reset by setting the LVD1ON bit in the OFS register to 0, the VW1C0 and VW1C6 bits in the VW1C register to 1 respectively, and the VCA26 bit in the VCA2 register to 1.
4. $t_{w(por1)}$ indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain $t_{w(por1)}$ for 30s or more if $-20^{\circ}\text{C} \leq T_{opr} \leq 125^{\circ}\text{C}$, maintain $t_{w(por1)}$ for 3,000s or more if $-40^{\circ}\text{C} \leq T_{opr} < -20^{\circ}\text{C}$.

**Figure 5.3 Power-on Reset Circuit Electrical Characteristics**

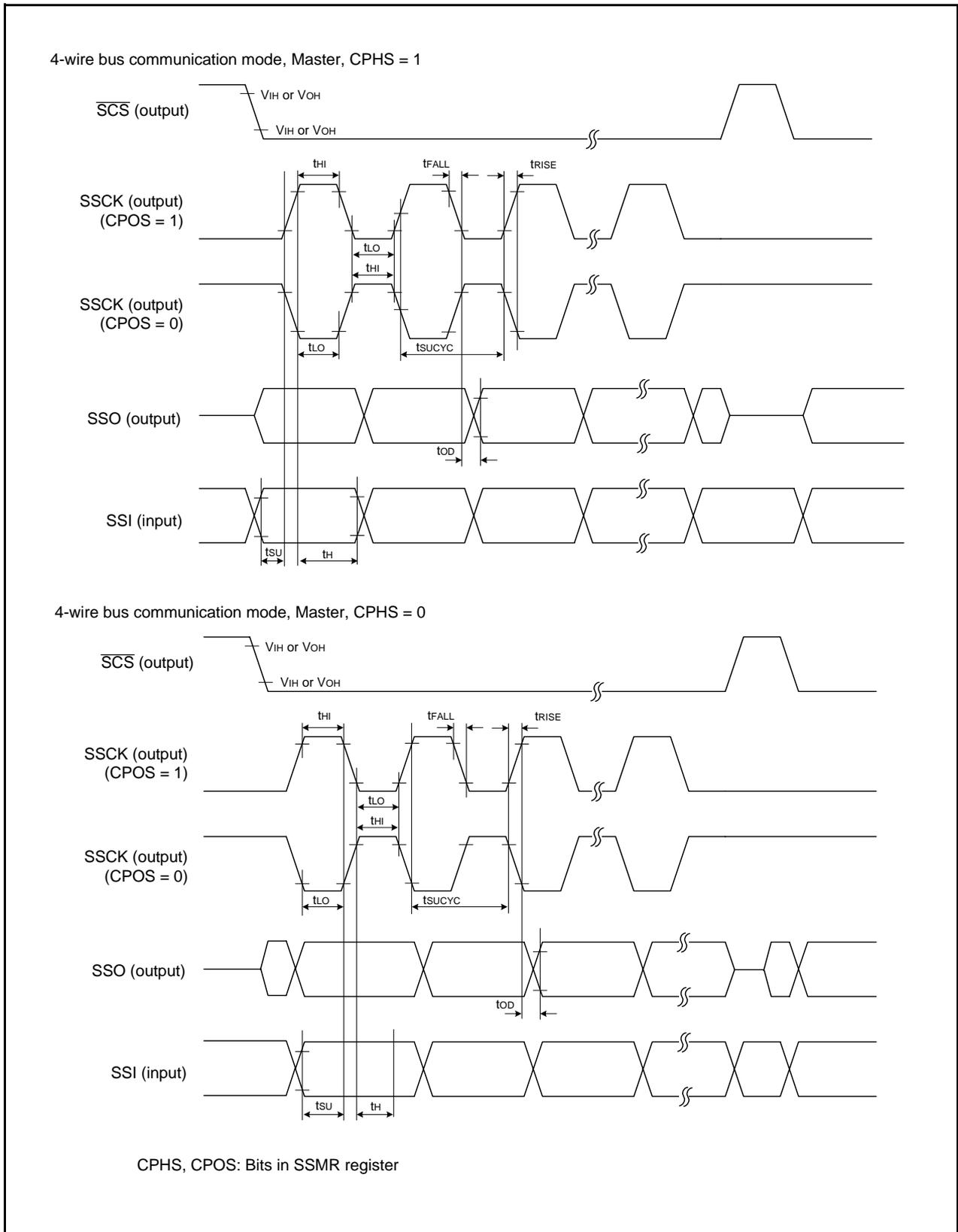


Figure 5.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

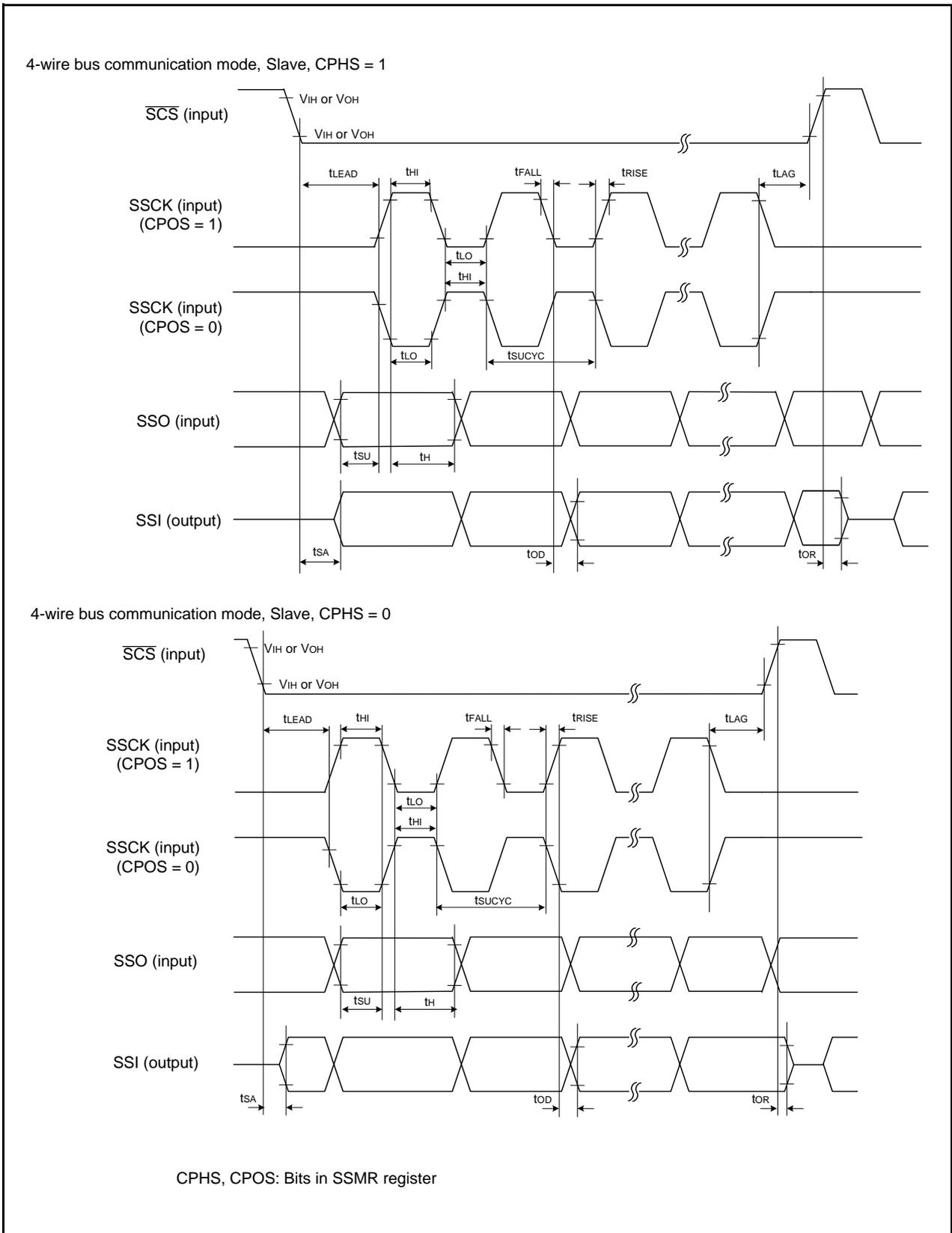


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

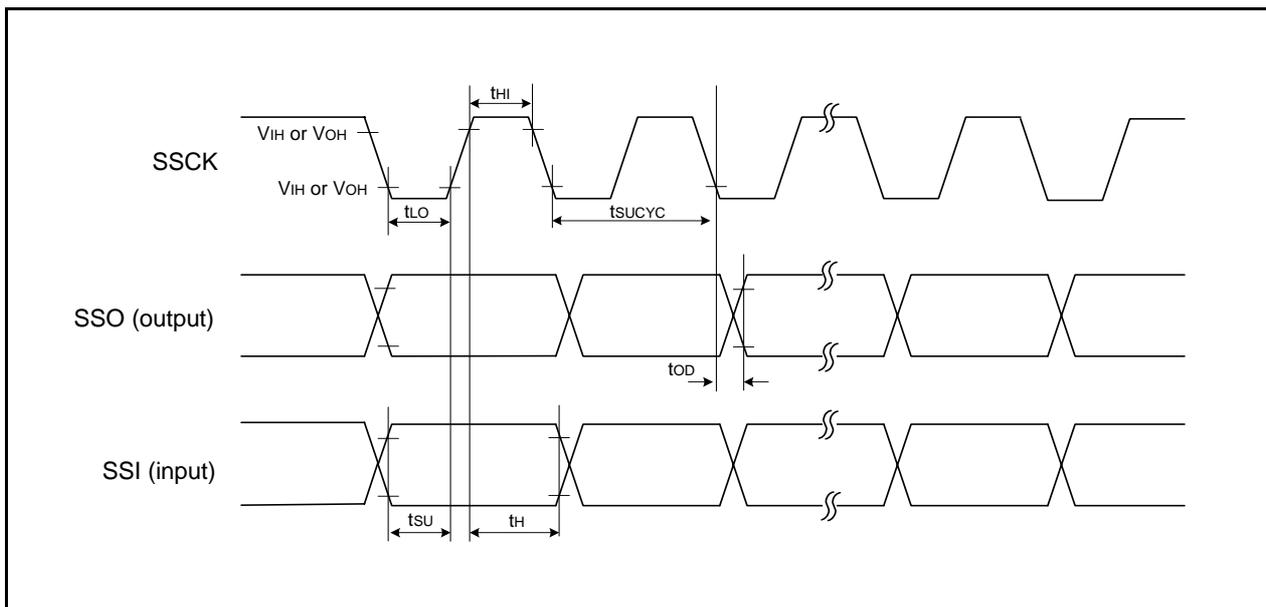


Figure 5.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

Table 5.13 Timing Requirements of I²C Bus Interface(1)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
t _{SCL}	SCL input cycle time		12t _{CYC} + 600 ⁽²⁾	–	–	ns
t _{SCLH}	SCL input “H” width		3t _{CYC} + 300 ⁽²⁾	–	–	ns
t _{SCLL}	SCL input “L” width		5t _{CYC} + 500 ⁽²⁾	–	–	ns
t _{sf}	SCL, SDA input falling time		–	–	300	ns
t _{SP}	SCL, SDA input spike pulse rejection time		–	–	1t _{CYC} ⁽²⁾	ns
t _{BUF}	SDA input bus-free time		5t _{CYC} ⁽²⁾	–	–	ns
t _{STAH}	Start condition input hole time		3t _{CYC} ⁽²⁾	–	–	ns
t _{STAS}	Retransmit start condition input setup time		3t _{CYC} ⁽²⁾	–	–	ns
t _{STOP}	Stop condition input setup time		3t _{CYC} ⁽²⁾	–	–	ns
t _{SOAS}	Data input setup time		1t _{CYC} + 20 ⁽²⁾	–	–	ns
t _{SDAH}	Data input hold time		0	–	–	ns

NOTES:

1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. 1t_{CYC} = 1/f₁(s)

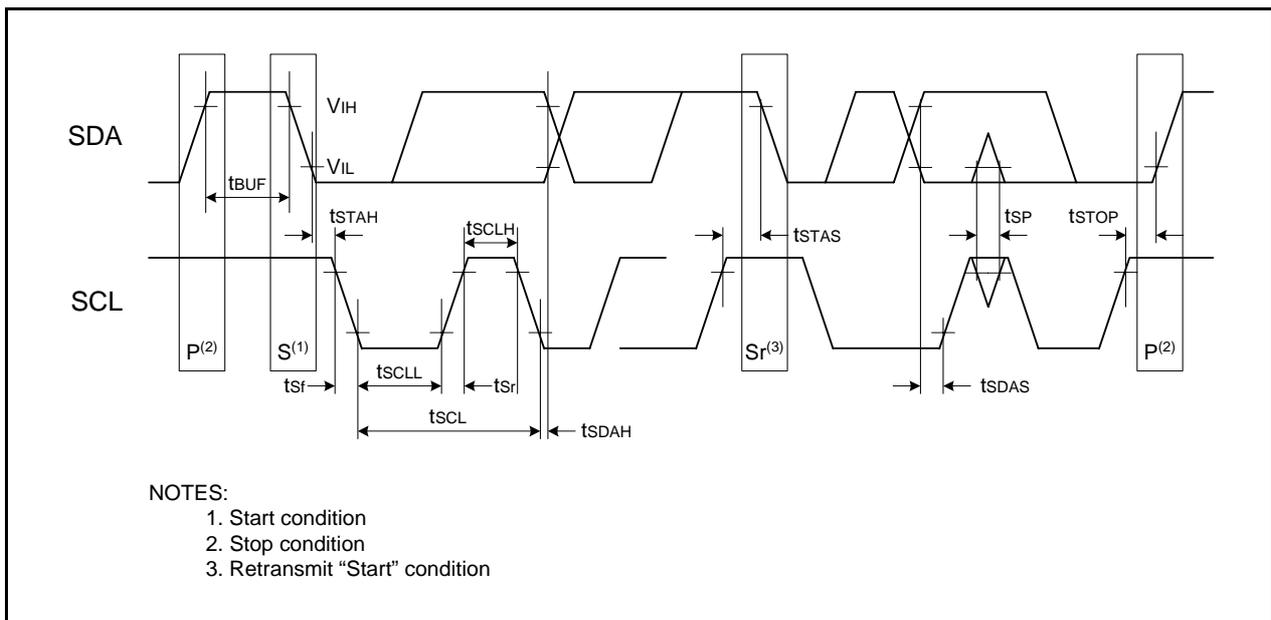
**Figure 5.7 I/O Timing of I²C Bus Interface**

Table 5.20 Electrical Characteristics (3) [V_{CC} = 3 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except XOUT	I _{OH} = -1 mA		V _{CC} - 0.5	-	V _{CC}	V
		XOUT	Drive capacity HIGH	I _{OH} = -0.1 mA	V _{CC} - 0.5	-	V _{CC}	V
			Drive capacity LOW	I _{OH} = -50 μA	V _{CC} - 0.5	-	V _{CC}	V
V _{OL}	Output "L" voltage	Except XOUT	I _{OL} = 1 mA		-	-	0.5	V
		XOUT	Drive capacity HIGH	I _{OL} = 0.1 mA	-	-	0.5	V
			Drive capacity LOW	I _{OL} = 50 μA	-	-	0.5	V
V _{T+} -V _{T-}	Hysteresis	$\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT2}}, \overline{\text{INT3}}, \text{KI0}, \text{KI1}, \text{KI2}, \text{KI3}, \text{TRAIO}, \text{RXD0}, \text{RXD1}, \text{CLK0}, \text{SSI}, \text{SCL}, \text{SDA}, \text{SSO}$			0.1	0.3	-	V
		$\overline{\text{RESET}}$			0.1	0.4	-	V
I _{IH}	Input "H" current		V _I = 3 V, V _{CC} = 3 V		-	-	4.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 3 V		-	-	-4.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 3 V		66	160	500	kΩ
R _{IXIN}	Feedback resistance	XIN			-	3.0	-	MΩ
V _{RAM}	RAM hold voltage		During stop mode		2.0	-	-	V

NOTE:

- V_{CC} = 2.7 to 3.3 V at T_{opr} = -40 to 85°C (D, J version) / -40 to 125°C (K version), f(XIN) = 10 MHz, unless otherwise specified.