Renesas Electronics America Inc - R5F21238KFP#U1 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21238kfp-u1

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

1. Overview

This MCU is built using the high-performance silicon gate CMOS process using the R8C CPU core and is packaged in a 48-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1 Mbyte of address space, it is capable of executing instructions at high speed. This MCU is equipped with one CAN module and suited to in-vehicle or FA networking.
Furthermore, the data flash (1 KB x 2 blocks) is embedded in the R8C/23 Group.
The difference between R8C/22 and R8C/23 Groups is only the existence of the data flash. Their peripheral functions are the same.

1.1 Applications

Automotive, etc.

Table 1.2 Functions and Specifications for R8C/23 Group

Item		Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to **Table 1.4 Product Information for R8C/23 Group**
Peripheral Function	Ports	I/O ports: 41 pins, Input port: 3 pins
	Timers	Timer RA: 8 bits x 1 channel, Timer RB: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer RD: 16 bits x 2 channel (Circuits of input capture and output compare) Timer RE: With compare match function
	Serial interface	1 channel (UART0) Clock synchronous I/O, UART 1 channel (UART1) UART
	Clock synchronous serial interface	1 channel I^2C bus interface(2), Clock synchronous serial I/O with chip select
	LIN module	Hardware LIN: 1 channel (Timer RA, UART0)
	CAN module	1 channel with 2.0B specification: 16 slots
	A/D converter	10-bit A/D converter: 1 circuit, 12 channels
	Watchdog timer	15 bits x 1 channel (with prescaler) Reset start selectable
	Interrupts	Internal: 14 sources, External: 6 sources, Software: 4 sources, Priority level: 7 levels
	Clock generation circuits	2 circuits XIN clock generation circuit (with on-chip feedback resistor) On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has frequency adjustment function.
	Oscillation stop detection function	Stop detection of XIN clock oscillation
	Voltage detection circuit	On-chip
	Power-on reset circuit include	On-chip
Electric Characteristics	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz)(D, J version) VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz)(K version) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)
	Current consumption	Typ. 12.5 mA (VCC = 5 V, f(XIN) = 20 MHz, High-speed on-chip oscillator stopping) Typ. 6.0 mA (VCC = 5 V, f(XIN) = 10 MHz, High-speed on-chip oscillator stopping)
Flash Memory	Programming and erasure voltage	VCC = 2.7 to 5.5 V
	Programming and erasure endurance	10,000 times (data flash)
		1,000 times (program ROM)
Operating Ambient Temperature		-40 to 85°C
		-40 to 125°C (option(1))
Package		48-pin mold-plastic LQFP

NOTES:
1. When using options, be sure to inquire about the specification.
2. I^2C bus is a registered trademark of Koninklijke Philips Electronics N.V.

1.4 Product Information

Table 1.3 lists Product Information for R8C/22 Group and Table 1.4 lists Product Information for R8C/23 Group.

Table 1.3 Product Information for R8C/22 Group **Current of Aug. 2008**

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks	
R5F21226DFP	32 Kbytes	2 Kbytes	PLQP0048KB-A	D version	Flash memory version
R5F21227DFP	48 Kbytes	2.5 Kbytes	PLQP0048KB-A		
R5F21228DFP	64 Kbytes	3 Kbytes	PLQP0048KB-A		
R5F21226JFP	32 Kbytes	2 Kbytes	PLQP0048KB-A	J version	
R5F21227JFP	48 Kbytes	2.5 Kbytes	PLQP0048KB-A		
R5F21228JFP	64 Kbytes	3 Kbytes	PLQP0048KB-A		
R5F2122AJFP	96 Kbytes	5 Kbytes	PLQP0048KB-A		
R5F2122CJFP	128 Kbytes(1)	6 Kbytes	PLQP0048KB-A		
R5F21226KFP	32 Kbytes	2 Kbytes	PLQP0048KB-A	K version	
R5F21227KFP	48 Kbytes	2.5 Kbytes	PLQP0048KB-A		
R5F21228KFP	64 Kbytes	3 Kbytes	PLQP0048KB-A		
R5F2122AKFP	96 Kbytes	5 Kbytes	PLQP0048KB-A		
R5F2122CKFP	128 Kbytes(1)	6 Kbytes	PLQP0048KB-A		

NOTE:
1. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **24. Notes on Emulator Debugger** of Hardware Manual.

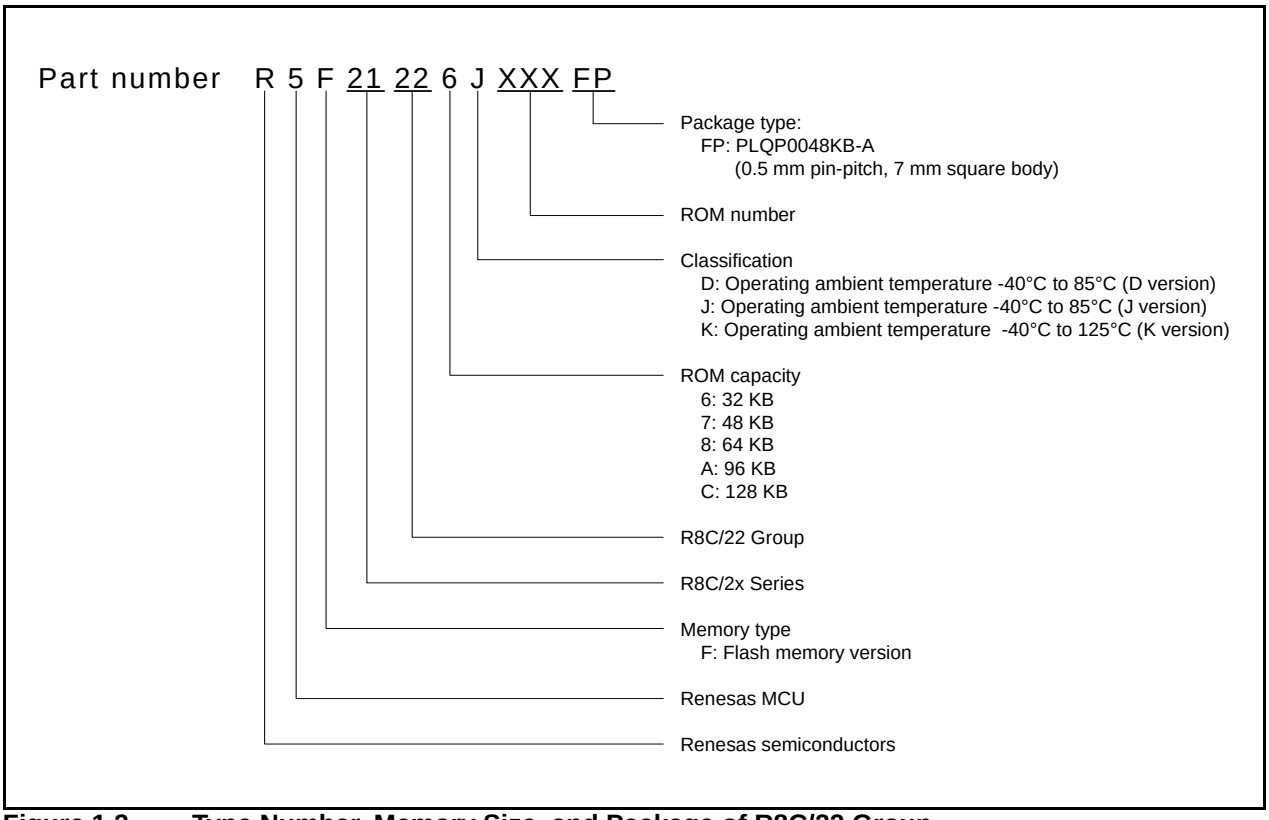
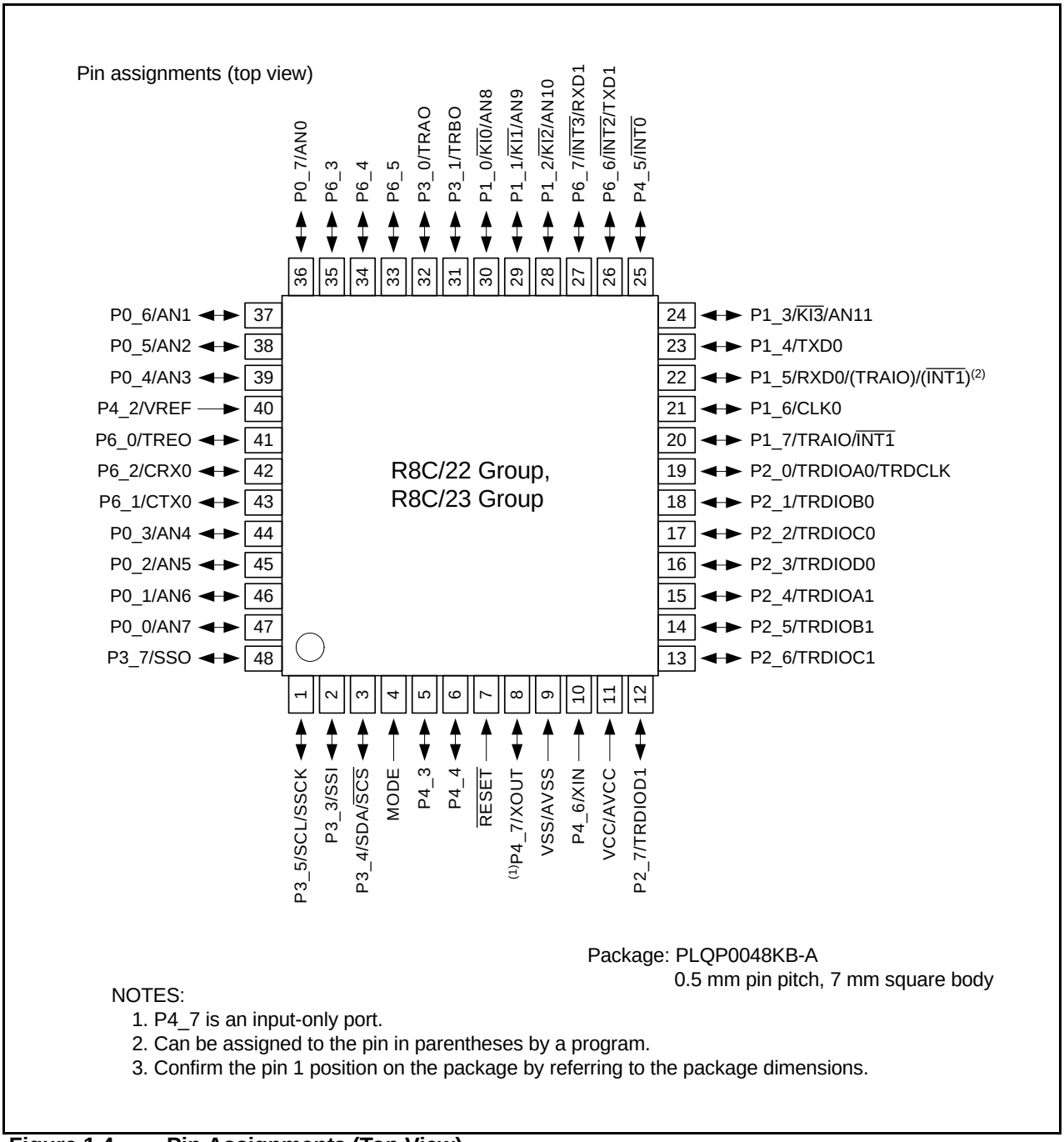


Figure 1.2 Type Number, Memory Size, and Package of R8C/22 Group

1.5 Pin Assignments

Figure 1.4 shows Pin Assignments (Top View).



NOTES:
1. P4_7 is an input-only port.
2. Can be assigned to the pin in parentheses by a program.
3. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.4 Pin Assignments (Top View)

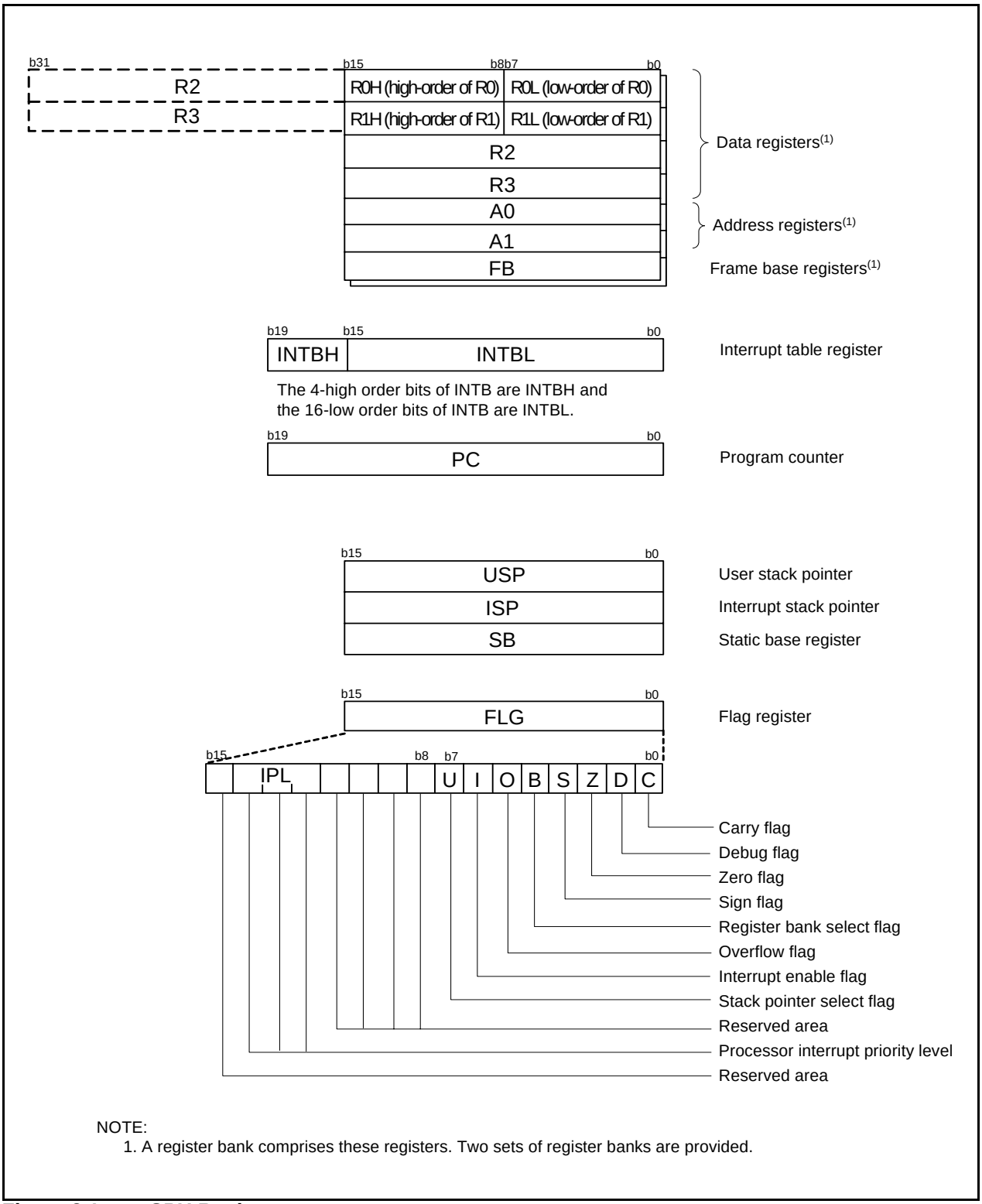
Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules						
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I^2C Bus Interface	CAN Module	A/D Converter
1		P3_5				SSCK	SCL		
2		P3_3				SSI			
3		P3_4				$\overline{SCS}$	SDA		
4	MODE								
5		P4_3							
6		P4_4							
7	$\overline{RESET}$								
8	XOUT	P4_7							
9	VSS/AVSS								
10	XIN	P4_6							
11	VCC/AVCC								
12		P2_7		TRDIOD1					
13		P2_6		TRDIOC1					
14		P2_5		TRDIOB1					
15		P2_4		TRDIOA1					
16		P2_3		TRDIOD0					
17		P2_2		TRDIOC0					
18		P2_1		TRDIOB0					
19		P2_0		TRDIOA0/TRDCLK					
20		P1_7	$\overline{INT1}$	TRAIO					
21		P1_6			CLK0				
22		P1_5	($\overline{INT1}$)(1)	(TRAIO)(1)	RXD0				
23		P1_4			TXD0				
24		P1_3	$\overline{KI3}$						AN11
25		P4_5	$\overline{INT0}$	$\overline{INT0}$					
26		P6_6	$\overline{INT2}$		TXD1				
27		P6_7	$\overline{INT3}$		RXD1				
28		P1_2	$\overline{KI2}$						AN10
29		P1_1	$\overline{KI1}$						AN9
30		P1_0	$\overline{KI0}$						AN8
31		P3_1		TRBO					
32		P3_0		TRAO					
33		P6_5							
34		P6_4							
35		P6_3							
36		P0_7							AN0
37		P0_6							AN1
38		P0_5							AN2
39		P0_4							AN3
40	VREF	P4_2							
41		P6_0		TREO					
42		P6_2						CRX0	
43		P6_1						CTX0	
44		P0_3							AN4
45		P0_2							AN5
46		P0_1							AN6
47		P0_0							AN7
48		P3_7				SSO			

NOTE:
1. Can be assigned to the pin in parentheses by a program.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. Of these, R0, R1, R2, R3, A0, A1, and FB comprise a register bank. Two sets of register banks are provided.



NOTE:
1. A register bank comprises these registers. Two sets of register banks are provided.

Figure 2.1 CPU Registers

Table 4.3 SFR Information (3)(1)

Address	Register	Symbol	After reset
0080h			
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART1 Transmit/Receive Mode Register	U1MR	00h
00A9h	UART1 Bit Rate Register	U1BRG	XXh
00AAh	UART1 Transmit Buffer Register	U1TB	XXh
00ABh			XXh
00ACh	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
00ADh	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
00AEh	UART1 Receive Buffer Register	U1RB	XXh
00AFh			XXh
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h	SS Control Register H/IIC Bus Control Register 1(2)	SSCRH/ICCR1	00h
00B9h	SS Control Register L/IIC Bus Control Register 2(2)	SSCRL/ICCR2	01111101b
00BAh	SS Mode Register/IIC Bus Mode Register 1(2)	SSMR/ICMR	00011000b
00BBh	SS Enable Register/IIC Bus Interrupt Enable Register(2)	SSER/ICIER	00h
00BCh	SS Status Register/IIC Bus Status Register(2)	SSSR/ICSR	00h/0000X000b
00BDh	SS Mode Register 2/Slave Address Register(2)	SSMR2/SAR	00h
00BEh	SS Transmit Data Register/IIC Bus Transmit Data Register(2)	SSTDR/ICDRT	FFh
00BFh	SS Receive Data Register/IIC Bus Receive Data Register(2)	SSRDR/ICDRR	FFh

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.4 SFR Information (4)(1)

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h			XXh
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Control Register 2	ADCON2	00h
00D5h			
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h	UART1 Function Select Register	U1SR	XXh
00F6h			
00F7h			
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	XX00XX00b
00FEh			
00FFh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.6 SFR Information (6)(1)

Address	Register	Symbol	After reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIORA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIORA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.7 SFR Information (7)(1)

Address	Register	Symbol	After reset
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01FDh			
01FEh			
01FFh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.9 SFR Information (9)(1)

Address	Register	Symbol	After reset
1340h			
1341h			
1342h	CAN0 Acceptance Filter Support Register	C0AFS	XXh
1343h			XXh
1344h			
1345h			
1346h			
1347h			
1348h			
1349h			
134Ah			
134Bh			
134Ch			
134Dh			
134Eh			
134Fh			
1350h			
1351h			
1352h			
1353h			
1354h			
1355h			
1356h			
1357h			
1358h			
1359h			
135Ah			
135Bh			
135Ch			
135Dh			
135Eh			
135Fh	CAN0 Clock Select Register	CCLKR	00h
1360h	CAN0 Slot 0: Identifier/DLC		XXh
1361h			XXh
1362h			XXh
1363h			XXh
1364h			XXh
1365h			XXh
1366h	CAN0 Slot 0: Data Field		XXh
1367h			XXh
1368h			XXh
1369h			XXh
136Ah			XXh
136Bh			XXh
136Ch			XXh
136Dh			XXh
136Eh	CAN0 Slot 0: Time Stamp		XXh
136Fh			XXh
1370h	CAN0 Slot 1: Identifier/DLC		XXh
1371h			XXh
1372h			XXh
1373h			XXh
1374h			XXh
1375h			XXh
1376h	CAN0 Slot 1: Data Field		XXh
1377h			XXh
1378h			XXh
1379h			XXh
137Ah			XXh
137Bh			XXh
137Ch			XXh
137Dh			XXh
137Eh	CAN0 Slot 1: Time Stamp		XXh
137Fh			XXh

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.11 SFR Information (11)(1)

Address	Register	Symbol	After reset
13C0h	CAN0 Slot 6: Identifier/DLC		XXh
13C1h			XXh
13C2h			XXh
13C3h			XXh
13C4h			XXh
13C5h			XXh
13C6h	CAN0 Slot 6: Data Field		XXh
13C7h			XXh
13C8h			XXh
13C9h			XXh
13CAh			XXh
13CBh			XXh
13CCh			XXh
13CDh			XXh
13CEh	CAN0 Slot 6: Time Stamp		XXh
13CFh			XXh
13D0h	CAN0 Slot 7: Identifier/DLC		XXh
13D1h			XXh
13D2h			XXh
13D3h			XXh
13D4h			XXh
13D5h			XXh
13D6h	CAN0 Slot 7: Data Field		XXh
13D7h			XXh
13D8h			XXh
13D9h			XXh
13DAh			XXh
13DBh			XXh
13DCh			XXh
13DDh			XXh
13DEh	CAN0 Slot 7: Time Stamp		XXh
13DFh			XXh
13E0h	CAN0 Slot 8: Identifier/DLC		XXh
13E1h			XXh
13E2h			XXh
13E3h			XXh
13E4h			XXh
13E5h			XXh
13E6h	CAN0 Slot 8: Data Field		XXh
13E7h			XXh
13E8h			XXh
13E9h			XXh
13EAh			XXh
13EBh			XXh
13ECh			XXh
13EDh			XXh
13EEh	CAN0 Slot 8: Time Stamp		XXh
13EFh			XXh
13F0h	CAN0 Slot 9: Identifier/DLC		XXh
13F1h			XXh
13F2h			XXh
13F3h			XXh
13F4h			XXh
13F5h			XXh
13F6h	CAN0 Slot 9: Data Field		XXh
13F7h			XXh
13F8h			XXh
13F9h			XXh
13FAh			XXh
13FBh			XXh
13FCh			XXh
13FDh			XXh
13FEh	CAN0 Slot 9: Time Stamp		XXh
13FFh			XXh

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.12 SFR Information (12)(1)

Address	Register	Symbol	After reset
1400h	CAN0 Slot 10: Identifier/DLC		XXh
1401h			XXh
1402h			XXh
1403h			XXh
1404h			XXh
1405h			XXh
1406h	CAN0 Slot 10: Data Field		XXh
1407h			XXh
1408h			XXh
1409h			XXh
140Ah			XXh
140Bh			XXh
140Ch			XXh
140Dh			XXh
140Eh	CAN0 Slot 10: Time Stamp		XXh
140Fh			XXh
1410h	CAN0 Slot 11: Identifier/DLC		XXh
1411h			XXh
1412h			XXh
1413h			XXh
1414h			XXh
1415h			XXh
1416h	CAN0 Slot 11: Data Field		XXh
1417h			XXh
1418h			XXh
1419h			XXh
141Ah			XXh
141Bh			XXh
141Ch			XXh
141Dh			XXh
141Eh	CAN0 Slot 11: Time Stamp		XXh
141Fh			XXh
1420h	CAN0 Slot 12: Identifier/DLC		XXh
1421h			XXh
1422h			XXh
1423h			XXh
1424h			XXh
1425h			XXh
1426h	CAN0 Slot 12: Data Field		XXh
1427h			XXh
1428h			XXh
1429h			XXh
142Ah			XXh
142Bh			XXh
142Ch			XXh
142Dh			XXh
142Eh	CAN0 Slot 12: Time Stamp		XXh
142Fh			XXh
1430h	CAN0 Slot 13: Identifier/DLC		XXh
1431h			XXh
1432h			XXh
1433h			XXh
1434h			XXh
1435h			XXh
1436h	CAN0 Slot 13: Data Field		XXh
1437h			XXh
1438h			XXh
1439h			XXh
143Ah			XXh
143Bh			XXh
143Ch			XXh
143Dh			XXh
143Eh	CAN0 Slot 13: Time Stamp		XXh
143Fh			XXh

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)	R8C/22 Group	100(3)	–	–	times
		R8C/23 Group	1,000(3)	–	–	times
–	Byte program time		–	50	400	µs
–	Block erase time		–	0.4	9	s
$t_{d(SR-SUS)}$	Time delay from suspend request until erase suspend		–	–	97 + CPU clock × 6 cycle	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3 + CPU clock × 4 cycle	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time(7)	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 1,000), each block can be erased n times.
   For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure endurance can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.5 Flash Memory (Data Flash Block A, Block B) Electrical Characteristics(4)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)		10,000(3)	–	–	times
–	Byte program time (Program/erase endurance ≤ 1,000 times)		–	50	400	µs
–	Byte program time (Program/erase endurance > 1,000 times)		–	65	–	µs
–	Block erase time (Program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (Program/erase endurance > 1,000 times)		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until erase suspend		–	–	97 + CPU clock × 6 cycle	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3 + CPU clock × 4 cycle	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		-40	–	85(8)	°C
–	Data hold time(9)	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times.
   For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Minimum endurance to guarantee all electrical characteristics after program and erase (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times are the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure endurance can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
6. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. 125°C for K version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.12 Timing Requirements of Clock Synchronous Serial I/O with Chip Select(1)

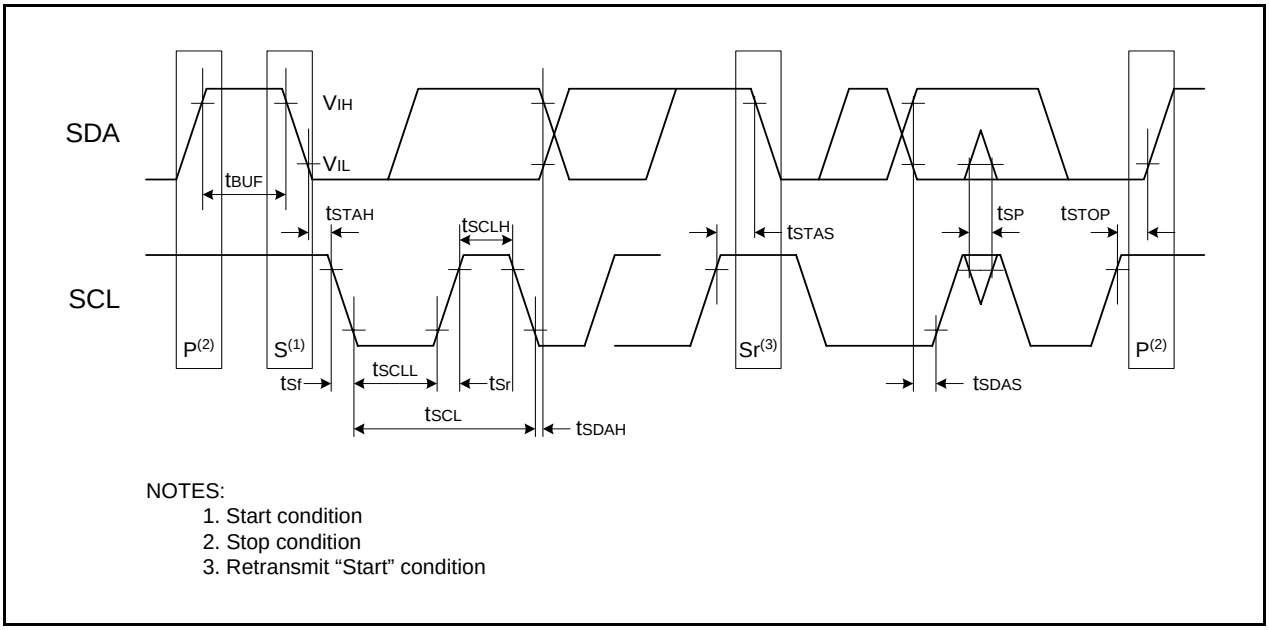
Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	–	t_{CYC}(2)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_H	SSO, SSI data input hold time			1	–	–	t_{CYC}(2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1	t_{CYC}(2)
t_{SA}	SSI slave access time			–	–	1t_{CYC} + 100	ns
t_{OR}	SSI slave out open time			–	–	1t_{CYC} + 100	ns

NOTES:
1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. 1t_{CYC} = 1/f1(s)

Table 5.13 Timing Requirements of I²C Bus Interface(1)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC}$ + 600(2)	–	–	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC}$ + 300(2)	–	–	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC}$ + 500(2)	–	–	ns
t_{sf}	SCL, SDA input falling time		–	–	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		–	–	$1t_{CYC}$(2)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$(2)	–	–	ns
t_{STAH}	Start condition input hole time		$3t_{CYC}$(2)	–	–	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$(2)	–	–	ns
t_{SOAS}	Data input setup time		$1t_{CYC}$ + 20(2)	–	–	ns
t_{SDAH}	Data input hold time		0	–	–	ns

NOTES:
1. V_{CC} = 2.7 to 5.5 V, V_{SS} = 0V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. $1t_{CYC}$ = 1/f1(s)



NOTES:
1. Start condition
2. Stop condition
3. Retransmit “Start” condition

Figure 5.7 I/O Timing of I²C Bus Interface

Table 5.14 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” Voltage	Except XOUT	I_{OH} = -5 mA		Vcc – 2.0	–	Vcc	V
			I_{OH} = -200 μA		Vcc – 0.3	–	Vcc	V
		XOUT	Drive capacity HIGH	I_{OH} = -1 mA	Vcc – 2.0	–	Vcc	V
			Drive capacity LOW	I_{OH} = -500 μA	Vcc – 2.0	–	Vcc	V
V_{OL}	Output “L” Voltage	Except XOUT	I_{OL} = 5 mA		–	–	2.0	V
			I_{OL} = 200 μA		–	–	0.45	V
		XOUT	Drive capacity HIGH	I_{OL} = 1 mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 500 μA	–	–	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, RXD0, RXD1, CLK0, SSI, SCL, SDA, SSO			0.1	0.5	–	V
		$\overline{RESET}$			0.1	1.0	–	V
I_{IH}	Input “H” current		VI = 5 V, Vcc = 5 V		–	–	5.0	μA
I_{IL}	Input “L” current		VI = 0 V, Vcc = 5 V		–	–	-5.0	μA
R_{PULLUP}	Pull-Up Resistance		VI = 0 V, Vcc = 5 V		30	50	167	kΩ
R_{fXIN}	Feedback Resistance	XIN			–	1.0	–	MΩ
V_{RAM}	RAM Hold Voltage		During stop mode		2.0	–	–	V

NOTE:
1. Vcc = 4.2 to 5.5 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.18 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	200	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	100	–	ns
$t_{W(CKL)}$	CLK0 input “L” width	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

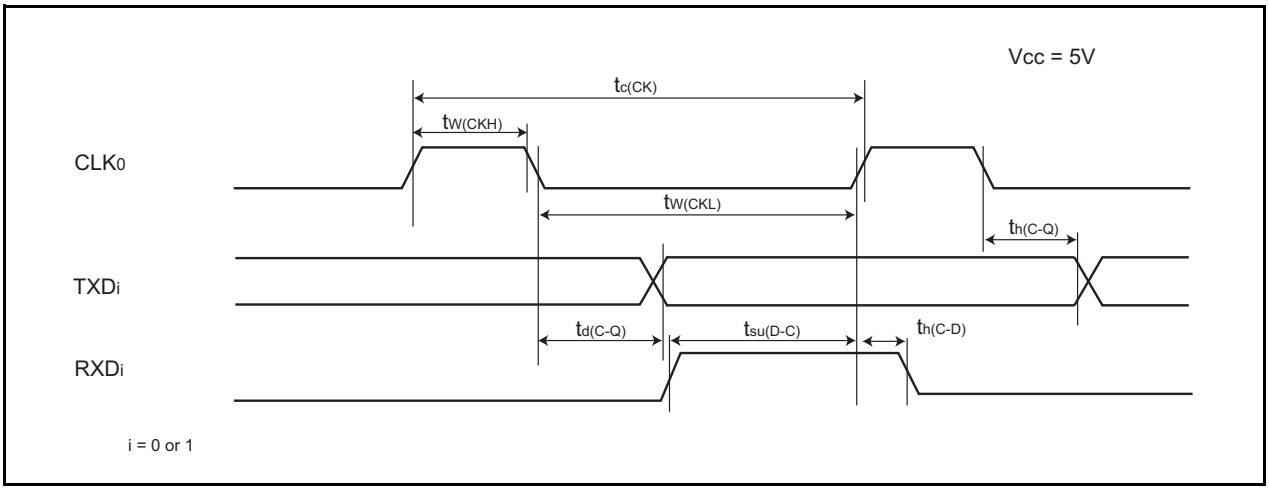


Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.19 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	250(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input HIGH width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input LOW width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.

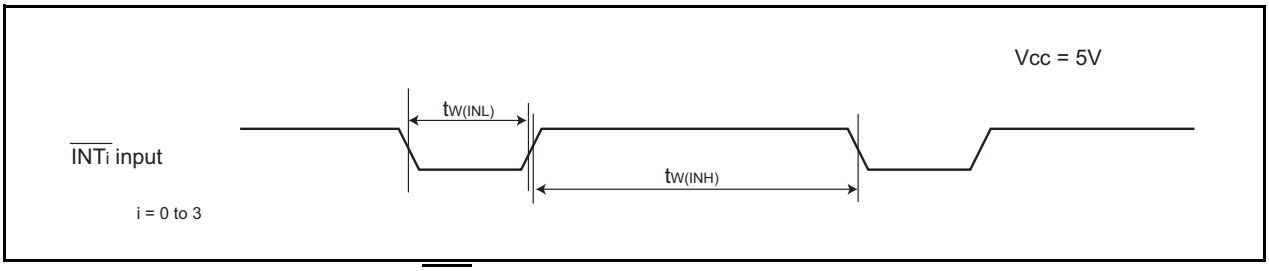


Figure 5.11 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 5 V (i = 0 to 3)