Renesas Electronics America Inc - R5F2123CKFP#U0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, Voltage Detect, WDT
Number of I/O	41
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2123ckfp-u0

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1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

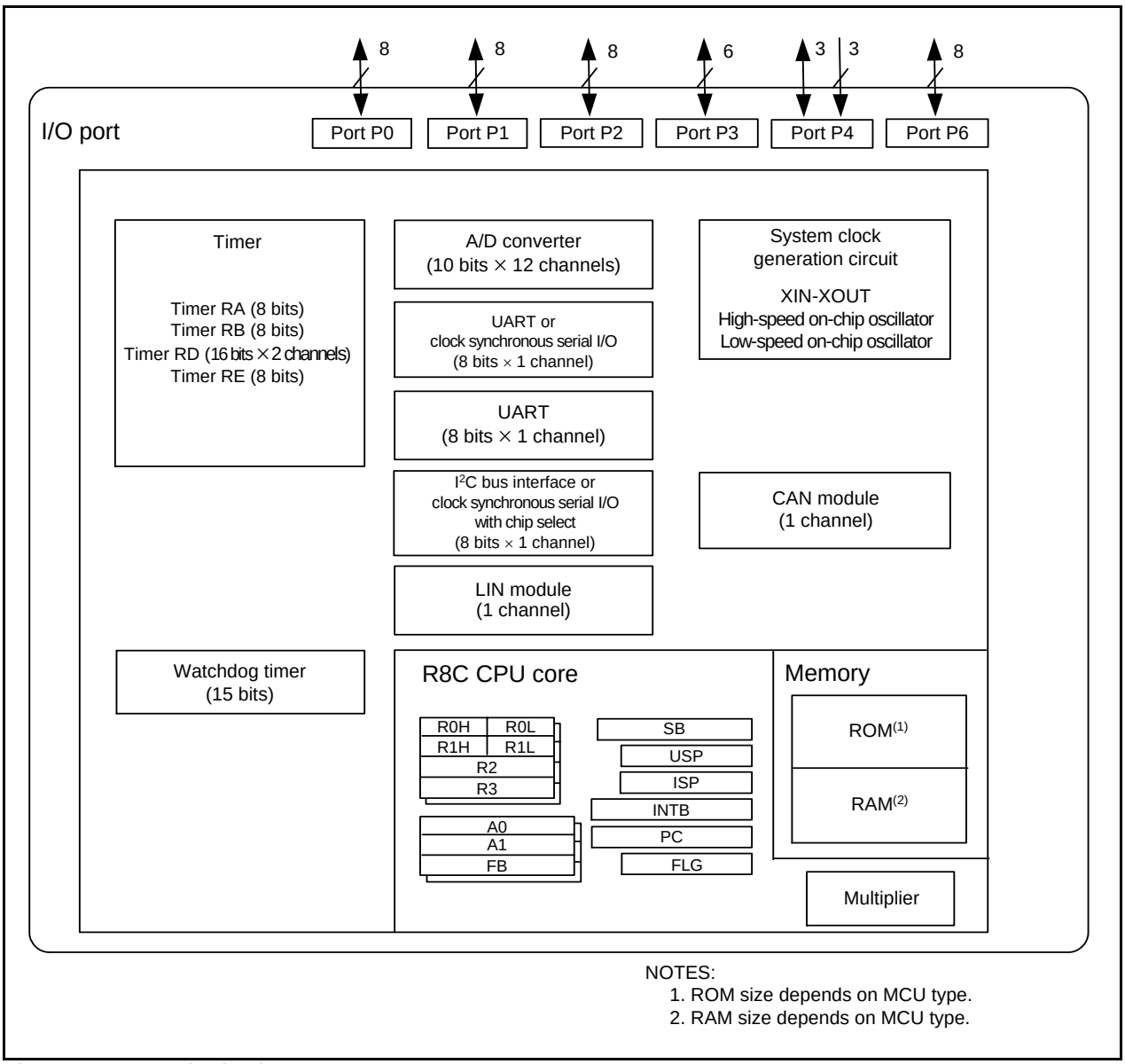


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.3 lists Product Information for R8C/22 Group and Table 1.4 lists Product Information for R8C/23 Group.

Table 1.3 Product Information for R8C/22 Group **Current of Aug. 2008**

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks	
R5F21226DFP	32 Kbytes	2 Kbytes	PLQP0048KB-A	D version	Flash memory version
R5F21227DFP	48 Kbytes	2.5 Kbytes	PLQP0048KB-A		
R5F21228DFP	64 Kbytes	3 Kbytes	PLQP0048KB-A		
R5F21226JFP	32 Kbytes	2 Kbytes	PLQP0048KB-A	J version	
R5F21227JFP	48 Kbytes	2.5 Kbytes	PLQP0048KB-A		
R5F21228JFP	64 Kbytes	3 Kbytes	PLQP0048KB-A		
R5F2122AJFP	96 Kbytes	5 Kbytes	PLQP0048KB-A		
R5F2122CJFP	128 Kbytes(1)	6 Kbytes	PLQP0048KB-A		
R5F21226KFP	32 Kbytes	2 Kbytes	PLQP0048KB-A	K version	
R5F21227KFP	48 Kbytes	2.5 Kbytes	PLQP0048KB-A		
R5F21228KFP	64 Kbytes	3 Kbytes	PLQP0048KB-A		
R5F2122AKFP	96 Kbytes	5 Kbytes	PLQP0048KB-A		
R5F2122CKFP	128 Kbytes(1)	6 Kbytes	PLQP0048KB-A		

NOTE:
1. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **24. Notes on Emulator Debugger** of Hardware Manual.

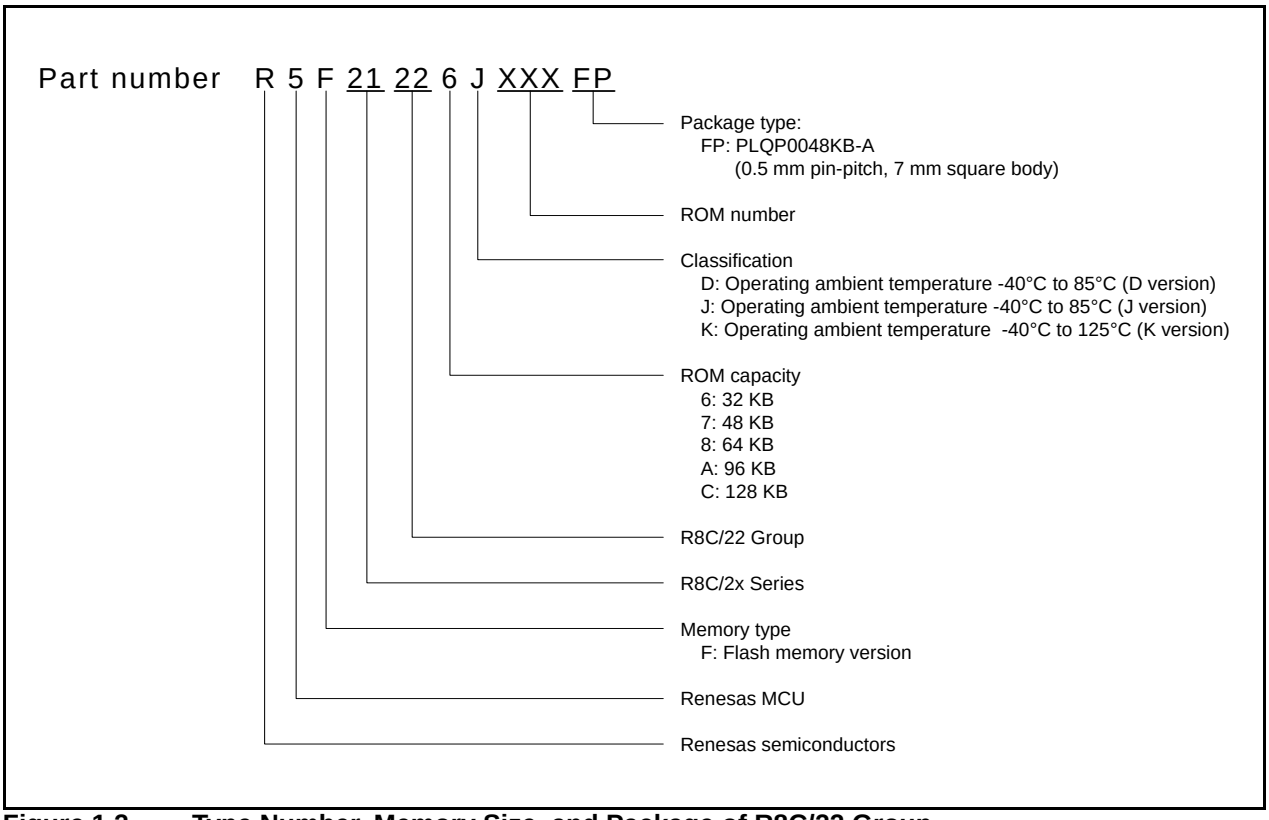
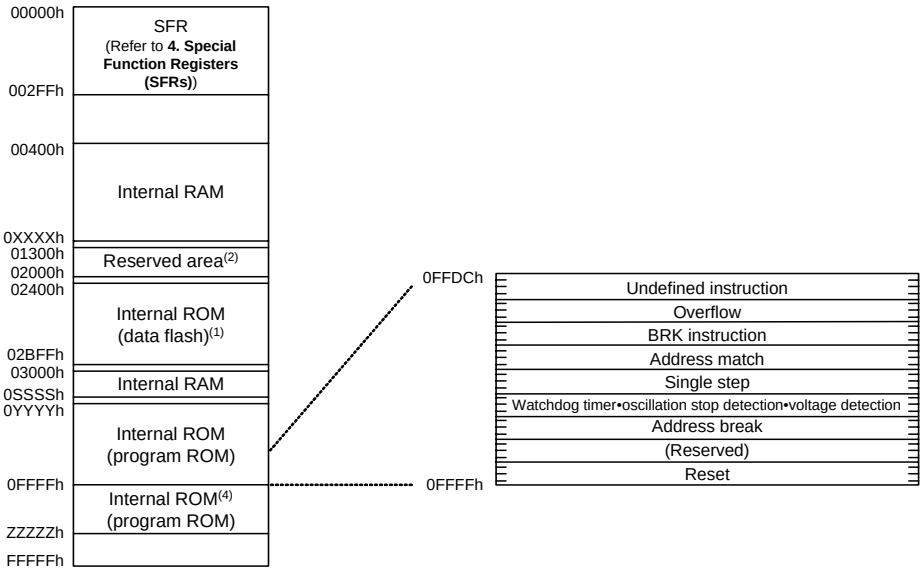


Figure 1.2 Type Number, Memory Size, and Package of R8C/22 Group

3.2 R8C/23 Group

Figure 3.2 shows a Memory Map of R8C/23 Group. The R8C/23 Group has 1 Mbyte of address space from address 00000h to FFFFFh.
The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFR) are allocated addresses 00000h to 002FFh and 01300h to 0147Fh (SFR area for CAN). The peripheral function control registers are allocated them. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTES:
1. Data flash block A (1 Kbyte) and B (1 Kbyte) are shown.
2. SFR area for CAN is allocated addresses 01300h to 0147Fh.
3. The blank regions are reserved. Do not access locations in these regions.
4. Do not use addresses 20000h to 23FFFh because these areas are used for the emulator debugger. Refer to **24. Notes on Emulator Debugger**.

Part Number	Internal ROM			Internal RAM		
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh	Address 0SSSSh
R5F21236DFP, R5F21236JFP, R5F21236KFP	32 Kbytes	08000h	-	2 Kbytes	00BFFh	-
R5F21237DFP, R5F21237JFP, R5F21237KFP	48 Kbytes	04000h	-	2.5 Kbytes	00DFFh	-
R5F21238DFP, R5F21238JFP, R5F21238KFP	64 Kbytes	04000h	13FFFh	3 Kbytes	00FFFh	-
R5F2123AJFP, R5F2123AKFP	96 Kbytes	04000h	1BFFFh	5 Kbytes	00FFFh	037FFh
R5F2123CJFP, R5F2123CKFP	128 Kbytes	04000h	23FFFh	6 Kbytes	00FFFh	03BFFh

Figure 3.2 Memory Map of R8C/23 Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function.
Table 4.1 to Table 4.13 list the SFR Information.

Table 4.1 SFR Information (1)[1]

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protect Mode Register	CSPR	00h 10000000b[8]
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0030h			
0031h	Voltage Detection Register 1[2]	VCA1	00001000b
0032h	Voltage Detection Register 2[6]	VCA2	00h[3] 01000000b[4]
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register[7]	VW1C	0000X000b[3] 0100X001b[4]
0037h	Voltage Monitor 2 Circuit Control Register[5]	VW2C	00h
0038h			
0039h			
003Fh			

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1.
4. Power-on reset, voltage monitor 1 reset or the LVD0ON bit in the OFS register is set to 0.
5. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect b2 and b3.
6. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect b7.
7. Software reset, the watchdog timer rest, and the voltage monitor 2 reset do not affect other than the b0 and b6.
8. The CSPROINI bit in the OFS register is 0.

Table 4.2 SFR Information (2)(1)

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h	CAN0 Wake Up Interrupt Control Register	C01WKIC	XXXXX000b
0044h	CAN0 Successful Reception Interrupt Control Register	C0RECIC	XXXXX000b
0045h	CAN0 Successful Transmission Interrupt Control Register	C0TRMIC	XXXXX000b
0046h	CAN0 State/Error Interrupt Control Register	C01ERRIC	XXXXX000b
0047h			
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register/IIC Bus Interrupt Control Register(2)	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.3 SFR Information (3)(1)

Address	Register	Symbol	After reset
0080h			
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART1 Transmit/Receive Mode Register	U1MR	00h
00A9h	UART1 Bit Rate Register	U1BRG	XXh
00AAh	UART1 Transmit Buffer Register	U1TB	XXh
00ABh			XXh
00ACh	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
00ADh	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
00AEh	UART1 Receive Buffer Register	U1RB	XXh
00AFh			XXh
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h	SS Control Register H/IIC Bus Control Register 1(2)	SSCRH/ICCR1	00h
00B9h	SS Control Register L/IIC Bus Control Register 2(2)	SSCRL/ICCR2	01111101b
00BAh	SS Mode Register/IIC Bus Mode Register 1(2)	SSMR/ICMR	00011000b
00BBh	SS Enable Register/IIC Bus Interrupt Enable Register(2)	SSER/ICIER	00h
00BCh	SS Status Register/IIC Bus Status Register(2)	SSSR/ICSR	00h/0000X000b
00BDh	SS Mode Register 2/Slave Address Register(2)	SSMR2/SAR	00h
00BEh	SS Transmit Data Register/IIC Bus Transmit Data Register(2)	SSTDR/ICDRT	FFh
00BFh	SS Receive Data Register/IIC Bus Receive Data Register(2)	SSRDR/ICDRR	FFh

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.8 SFR Information (8)(1)

Address	Register	Symbol	After reset
1300h	CAN0 Message Control Register 0	C0MCTL0	00h
1301h	CAN0 Message Control Register 1	C0MCTL1	00h
1302h	CAN0 Message Control Register 2	C0MCTL2	00h
1303h	CAN0 Message Control Register 3	C0MCTL3	00h
1304h	CAN0 Message Control Register 4	C0MCTL4	00h
1305h	CAN0 Message Control Register 5	C0MCTL5	00h
1306h	CAN0 Message Control Register 6	C0MCTL6	00h
1307h	CAN0 Message Control Register 7	C0MCTL7	00h
1308h	CAN0 Message Control Register 8	C0MCTL8	00h
1309h	CAN0 Message Control Register 9	C0MCTL9	00h
130Ah	CAN0 Message Control Register 10	C0MCTL10	00h
130Bh	CAN0 Message Control Register 11	C0MCTL11	00h
130Ch	CAN0 Message Control Register 12	C0MCTL12	00h
130Dh	CAN0 Message Control Register 13	C0MCTL13	00h
130Eh	CAN0 Message Control Register 14	C0MCTL14	00h
130Fh	CAN0 Message Control Register 15	C0MCTL15	00h
1310h	CAN0 Control Register	C0CTLR	X0000001b
1311h			XX0X0000b
1312h	CAN0 Status Register	C0STR	00h
1313h			X0000001b
1314h	CAN0 Slot Status Register	C0SSTR	00h
1315h			00h
1316h	CAN0 Interrupt Control Register	C0ICR	00h
1317h			00h
1318h	CAN0 Extended ID Register	C0IDR	00h
1319h			00h
131Ah	CAN0 Configuration Register	C0CONR	XXh
131Bh			XXh
131Ch	CAN0 Receive Error Count Register	C0RECR	00h
131Dh	CAN0 Transmit Error Count Register	C0TECR	00h
131Eh			
131Fh			
1320h			
1321h			
1322h			
1323h			
1324h			
1325h			
1326h			
1327h			
1328h			
1329h			
132Ah			
132Bh			
132Ch			
132Dh			
132Eh			
132Fh			
1330h			
1331h			
1332h			
1333h			
1334h			
1335h			
1336h			
1337h			
1338h			
1339h			
133Ah			
133Bh			
133Ch			
133Dh			
133Eh			
133Fh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.9 SFR Information (9)(1)

Address	Register	Symbol	After reset
1340h			
1341h			
1342h	CAN0 Acceptance Filter Support Register	C0AFS	XXh
1343h			XXh
1344h			
1345h			
1346h			
1347h			
1348h			
1349h			
134Ah			
134Bh			
134Ch			
134Dh			
134Eh			
134Fh			
1350h			
1351h			
1352h			
1353h			
1354h			
1355h			
1356h			
1357h			
1358h			
1359h			
135Ah			
135Bh			
135Ch			
135Dh			
135Eh			
135Fh	CAN0 Clock Select Register	CCLKR	00h
1360h	CAN0 Slot 0: Identifier/DLC		XXh
1361h			XXh
1362h			XXh
1363h			XXh
1364h			XXh
1365h			XXh
1366h	CAN0 Slot 0: Data Field		XXh
1367h			XXh
1368h			XXh
1369h			XXh
136Ah			XXh
136Bh			XXh
136Ch			XXh
136Dh			XXh
136Eh	CAN0 Slot 0: Time Stamp		XXh
136Fh			XXh
1370h	CAN0 Slot 1: Identifier/DLC		XXh
1371h			XXh
1372h			XXh
1373h			XXh
1374h			XXh
1375h			XXh
1376h	CAN0 Slot 1: Data Field		XXh
1377h			XXh
1378h			XXh
1379h			XXh
137Ah			XXh
137Bh			XXh
137Ch			XXh
137Dh			XXh
137Eh	CAN0 Slot 1: Time Stamp		XXh
137Fh			XXh

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V_{CC}/AV_{CC}	Supply voltage		-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC}+0.3	V
V_O	Output voltage		-0.3 to V_{CC}+0.3	V
P_d	Power dissipation	-40°C ≤ Topr ≤ 85°C	300	mW
		85°C < Topr ≤ 125°C	125	mW
T_{opr}	Operating ambient temperature		-40 to 85 (D, J version) / -40 to 125 (K version)	°C
T_{stg}	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage			2.7	–	5.5	V
V_{SS}/AV_{CC}	Supply voltage			–	0	–	V
V_{IH}	Input “H” voltage			0.8V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” voltage			0	–	0.2V_{CC}	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all Pins $I_{OH\ (peak)}$		–	–	-60	mA
$I_{OH(peak)}$	Peak output “H” current			–	–	-10	mA
$I_{OH(avg)}$	Average output “H” current			–	–	-5	mA
$I_{OL(sum)}$	Peak sum output “L” currents	Sum of all Pins $I_{OL\ (peak)}$		–	–	60	mA
$I_{OL(peak)}$	Peak output “L” currents			–	–	10	mA
$I_{OL(avg)}$	Average output “L” current			–	–	5	mA
$f_{(XIN)}$	XIN clock input oscillation frequency		3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	0	–	20	MHz
			3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 125°C	0	–	16	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
–	System clock	OCD2 = 0 When XIN clock is selected.	3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	0	–	20	MHz
			3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 125°C	0	–	16	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz
		OCD2 = 1 When on-chip oscillator clock is selected.	FRA01 = 0 When low-speed on-chip oscillator clock is selected.	–	125	–	kHz
			FRA01 = 1 When high-speed on-chip oscillator clock is selected. 3.0 V ≤ V_{CC} ≤ 5.5 V -40°C ≤ Topr ≤ 85°C	–	–	20	MHz
			FRA01 = 1 When high-speed on-chip oscillator clock is selected.	–	–	10	MHz

NOTES:
1. V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		V_{ref} = AVCC	–	–	10	Bits
–	Absolute Accuracy	10-bit mode	φAD = 10 MHz, V_{ref} = AVCC = 5.0 V	–	–	±3	LSB
		8-bit mode	φAD = 10 MHz, V_{ref} = AVCC = 5.0 V	–	–	±2	LSB
		10-bit mode	φAD = 10 MHz, V_{ref} = AVCC = 3.3 V	–	–	±5	LSB
		8-bit mode	φAD = 10 MHz, V_{ref} = AVCC = 3.3 V	–	–	±2	LSB
R_{ladder}	Resistor ladder		V_{ref} = AVCC	10	–	40	kΩ
t_{conv}	Conversion time	10-bit mode	φAD = 10 MHz, V_{ref} = AVCC = 5.0 V	3.3	–	–	µs
		8-bit mode	φAD = 10 MHz, V_{ref} = AVCC = 5.0 V	2.8	–	–	µs
V_{ref}	Reference voltage			2.7	–	AVCC	V
V_{IA}	Analog input voltage(2)			0	–	AVCC	V
–	A/D operating clock frequency	Without sample & hold		0.25	–	10	MHz
		With sample & hold		1	–	10	MHz

NOTES:
1. VCC = AVCC = 2.7 to 5.5 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. When analog input voltage exceeds reference voltage, A/D conversion result is 3FFh in 10-bit mode, FFh in 8-bit mode.

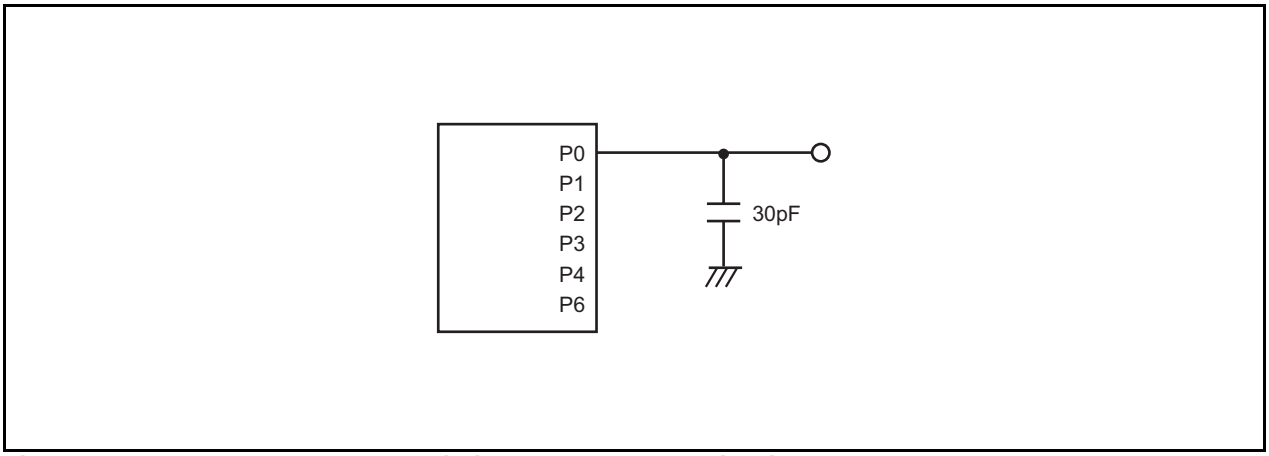


Figure 5.1 Ports P0 to P4, P6 Timing Measurement Circuit

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)	R8C/22 Group	100(3)	–	–	times
		R8C/23 Group	1,000(3)	–	–	times
–	Byte program time		–	50	400	µs
–	Block erase time		–	0.4	9	s
$t_{d(SR-SUS)}$	Time delay from suspend request until erase suspend		–	–	97 + CPU clock × 6 cycle	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3 + CPU clock × 4 cycle	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time(7)	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 1,000), each block can be erased n times.
   For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure endurance can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.5 Flash Memory (Data Flash Block A, Block B) Electrical Characteristics(4)

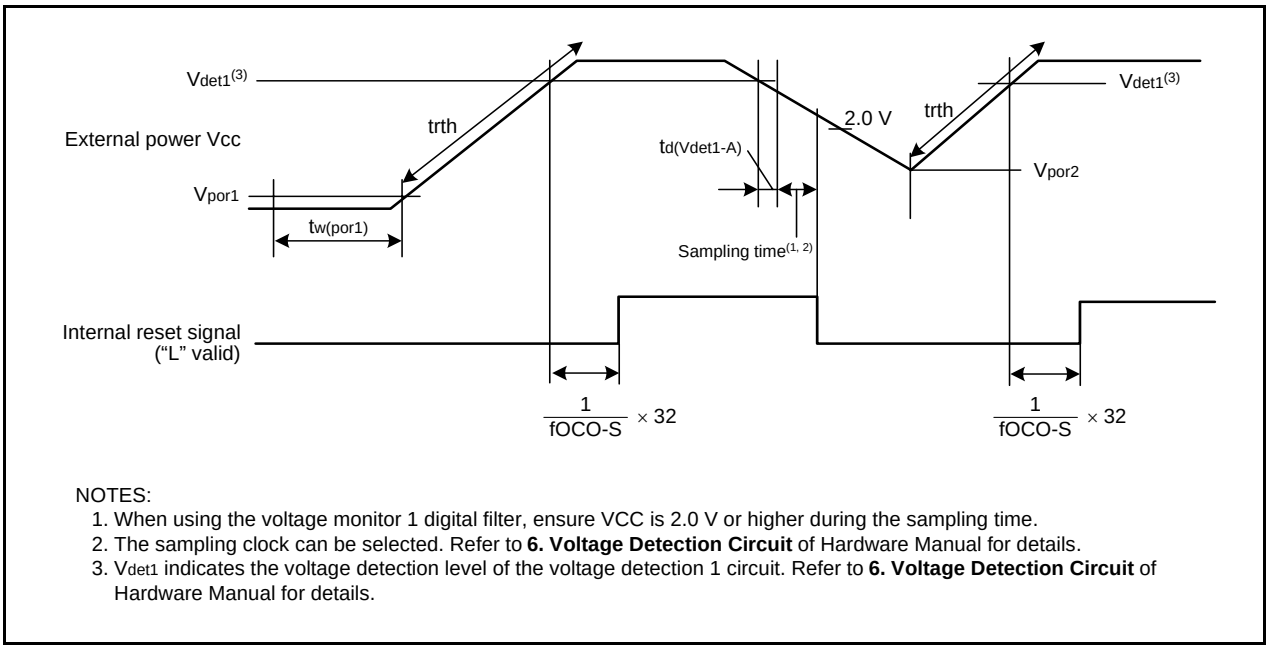
Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)		10,000(3)	–	–	times
–	Byte program time (Program/erase endurance ≤ 1,000 times)		–	50	400	µs
–	Byte program time (Program/erase endurance > 1,000 times)		–	65	–	µs
–	Block erase time (Program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (Program/erase endurance > 1,000 times)		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until erase suspend		–	–	97 + CPU clock × 6 cycle	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3 + CPU clock × 4 cycle	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		-40	–	85(8)	°C
–	Data hold time(9)	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times.
   For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Minimum endurance to guarantee all electrical characteristics after program and erase (1 to Min. value can be guaranteed).
4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times are the same as that in program ROM.
5. In a system that executes multiple programming operations, the actual erasure endurance can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
6. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.
7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
8. 125°C for K version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.8 Power-on Reset Circuit, Voltage Monitor 1 Reset Circuit Electrical Characteristics(3)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage(4)		–	–	0.1	V
V_{por2}	Power-on reset or voltage monitor 1 valid voltage		0	–	Vdet1	V
trth	External power V_{CC} rise gradient	$V_{CC} \leq 3.6$ V	20(2)	–	–	mV/msec
		$V_{CC} > 3.6$ V	20(2)	–	2,000	mV/msec

NOTES:
1. Topr = -40°C to 85°C (D, J version) / -40°C to 125°C (K version), unless otherwise specified.
2. This condition (the minimum value of external power V_{CC} rise gradient) does not apply if $V_{por2} \geq 1.0$ V.
3. To use the power-on reset function, enable voltage monitor 1 reset by setting the LVD1ON bit in the OFS register to 0, the VW1C0 and VW1C6 bits in the VW1C register to 1 respectively, and the VCA26 bit in the VCA2 register to 1.
4. $t_{w(por1)}$ indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain tw(por1) for 30s or more if -20°C ≤ Topr ≤ 125°C, maintain $t_{w(por1)}$ for 3,000s or more if -40°C ≤ Topr < -20°C.



NOTES:
1. When using the voltage monitor 1 digital filter, ensure VCC is 2.0 V or higher during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.
3. V_{det1} indicates the voltage detection level of the voltage detection 1 circuit. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.

Figure 5.3 Power-on Reset Circuit Electrical Characteristics

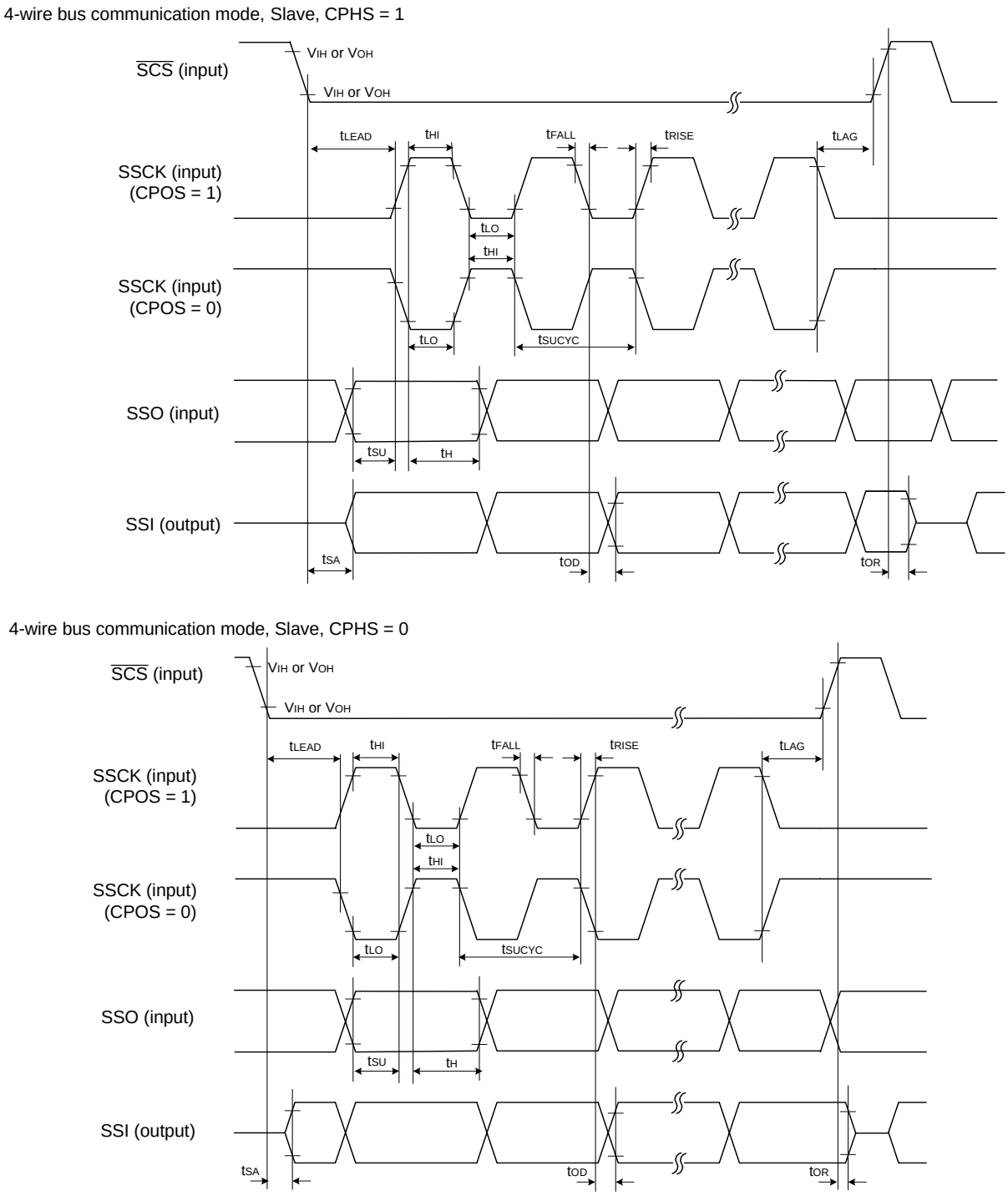


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

Table 5.15 Electrical Characteristics (2) [Vcc = 5 V]
(Topr = -40 to 85°C (D, J version) / -40 to 125°C (K version), Unless Otherwise Specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) In single-chip mode, the output pins are open and other pins are Vss	High-clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	12.5	25.0	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	10.0	20.0	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	6.5	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	6.5	–	mA
			XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	5.0	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.5	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	6.5	13.0	mA
			XIN clock off High-speed on-chip oscillator on fOCO= 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.2	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 FMR47 = 1	–	150	300	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA20 = 0 VCA26 = VCA27 = 0	–	60	120	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA20 = 0 VCA26 = VCA27 = 0	–	38	76	µA
		Stop mode Topr = 25°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	0.8	3.0	µA
		Stop mode Topr = 85°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	1.2	–	µA
		Stop mode Topr = 125°C	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	4.0	–	µA

Timing Requirements (Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C) [Vcc = 5 V]

Table 5.16 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	25	–	ns
$t_{WL(XIN)}$	XIN input “L” width	25	–	ns

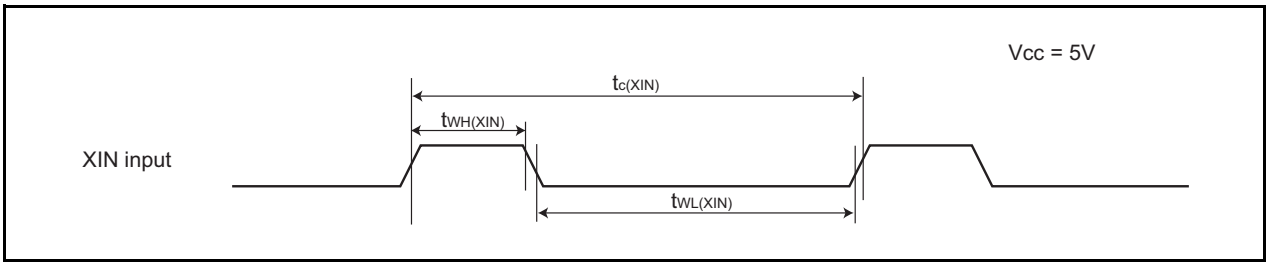


Figure 5.8 XIN Input Timing Diagram when Vcc = 5 V

Table 5.17 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

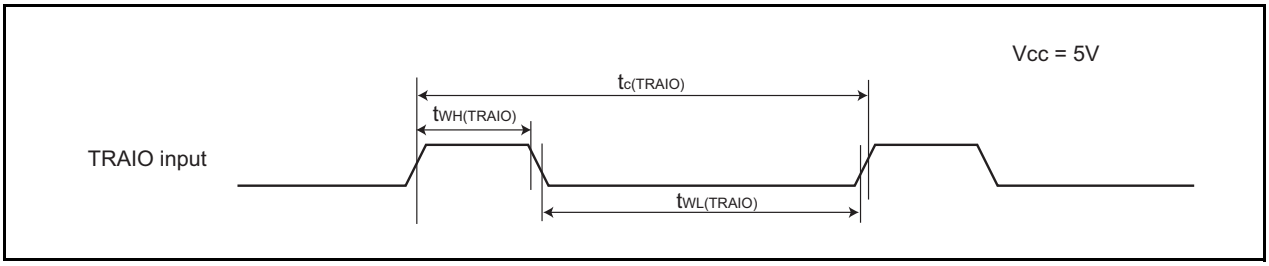


Figure 5.9 TRAIO Input Timing Diagram when Vcc = 5 V

Table 5.18 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	200	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	100	–	ns
$t_{W(CKL)}$	CLK0 input “L” width	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

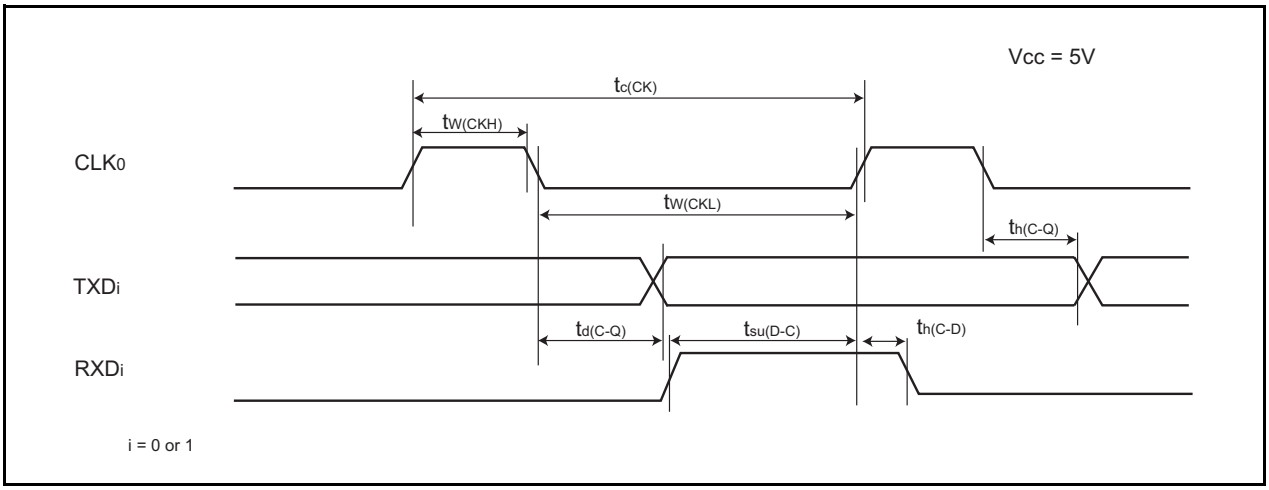


Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.19 External Interrupt $\overline{INTi}$ (i = 0 to 3) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	250(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input HIGH width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use the $\overline{INTi}$ input LOW width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.

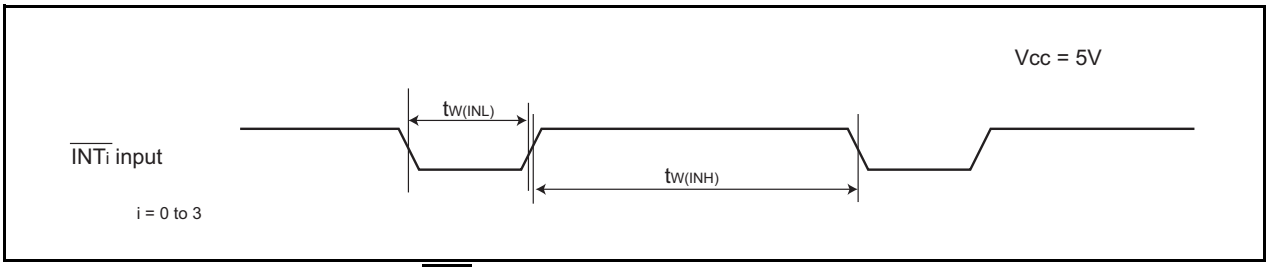


Figure 5.11 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 5 V (i = 0 to 3)

REVISION HISTORY	R8C/22 Group, R8C/23 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.20	Sep 29, 2005	20	Table 4.6 SFR Information (6) revised - 0145h: POCR0 → TRDPOCR0 - 0146h, 0147h: TRDCNT0 → TRD0 - 0148h, 0149h: GRA0 → TRDGRA0 - 014Ah, 014Bh: GRB0 → TRDGRB0 - 014Ch, 014Dh: GRC0 → TRDGRC0 - 014Eh, 014Fh: GRD0 → TRDGRD0 - 0155h: POCR1 -> TRDPOCR1 - 0156h, 0157h: TRDCNT1 → TRD1 - 0158h, 0159h: GRA1 → TRDGRA1 - 015Ah, 015Bh: GRB1 → TRDGRB1 - 015Ch, 015Dh: GRC1 → TRDGRC1 - 015Eh, 015Fh: GRD1 → TRDGRD1
		28	5. Electrical Characteristics added
1.00	Oct 27, 2006	All pages	"Preliminary" and "Under development" deleted
		2	Table 1.1 Functions and Specifications for R8C/22 Group revised. NOTE1 deleted.
		3	Table 1.2 Functions and Specifications for R8C/23 Group revised. NOTE1 deleted.
		5	Table 1.3 Product Information for R8C/22 Group; "R5F2122AJFP (D)", "R5F2122CJFP (D)", "R5F2122AKFP (D)", "R5F2122CKFP (D)", and NOTE added. Figure 1.2 Type Number, Memory Size, and Package of R8C/22 Group; "A: 96 KB" and "C: 128 KB" added.
		6	Table 1.4 Product Information for R8C/23 Group; "R5F2123AJFP (D)", "R5F2123CJFP (D)", "R5F2123AKFP (D)", "R5F2123CKFP (D)", and NOTE added. Figure 1.3 Type Number, Memory Size, and Package of R8C/23 Group; "A: 96 KB" and "C: 128 KB" added.
		13	Figure 3.1 Memory Map of R8C/22 Group revised.
		14	Figure 3.2 Memory Map of R8C/23 Group revised.
		15	Table 4.1 SFR Information (1)(1); NOTE8; "The CSPROINI bit in the OFS register is set to 0." → "The CSPROINI bit in the OFS register is 0." revised.
		28	Table 5.1 Absolute Maximum Ratings; Power dissipation revised. Table 5.2 Recommended Operating Conditions; System clock revised.
		33	Table 5.8 Voltage Monitor 1 Reset Circuit Electrical Characteristics → Table 5.8 Power-on Reset Circuit, Voltage Monitor 1 Reset Circuit Electrical Characteristics(1) replaced. Table 5.8 revised. NOTE3 added. Table 5.9 Power-on Reset Circuit Electrical Characteristics deleted. Figure 5.3 Power-on Reset Circuit Electrical Characteristics revised.
		34	Table 5.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics → Table 5.9 High-Speed On-Chip Oscillator Circuit Electrical Characteristics revised.

REVISION HISTORY	R8C/22 Group, R8C/23 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Oct 27, 2006	40	Table 5.15 Electrical Characteristics (1) [VCC = 5 V] → Table 5.14 Electrical Characteristics (1) [VCC = 5 V] revised. RAM Hold Voltage, Min.; "1.8" → "2.0" corrected.
		41	Table 5.16 Electrical Characteristics (2) [Vcc = 5 V] → Table 5.15 Electrical Characteristics (2) [Vcc = 5 V] revised. Wait mode revised.
		44	Table 5.21 Electrical Characteristics (3) [VCC = 3 V → Table 5.20 Electrical Characteristics (3) [VCC = 3 V] revised. RAM hold voltage, Min.; "1.8" → "2.0" corrected.
		45	Table 5.22 Electrical Characteristics (4) [Vcc = 3 V] → Table 5.21 Electrical Characteristics (4) [Vcc = 3 V] revised. Wait mode revised.
1.10	Mar 16, 2007	–	D version products added. Relevant descriptions revised because of expanding products - Table 1.1 to 1.4 revised. - Figure 1.2 and 1.3 revised. - Figure 3.1 and 3.2 revised. - Table 5.1 to 5.15 revised. - Table 5.20 and 5.21 revised.
		15	Table 4.1 revised; 000Ah: "00XXX000b" → "00h", 000Fh: "00011111b" → "00X11111b"
		42	Table 5.17 and Figure 5.9 revised; "$\overline{\text{INT1}}$ input" deleted
		43	Table 5.19 and Figure 5.11 revised; "i = 0, 2, 3" → "i = 0 to 3"
		46	Table 5.23 and Figure 5.13 revised; "$\overline{\text{INT1}}$ input" deleted
		47	Table 5.25 and Figure 5.15 revised; "i = 0, 2, 3" → "i = 0 to 3"
2.00	Aug 20, 2008	–	"RENESAS TECHNICAL UPDATE" reflected: TN-16C-A172A/E
		5, 6	Table 1.3, Table 1.4 revised Figure 1.2, Figure 1.3; ROM number "XXX" added
		13, 14	Figure 3.1, Figure 3.2; "Expanding area" deleted
		23	Table 4.9 135Fh Address "XXXX0000b" → "00h"
		28	Table 5.2; NOTE2 revised
		30	Table 5.4; NOTE2 and NOTE4 revised
		31	Table 5.5; NOTE2 and NOTE5 revised
		32	Table 5.6; "td(Vdet1-A)" added, NOTE5 added Table 5.7; "td(Vdet2-A)" and NOTE2 revised, NOTE5 added
		33	Table 5.8; "trth" and NOTE2 revised, Figure 5.3 revised