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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/atuc256l3u-aut

The Frequency Meter (FREQM) allows accurate measuring of a clock frequency by comparing it to a known reference clock.

The Full-speed USB 2.0 device interface (USBC) supports several USB classes at the same time, thanks to the rich end-point configuration.

The device includes six identical 16-bit Timer/Counter (TC) channels. Each channel can be independently programmed to perform frequency measurement, event counting, interval measurement, pulse generation, delay timing, and pulse width modulation.

The Pulse Width Modulation controller (PWMA) provides 12-bit PWM channels which can be synchronized and controlled from a common timer. 36 PWM channels are available, enabling applications that require multiple PWM outputs, such as LCD backlight control. The PWM channels can operate independently, with duty cycles set individually, or in interlinked mode, with multiple channels changed at the same time.

The ATUC64/128/256L3/4U also features many communication interfaces, like USART, SPI, and TWI, for communication intensive applications. The USART supports different communication modes, like SPI Mode and LIN Mode.

A general purpose 8-channel ADC is provided, as well as eight analog comparators (AC). The ADC can operate in 10-bit mode at full speed or in enhanced mode at reduced speed, offering up to 12-bit resolution. The ADC also provides an internal temperature sensor input channel. The analog comparators can be paired to detect when the sensing voltage is within or outside the defined reference window.

The Capacitive Touch (CAT) module senses touch on external capacitive touch sensors, using the QTouch technology. Capacitive touch sensors use no external mechanical components, unlike normal push buttons, and therefore demand less maintenance in the user application. The CAT module allows up to 17 touch sensors, or up to 16 by 8 matrix sensors to be interfaced. All touch sensors can be configured to operate autonomously without software interaction, allowing wakeup from sleep modes when activated.

Atmel offers the QTouch library for embedding capacitive touch buttons, sliders, and wheels functionality into AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys as well as Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The easy-to-use QTouch Suite toolchain allows you to explore, develop, and debug your own touch applications.

The Audio Bitstream DAC (ABDACB) converts a 16-bit sample value to a digital bitstream with an average value proportional to the sample value. Two channels are supported, making the ABDAC particularly suitable for stereo audio.

The Inter-IC Sound Controller (IISC) provides a 5-bit wide, bidirectional, synchronous, digital audio link with external audio devices. The controller is compliant with the Inter-IC Sound (I2S) bus specification.

The ATUC64/128/256L3/4U integrates a class 2+ Nexus 2.0 On-chip Debug (OCD) System, with non-intrusive real-time trace and full-speed read/write memory access, in addition to basic runtime control. The NanoTrace interface enables trace feature for aWire- or JTAG-based debuggers. The single-pin aWire interface allows all features available through the JTAG interface to be accessed through the RESET pin, allowing the JTAG pins to be used for GPIO or peripherals.

8.7.1.11 USB Descriptor Address

Register Name: UDESC

Access Type: Read-Write

Offset: 0x0830

Reset Value: -

31	30	29	28	27	26	25	24
UDESCA[31:24]							

23	22	21	20	19	18	17	16
UDESCA[23:16]							

15	14	13	12	11	10	9	8
UDESCA[15:8]							

7	6	5	4	3	2	1	0
UDESCA[7:0]							

- **UDESCA: USB Descriptor Address**
  This field contains the address of the USB descriptor. The three least significant bits are always zero.

14.6.10 DFLLn Configuration Register

Name: DFLLnCONF

Access Type: Read/Write

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
COARSE[7:0]							

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	FINE[8]

15	14	13	12	11	10	9	8
FINE[7:0]							

7	6	5	4	3	2	1	0
-	QLEN	CCEN	-	LLAW	DITHER	MODE	EN

- **COARSE: Coarse Calibration Value**
  Set the value of the coarse calibration register. If in closed loop mode, this field is Read-only.
- **FINE: FINE Calibration Value**
  Set the value of the fine calibration register. If in closed loop mode, this field is Read-only.
- **QLEN: Quick Lock Enable**
  0: Quick Lock is disabled.
  1: Quick Lock is enabled.
- **CCEN: Chill Cycle Enable**
  0: Chill Cycle is disabled.
  1: Chill Cycle is enabled.
- **LLAW: Lose Lock After Wake**
  0: Locks will not be lost after waking up from sleep modes.
  1: Locks will be lost after waking up from sleep modes where the DFLL clock has been stopped.
- **DITHER: Enable Dithering**
  0: The fine LSB input to the VCO is constant.
  1: The fine LSB input to the VCO is dithered to achieve sub-LSB approximation to the correct multiplication ratio.
- **MODE: Mode Selection**
  0: The DFLL is in open loop operation.
  1: The DFLL is in closed loop operation.
- **EN: Enable**
  0: The DFLL is disabled.
  1: The DFLL is enabled.

Note that this register is protected by a lock. To write to this register the UNLOCK register has to be written first. Please refer to the UNLOCK register description for details.

14.6.19 Supply Monitor 33 Calibration Register

Name: SM33

Access Type: Read/Write

Reset Value: -

31	30	29	28	27	26	25	24
-	-	-	-	SAMPFREQ			

23	22	21	20	19	18	17	16
-	-	-	-	-	ONSM	SFV	FCD

15	14	13	12	11	10	9	8
-	-	-	-	CALIB			

7	6	5	4	3	2	1	0
FS	-	-	-	CTRL			

- **SAMPFREQ: Sampling Frequency**
  Selects the sampling mode frequency of the 3.3V supply monitor. In sampling mode, the SM33 performs a measurement every $2^{(SAMPFREQ+5)}$ cycles of the internal 32kHz RC oscillator.
- **ONSM: Supply Monitor On Indicator**
  0: The supply monitor is disabled.
  1: The supply monitor is enabled.
  This bit is read-only. Writing to this bit has no effect.
- **SFV: Store Final Value**
  0: The register is read/write
  1: The register is read-only, to protect against further accidental writes.
  This bit is cleared after a reset.
- **FCD: Flash Calibration Done**
  This bit is cleared after a reset.
  This bit is set when CALIB field has been updated after a reset.
- **CALIB: Calibration Value**
  Calibration Value for the SM33.
- **FS: Force Sampling Mode**
  0: Sampling mode is enabled in DeepStop and Static mode only.
  1: Sampling mode is always enabled.
- **CTRL: Supply Monitor Control**

If ADD is ‘1’, the prescaler frequency is increased:

$$f_{TUNED} = f_0 \left(1 + \frac{1}{\text{roundup}\left(\frac{256}{VALUE}\right) \cdot (2^{EXP}) - 1} \right)$$

Note that for these formulas to be within an error of 0.01%, it is recommended that the prescaler bit that is used as the clock for the counter (selected by CR.PSEL) or to trigger the periodic interrupt (selected by PIRn.INSEL) be bit 6 or higher.

15.5.8 Synchronization

As the prescaler and counter operate asynchronously from the user interface, the AST needs a few clock cycles to synchronize the values written to the CR, CV, SCR, WER, EVE, EVD, PIRn, ARn, and DTR registers. The Busy bit in the Status Register (SR.BUSY) indicates that the synchronization is ongoing. During this time, writes to these registers will be discarded and reading will return a zero value.

Note that synchronization takes place also if the prescaler is clocked from CLK_AST.

16.6.3 Status Register

Name: SR

Access Type: Read-only

Offset: 0x008

Reset Value: 0x00000003

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	-	-	-	CLEARED	WINDOW

- **CLEARED: WDT Counter Cleared**
  This bit is cleared when writing a one to the CLR.WDTCLR bit.
  This bit is set when clearing the WDT counter is done.
- **WINDOW: Within Window**
  This bit is cleared when the WDT counter is inside the TBAN period.
  This bit is set when the WDT counter is inside the PSEL period.

17.7.15 Version Register

Name: VERSION

Access Type: Read-only

Offset: 0x3FC

Reset Value: -

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	VERSION[11:8]			

7	6	5	4	3	2	1	0
VERSION[7:0]							

- **VERSION: Version number**
  Version number of the module. No functionality associated.

Table 19-2. GPIO Register Memory Map

Offset	Register	Function	Register Name	Access	Reset	Config. Protection	Access Protection
0x0C0	Glitch Filter Enable Register	Read/Write	GFER	Read/Write	-[1]	N	N
0x0C4	Glitch Filter Enable Register	Set	GFERS	Write-only		N	N
0x0C8	Glitch Filter Enable Register	Clear	GFERC	Write-only		N	N
0x0CC	Glitch Filter Enable Register	Toggle	GFERT	Write-only		N	N
0x0D0	Interrupt Flag Register	Read	IFR	Read-only	-[1]	N	N
0x0D4	Interrupt Flag Register	-	-	-		N	N
0x0D8	Interrupt Flag Register	Clear	IFRC	Write-only		N	N
0x0DC	Interrupt Flag Register	-	-	-		N	N
0x180	Event Enable Register	Read	EVER	Read/Write	-[1]	N	N
0x184	Event Enable Register	Set	EVERS	Write-only		N	N
0x188	Event Enable Register	Clear	EVERC	Write-only		N	N
0x18C	Event Enable Register	Toggle	EVERT	Write-only		N	N
0x1A0	Lock Register	Read/Write	LOCK	Read/Write	-[1]	N	Y
0x1A4	Lock Register	Set	LOCKS	Write-only		N	N
0x1A8	Lock Register	Clear	LOCKC	Write-only		N	Y
0x1AC	Lock Register	Toggle	LOCKT	Write-only		N	Y
0x1E0	Unlock Register	Read/Write	UNLOCK	Write-only		N	N
0x1E4	Access Status Register	Read/Write	ASR	Read/Write			N
0x1F8	Parameter Register	Read	PARAMETER	Read-only	-[1]	N	N
0x1FC	Version Register	Read	VERSION	Read-only	-[1]	N	N

Note: 1. The reset values for these registers are device specific. Please refer to the Module Configuration section at the end of this chapter.

20.7.9 Baud Rate Generator Register

Name: BRGR

Access Type: Read-write

Offset: 0x20

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	FP		

15	14	13	12	11	10	9	8
CD[15:8]							

7	6	5	4	3	2	1	0
CD[7:0]							

This register can only be written to if write protection is disabled, see ”Write Protect Mode Register” on page 482.

- **FP: Fractional Part**
  0: Fractional divider is disabled.
  1 - 7: Baud rate resolution, defined by FP x 1/8.
- **CD: Clock Divider**

Table 20-17.

	SYNC = 0		**SYNC = 1 or MODE = SPI (Master or Slave)**	
CD	**OVER = 0**	**OVER = 1**		
0	Baud Rate Clock Disabled			
1 to 65535	Baud Rate = Selected Clock/16/CD	Baud Rate = Selected Clock/8/CD	Baud Rate = Selected Clock /CD	

21.8.9 Chip Select Register 0

Name: CSR0

Access Type: Read/Write

Offset: 0x30

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
DLYBCT							

23	22	21	20	19	18	17	16
DLYBS							

15	14	13	12	11	10	9	8
SCBR							

7	6	5	4	3	2	1	0
BITS				CSAAT	CSNAAT	NCPHA	CPOL

- **DLYBCT: Delay Between Consecutive Transfers**

  This field defines the delay between two consecutive transfers with the same peripheral without removing the chip select. The delay is always inserted after each transfer and before removing the chip select if needed.

  When DLYBCT equals zero, no delay between consecutive transfers is inserted and the clock keeps its duty cycle over the character transfers.

  Otherwise, the following equation determines the delay:

$$\text{Delay Between Consecutive Transfers} = \frac{32 \times DLYBCT}{CLKSPI}$$

- **DLYBS: Delay Before SPCK**

  This field defines the delay from NPCS valid to the first valid SPCK transition.

  When DLYBS equals zero, the NPCS valid to SPCK transition is 1/2 the SPCK clock period.

  Otherwise, the following equations determine the delay:

$$\text{Delay Before SPCK} = \frac{DLYBS}{CLKSPI}$$

- **SCBR: Serial Clock Baud Rate**

  In Master Mode, the SPI Interface uses a modulus counter to derive the SPCK baud rate from the CLK_SPI. The Baud rate is selected by writing a value from 1 to 255 in the SCBR field. The following equations determine the SPCK baud rate:

$$\text{SPCK Baudrate} = \frac{CLKSPI}{SCBR}$$

  Writing the SCBR field to zero is forbidden. Triggering a transfer while SCBR is zero can lead to unpredictable results.

  At reset, SCBR is zero and the user has to write it to a valid value before performing the first transfer.

  If a clock divider (SCBRn) field is set to one and the other SCBR fields differ from one, access on CSn is correct but no correct access will be possible on other CS.

the increase event will decrease the duty cycle value and decrease event will increase the duty cycle value. If both the increase event and the decrease event occur at the same time for a channel, the duty cycle value will not be changed.

The number of channels supporting input peripheral events is device specific. Please refer to the Module Configuration section at the end of this chapter for details.

25.6.10.2 Output Peripheral Event

The PWMA also supports one output peripheral event (event_ch0) to the Peripheral Event System. This output peripheral event is connected to channel 0 and will be asserted when the timebase counter reaches the duty cycle value for channel 0. This output event is always enabled.

25.7.17 Interlinked Multiple Value Duty0/1/2/3 Register

Name: DUTY0/1/2/3

Access Type: Write-only

Offset: 0x80-0x8C

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	DUTY[11:8]			

7	6	5	4	3	2	1	0
DUTY[7:0]							

These registers allows up to 4 channels to be updated with a common 12-bits duty cycle value at a time. They are the extension of the IMDUTY register which only supports updating the least significant 8 bits of the duty registers for up to 4 channels.

- **DUTY: Duty Cycle Value**
  The duty cycle value written to this field will be updated to the channel specified by IMCHSEL.
  DUTY0 is specified by IMCHSEL.SEL0, DUTY1 is specified by IMCHSEL.SEL1, and so on.

29. ADC Interface (ADCIFB)

Rev:1.0.1.1

29.1 Features

- **Multi-channel Analog-to-Digital Converter with up to 12-bit resolution**
- **Enhanced Resolution Mode**
  - **11-bit resolution obtained by interpolating 4 samples**
  - **12-bit resolution obtained by interpolating 16 samples**
- **Glueless interface with resistive touch screen panel, allowing**
  - **Resistive Touch Screen position measurement**
  - **Pen detection and pen loss detection**
- **Integrated enhanced sequencer**
  - **ADC Mode**
  - **Resistive Touch Screen Mode**
- **Numerous trigger sources**
  - **Software**
  - **Embedded 16-bit timer for periodic trigger**
  - **Pen detect trigger**
  - **Continuous trigger**
  - **External trigger, rising, falling, or any-edge trigger**
  - **Peripheral event trigger**
- **ADC Sleep Mode for low power ADC applications**
- **Programmable ADC timings**
  - **Programmable ADC clock**
  - **Programmable startup time**

29.2 Overview

The ADC Interface (ADCIFB) converts analog input voltages to digital values. The ADCIFB is based on a Successive Approximation Register (SAR) 10-bit Analog-to-Digital Converter (ADC). The conversions extend from 0V to ADVREFP.

The ADCIFB supports 8-bit and 10-bit resolution mode, in addition to enhanced resolution mode with 11-bit and 12-bit resolution. Conversion results are reported in a common register for all channels.

The 11-bit and 12-bit resolution modes are obtained by interpolating multiple samples to acquire better accuracy. For 11-bit mode 4 samples are used, which gives an effective sample rate of 1/4 of the actual sample frequency. For 12-bit mode 16 samples are used, giving a effective sample rate of 1/16 of actual. This arrangement allows conversion speed to be traded for better accuracy.

Conversions can be started for all enabled channels, either by a software trigger, by detection of a level change on the external trigger pin (TRIGGER), or by an integrated programmable timer.

When the Resistive Touch Screen Mode is enabled, an integrated sequencer automatically configures the pad control signals and performs resistive touch screen conversions.

The ADCIFB also integrates an ADC Sleep Mode, a Pen-Detect Mode, and an Analog Compare Mode, and connects with one Peripheral DMA Controller channel. These features reduce both power consumption and processor intervention.

29.10 Module Configuration

The specific configuration for each ADCIFB instance is listed in the following tables.The module bus clocks listed here are connected to the system bus clocks. Please refer to the Power Manager chapter for details.

Table 29-5. Module Configuration

Feature	ADCIFB
Number of ADC channels	9 (8 + 1 internal temperature sensor channel)

Table 29-6. ADCIFB Clocks

Clock Name	Description
CLK_ADCIFB	Clock for the ADCIFB bus interface

Table 29-7. Register Reset Values

Register	Reset Value
VERSION	0x00000110
PARAMETER	0x000003FF

Table 29-8. ADC Input Channels[1]

Channel	Input
CH0	AD0
CH1	AD1
CH2	AD2
CH4	AD4
CH5	AD5
CH6	AD6
CH7	AD7
CH8	AD8
CH9	Temperature sensor

Note: 1. AD3 does not exist

30.9 User Interface

Table 30-4. ACIFB Register Memory Map

Offset	Register	Register Name	Access	Reset
0x00	Control Register	CTRL	Read/Write	0x00000000
0x04	Status Register	SR	Read-only	0x00000000
0x10	Interrupt Enable Register	IER	Write-only	0x00000000
0x14	Interrupt Disable Register	IDR	Write-only	0x00000000
0x18	Interrupt Mask Register	IMR	Read-only	0x00000000
0x1C	Interrupt Status Register	ISR	Read-only	0x00000000
0x20	Interrupt Status Clear Register	ICR	Write-only	0x00000000
0x24	Test Register	TR	Read/Write	0x00000000
0x30	Parameter Register	PARAMETER	Read-only	-(1)
0x34	Version Register	VERSION	Read-only	-(1)
0x80	Window0 Configuration Register	CONFW0	Read/Write	0x00000000
0x84	Window1 Configuration Register	CONFW1	Read/Write	0x00000000
0x88	Window2 Configuration Register	CONFW2	Read/Write	0x00000000
0x8C	Window3 Configuration Register	CONFW3	Read/Write	0x00000000
0xD0	AC0 Configuration Register	CONF0	Read/Write	0x00000000
0xD4	AC1 Configuration Register	CONF1	Read/Write	0x00000000
0xD8	AC2 Configuration Register	CONF2	Read/Write	0x00000000
0xDC	AC3 Configuration Register	CONF3	Read/Write	0x00000000
0xE0	AC4 Configuration Register	CONF4	Read/Write	0x00000000
0xE4	AC5 Configuration Register	CONF5	Read/Write	0x00000000
0xE8	AC6 Configuration Register	CONF6	Read/Write	0x00000000
0xEC	AC7 Configuration Register	CONF7	Read/Write	0x00000000

Note: 1. The reset values for these registers are device specific. Please refer to the Module Configuration section at the end of this chapter.

31.7.26 Autonomous Touch Current Count Register

Name: ATCURR

Access Type: Read-only

Offset: 0x70

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-							

23	22	21	20	19	18	17	16
-							

15	14	13	12	11	10	9	8
COUNT[15:8]							

7	6	5	4	3	2	1	0
COUNT[7:0]							

- **COUNT: Count value**
  The current count acquired by the autonomous touch sensor. This is useful for autonomous touch debugging purposes.

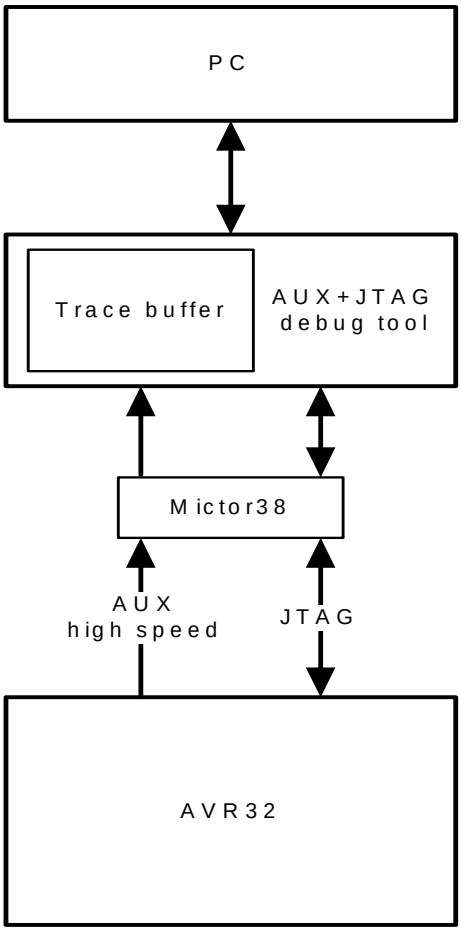
33.7 User Interface

Table 33-2. aWire UART user interface Register Memory Map

Offset	Register	Register Name	Access	Reset
0x00	Control Register	CTRL	Read/Write	0x00000000
0x04	Status Register	SR	Read-only	0x00000000
0x08	Status Clear Register	SCR	Write-only	-
0x0C	Interrupt Enable Register	IER	Write-only	-
0x10	Interrupt Disable Register	IDR	Write-only	-
0x14	Interrupt Mask Register	IMR	Read-only	0x00000000
0x18	Receive Holding Register	RHR	Read-only	0x00000000
0x1C	Transmit Holding Register	THR	Read/Write	0x00000000
0x20	Baud Rate Register	BRR	Read/Write	0x00000000
0x24	Version Register	VERSION	Read-only	-(1)
0x28	Clock Request Register	CLKR	Read/Write	0x00000000

Note: 1. The reset values are device specific. Please refer to the Module Configuration section at the end of this chapter.

Figure 34-4. AUX+JTAG Based Debugger



34.3.8.1 *Trace Operation*

Trace features are enabled by writing OCD registers by the debugger. The OCD extracts the trace information from the CPU, compresses this information and formats it into variable-length messages according to the Nexus standard. The messages are buffered in a 16-frame transmit queue, and are output on the AUX port one frame at a time.

The trace features can be configured to be very selective, to reduce the bandwidth on the AUX port. In case the transmit queue overflows, error messages are produced to indicate loss of data. The transmit queue module can optionally be configured to halt the CPU when an overflow occurs, to prevent the loss of messages, at the expense of longer run-time for the program.

34.3.8.2 *Program Trace*

Program trace allows the debugger to continuously monitor the program execution in the CPU. Program trace messages are generated for every branch in the program, and contains compressed information, which allows the debugger to correlate the message with the source code to identify the branch instruction and target address.

34.3.8.3 *Data Trace*

Data trace outputs a message every time a specific location is read or written. The message contains information about the type (read/write) and size of the access, as well as the address and data of the accessed location. The ATUC64/128/256L3/4U contains two data trace chan-

Figure 35-15. SPI Master Mode with (CPOL= 0 and NCPHA= 1) or (CPOL= 1 and NCPHA= 0)

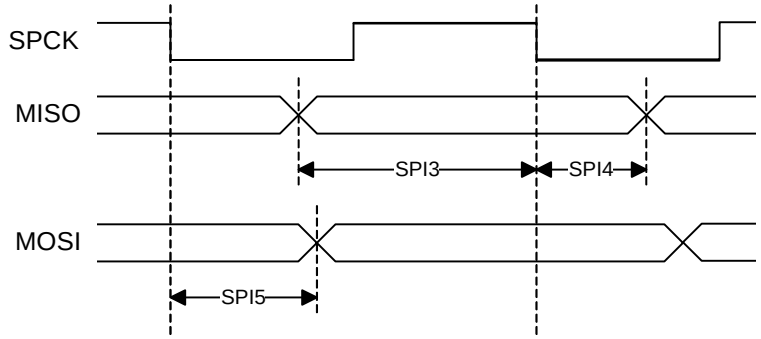


Table 35-43. SPI Timing, Master Mode[1]

Symbol	Parameter	Conditions	Min	Max	Units
SPI0	MISO setup time before SPCK rises	V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF	33.4 + (t_{CLK_SPI})/2		ns
SPI1	MISO hold time after SPCK rises		0		
SPI2	SPCK rising to MOSI delay			7.1	
SPI3	MISO setup time before SPCK falls		29.2 + (t_{CLK_SPI})/2		
SPI4	MISO hold time after SPCK falls		0		
SPI5	SPCK falling to MOSI delay			8.63	

Note: 1. These values are based on simulation and characterization of other AVR microcontrollers manufactured in the same process technology. These values are not covered by test limits in production.

Maximum SPI Frequency, Master Output

The maximum SPI master output frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(f_{PINMAX}, \frac{1}{SPIn})$$

Where $SPIn$ is the MOSI delay, SPI2 or SPI5 depending on CPOL and NCPHA. f_{PINMAX} is the maximum frequency of the SPI pins. Please refer to the I/O Pin Characteristics section for the maximum frequency of the pins.

Maximum SPI Frequency, Master Input

The maximum SPI master input frequency is given by the following formula:

$$f_{SPCKMAX} = \frac{1}{SPIn + t_{VALID}}$$

Where $SPIn$ is the MISO setup and hold time, SPI0 + SPI1 or SPI3 + SPI4 depending on CPOL and NCPHA. t_{VALID} is the SPI slave response time. Please refer to the SPI slave datasheet for t_{VALID} .