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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/atuc64l4u-aur

3.3 Signal Descriptions

The following table gives details on signal name classified by peripheral.

Table 3-7. Signal Descriptions List

Signal Name	Function	Type	Active Level	Comments
Audio Bitstream DAC - ABDACB				
CLK	D/A Clock out	Output		
DAC1 - DAC0	D/A Bitstream out	Output		
DACN1 - DACN0	D/A Inverted bitstream out	Output		
Analog Comparator Interface - ACIFB				
ACAN3 - ACAN0	Negative inputs for comparators "A"	Analog		
ACAP3 - ACAP0	Positive inputs for comparators "A"	Analog		
ACBN3 - ACBN0	Negative inputs for comparators "B"	Analog		
ACBP3 - ACBP0	Positive inputs for comparators "B"	Analog		
ACREFN	Common negative reference	Analog		
ADC Interface - ADCIFB				
AD8 - AD0	Analog Signal	Analog		
ADP1 - ADP0	Drive Pin for resistive touch screen	Output		
TRIGGER	External trigger	Input		
aWire - AW				
DATA	aWire data	I/O		
DATAOUT	aWire data output for 2-pin mode	I/O		
Capacitive Touch Module - CAT				
CSA16 - CSA0	Capacitive Sense A	I/O		
CSB16 - CSB0	Capacitive Sense B	I/O		
DIS	Discharge current control	Analog		
SMP	SMP signal	Output		
SYNC	Synchronize signal	Input		
VDIVEN	Voltage divider enable	Output		
External Interrupt Controller - EIC				
NMI (EXTINT0)	Non-Maskable Interrupt	Input		
EXTINT5 - EXTINT1	External interrupt	Input		
Glue Logic Controller - GLOC				
IN7 - IN0	Inputs to lookup tables	Input		
OUT1 - OUT0	Outputs from lookup tables	Output		
Inter-IC Sound (I2S) Controller - IISC				

7. Peripheral DMA Controller (PDCA)

Rev: 1.2.3.1

7.1 Features

- **Multiple channels**
- **Generates transfers between memories and peripherals such as USART and SPI**
- **Two address pointers/counters per channel allowing double buffering**
- **Performance monitors to measure average and maximum transfer latency**
- **Optional synchronizing of data transfers with extenal peripheral events**
- **Ring buffer functionality**

7.2 Overview

The Peripheral DMA Controller (PDCA) transfers data between on-chip peripheral modules such as USART, SPI and memories (those memories may be on- and off-chip memories). Using the PDCA avoids CPU intervention for data transfers, improving the performance of the microcontroller. The PDCA can transfer data from memory to a peripheral or from a peripheral to memory.

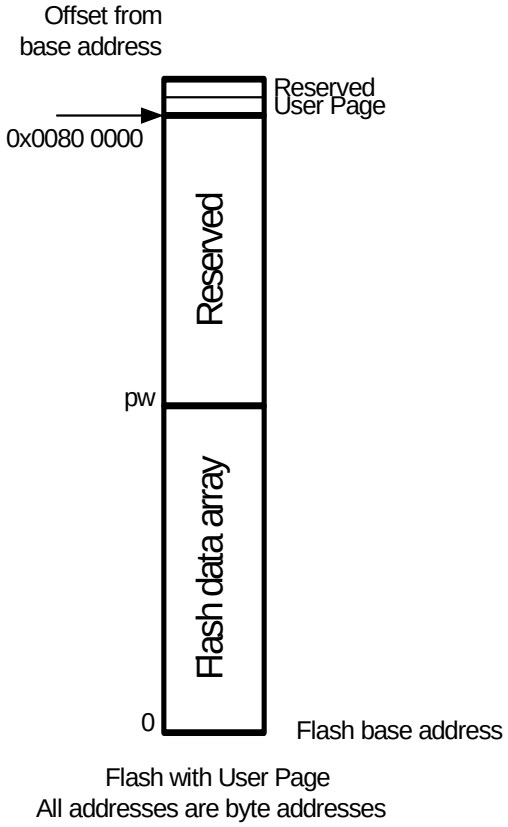
The PDCA consists of multiple DMA channels. Each channel has:

- A Peripheral Select Register
- A 32-bit memory pointer
- A 16-bit transfer counter
- A 32-bit memory pointer reload value
- A 16-bit transfer counter reload value

The PDCA communicates with the peripheral modules over a set of handshake interfaces. The peripheral signals the PDCA when it is ready to receive or transmit data. The PDCA acknowledges the request when the transmission has started.

When a transmit buffer is empty or a receive buffer is full, an optional interrupt request can be generated.

Figure 9-1. Memory Map for the Flash Memories



9.4.5 High Speed Read Mode

The flash provides a High Speed Read Mode, offering slightly higher flash read speed at the cost of higher power consumption. Two dedicated commands, High Speed Read Mode Enable (HSEN) and High Speed Read Mode Disable (HSDIS) control the speed mode. The High Speed Mode (HSMODE) bit in the Flash Status Register (FSR) shows which mode the flash is in. After reset, the High Speed Mode is disabled, and must be manually enabled if the user wants to.

Refer to the Electrical Characteristics chapter at the end of this datasheet for details on the maximum clock frequencies in Normal and High Speed Read Mode.

11.6 Module Configuration

The specific configuration for each HMATRIX instance is listed in the following tables.The module bus clocks listed here are connected to the system bus clocks. Please refer to the Power Manager chapter for details.

Table 11-3. HMATRIX Clocks

Clock Name	Description
CLK_HMATRIX	Clock for the HMATRIX bus interface

11.6.1 Bus Matrix Connections

The bus matrix has the several masters and slaves. Each master has its own bus and its own decoder, thus allowing a different memory mapping per master. The master number in the table below can be used to index the HMATRIX control registers. For example, HMATRIX MCFG0 register is associated with the CPU Data master interface.

Table 11-4. High Speed Bus Masters

Master 0	CPU Data
Master 1	CPU Instruction
Master 2	CPU SAB
Master 3	SAU
Master 4	PDCA
Master 5	USBC

Each slave has its own arbiter, thus allowing a different arbitration per slave. The slave number in the table below can be used to index the HMATRIX control registers. For example, SCFG3 is associated with the Internal SRAM Slave Interface.

Accesses to unused areas returns an error result to the master requesting such an access.

Table 11-5. High Speed Bus Slaves

Slave 0	Internal Flash
Slave 1	HSB-PB Bridge A
Slave 2	HSB-PB Bridge B
Slave 3	Internal SRAM
Slave 4	SAU

abled in certain sleep modes to reduce power consumption, as described in the Power Manager chapter.

After a hard reset, or when waking up from a sleep mode where the oscillators were disabled, the oscillator will need a certain amount of time to stabilize on the correct frequency. This start-up time can be set in the OSCCTRLn register.

The SCIF masks the oscillator outputs during the start-up time, to ensure that no unstable clocks propagate to the digital logic.

The OSCn Ready bit in the Power and Clock Status Register (PCLKSR.OSCnRDY) is set when the oscillator is stable and ready to be used as clock source. An interrupt can be generated on a zero-to-one transition on OSCnRDY if the OSCnRDY bit in the Interrupt Mask Register (IMR.OSCnRDY) is set. This bit is set by writing a one to the corresponding bit in the Interrupt Enable Register (IER.OSCnRDY).

14.5.2 32KHz Oscillator (OSC32K) Operation

Rev: 1.1.0.1

The 32KHz oscillator operates as described for the oscillator above. The 32KHz oscillator can be used as source clock for the Asynchronous Timer (AST) and the Watchdog Timer (WDT). The 32KHz oscillator can also be used as source for the generic clocks.

The oscillator is disabled by default after reset. When the oscillator is disabled, the XIN32 and XOUT32 pins can be used as general-purpose I/Os. When the oscillator is enabled, the XIN32 and XOUT32 pins are controlled directly by the SCIF, overriding GPIO settings. When the oscillator is configured to use an external clock, the clock must be applied to the XIN32 pin while the XOUT32 pin can be used as general-purpose I/O.

The oscillator is enabled writing a one to the OSC32 Enable bit in the 32KHz Oscillator Control Register (OSCCTRL32OSC32EN). The oscillator is disabled by writing a zero to the OSC32EN bit, while keeping the other bits unchanged. Writing to OSC32EN while also writing to other bits may result in unpredictable behavior. Operation mode (external clock or crystal) is selected by writing to the Oscillator Mode bit in OSCCTRL32 (OSCCTRL32.MODE). The oscillator is an ultra-low-power design and remains enabled in all sleep modes.

The start-up time of the 32KHz oscillator is selected by writing to the Oscillator Start-up Time field in the OSCCTRL32 register (OSCCTRL32.STARTUP). The SCIF masks the oscillator output during the start-up time, to ensure that no unstable clock cycles propagate to the digital logic.

The OSC32 Ready bit in the Power and Clock Status Register (PCLKSR.OSC32RDY) is set when the oscillator is stable and ready to be used as clock source. An interrupt can be generated on a zero-to-one transition on PCLKSR.OSC32RDY if the OSC32RDY bit in the Interrupt Mask Register (IMR.OSC32RDY) is set. This bit is set by writing a one to the corresponding bit in the Interrupt Enable Register (IER.OSC32RDY).

.As a crystal oscillator usually requires a very long start-up time (up to 1 second), the 32KHz oscillator will keep running across resets, except a Power-on Reset (POR).

The 32KHz oscillator also has a 1KHz output. This is enabled by writing a one to the Enable 1KHz output bit in OSCCTRL32 register (OSCCTRL32.EN1K). If the 32KHz output clock is not needed when 1K is enabled, this can be disabled by writing a zero to the Enable 32KHz output bit in the OSCCTRL32 register (OSCCTRL32.EN32K). OSCCTRL32.EN32K is set after a POR.

The 32KHz oscillator has two possible sets of pins. To select between them write to the Pin Select bit in the OSCCTRL32 register (OSCCTRL32.PINSEL). If the 32KHz oscillator is to be

- **MODE: Oscillator Mode**

Table 14-4. Operation Mode for 32 KHz Oscillator

MODE	Description
0	External clock connected to XIN32, XOUT32 can be used as general-purpose I/O (no crystal)
1	Crystal mode. Crystal is connected to XIN32/XOUT32.
2	Reserved
3	Reserved
4	Crystal and high current mode. Crystal is connected to XIN32/XOUT32.
5	Reserved
6	Reserved
7	Reserved

- **EN1K: 1 KHz output Enable**
  0: The 1 KHz output is disabled.
  1: The 1 KHz output is enabled.
- **EN32K: 32 KHz output Enable**
  0: The 32 KHz output is disabled.
  1: The 32 KHz output is enabled.
- **PINSEL: Pins Select**
  0: Default pins used.
  1: Alternate pins: XIN32_2 pin is used instead of XIN32 pin, XOUT32_2 pin is used instead of XOUT32.
- **OSC32EN: 32 KHz Oscillator Enable**
  0: The 32 KHz Oscillator is disabled
  1: The 32 KHz Oscillator is enabled

14.6.26 High Resolution Prescaler Control Register

Name: HRPCR

Access Type: Read/Write

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
HRCOUNT[23:16]							

23	22	21	20	19	18	17	16
HRCOUNT[15:8]							

15	14	13	12	11	10	9	8
HRCOUNT[7:0]							

7	6	5	4	3	2	1	0
-	-	-	-	CKSEL			HRPEN

- **HRCOUNT: High Resolution Counter**
  Specify the input clock period to count to generate the output clock edge.
  HRCOUNT can be written to dynamically in order to tune the HRPCLK frequency on-the-go.
- **CKSEL: Clock input selection**
  This field selects the Clock input for the prescaler. See the “HRP clock sources” table in the SCIF Module Configuration section for details. It must not be changed if the HRPEN is one.
- **HRPEN: High Resolution Prescaler Enable**
  0: The High Resolution Prescaler is disabled.
  1: The High Resolution Prescaler is enabled.

14.6.36 Brown-Out Detector Version Register

Name: BODIFAVERSION

Access Type: Read-only

Offset: 0x03D4

Reset Value: -

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	VARIANT			

15	14	13	12	11	10	9	8
-	-	-	-	VERSION[11:8]			

7	6	5	4	3	2	1	0
VERSION[7:0]							

- **VARIANT: Variant number**
  Reserved. No functionality associated.
- **VERSION: Version number**
  Version number of the module. No functionality associated.

15.6 User Interface

Table 15-1. AST Register Memory Map

Offset	Register	Register Name	Access	Reset
0x00	Control Register	CR	Read/Write	0x00000000
0x04	Counter Value	CV	Read/Write	0x00000000
0x08	Status Register	SR	Read-only	0x00000000
0x0C	Status Clear Register	SCR	Write-only	0x00000000
0x10	Interrupt Enable Register	IER	Write-only	0x00000000
0x14	Interrupt Disable Register	IDR	Write-only	0x00000000
0x18	Interrupt Mask Register	IMR	Read-only	0x00000000
0x1C	Wake Enable Register	WER	Read/write	0x00000000
0x20	Alarm Register 0(2)	AR0	Read/Write	0x00000000
0x24	Alarm Register 1(2)	AR1	Read/Write	0x00000000
0x30	Periodic Interval Register 0(2)	PIR0	Read/Write	0x00000000
0x34	Periodic Interval Register 1(2)	PIR1	Read/Write	0x00000000
0x40	Clock Control Register	CLOCK	Read/Write	0x00000000
0x44	Digital Tuner Register	DTR	Read/Write	0x00000000
0x48	Event Enable	EVE	Write-only	0x00000000
0x4C	Event Disable	EVD	Write-only	0x00000000
0x50	Event Mask	EVM	Read-only	0x00000000
0x54	Calendar Value	CALV	Read/Write	0x00000000
0xF0	Parameter Register	PARAMETER	Read-only	-(1)
0xFC	Version Register	VERSION	Read-only	-(1)

Note: 1. The reset values are device specific. Please refer to the Module Configuration section at the end of this chapter.

2. The number of Alarm and Periodic Interval registers are device specific. Please refer to the Module Configuration section at the end of this chapter.

15.6.2 Counter Value

Name: CV

Access Type: Read/Write

Offset: 0x04

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
VALUE[31:24]							

23	22	21	20	19	18	17	16
VALUE[23:16]							

15	14	13	12	11	10	9	8
VALUE[15:8]							

7	6	5	4	3	2	1	0
VALUE[7:0]							

When the SR.BUSY bit is set, writes to this register will be discarded and this register will read as zero.

- **VALUE: AST Value**
  The current value of the AST counter.

20.6.8.1 Master Node Configuration

The Peripheral DMA Controller Mode bit (LINMR.PDCM) allows the user to select configuration:

- PDCM=0: LIN configuration must be written to LINMR, it is not stored in the write buffer.
- PDCM=1: LIN configuration is written by the DMA Controller to THR, and is stored in the write buffer. Since data transfer size is a byte, the transfer is split into two accesses. The first writes the NACT, PARDIS, CHKDIS, CHKTYP, DLM and FSDIS bits, while the second writes the DLC field. If NACT=PUBLISH, the write buffer will also contain the Identifier.

When NACT=SUBSCRIBE, the read buffer contains the data.

Figure 20-33. Master Node with Peripheral DMA Controller (PDCM=0)

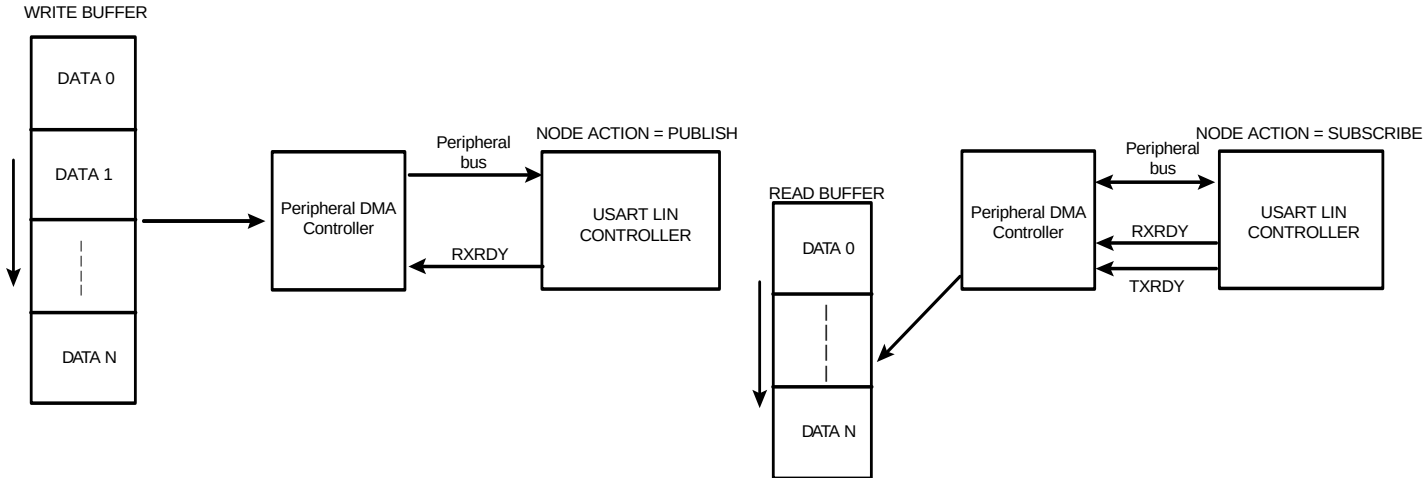


Figure 20-34. Master Node with Peripheral DMA Controller (PDCM=1)

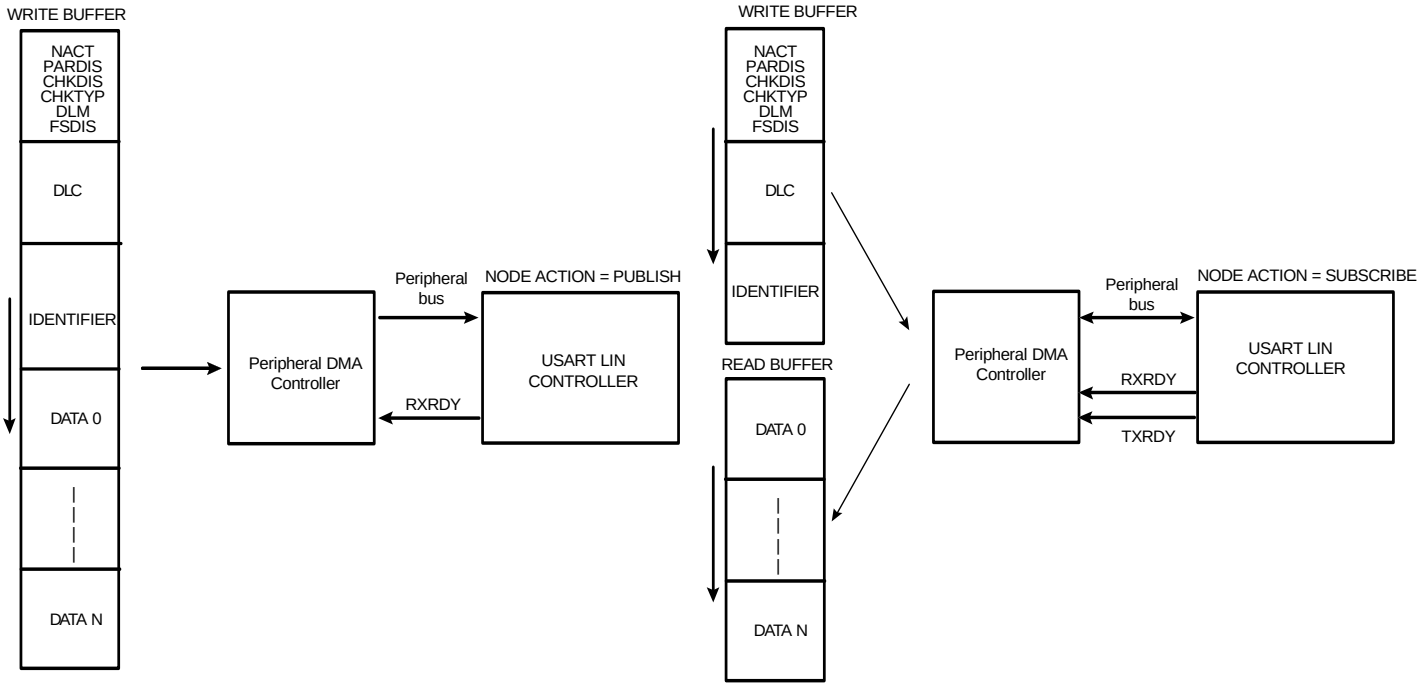
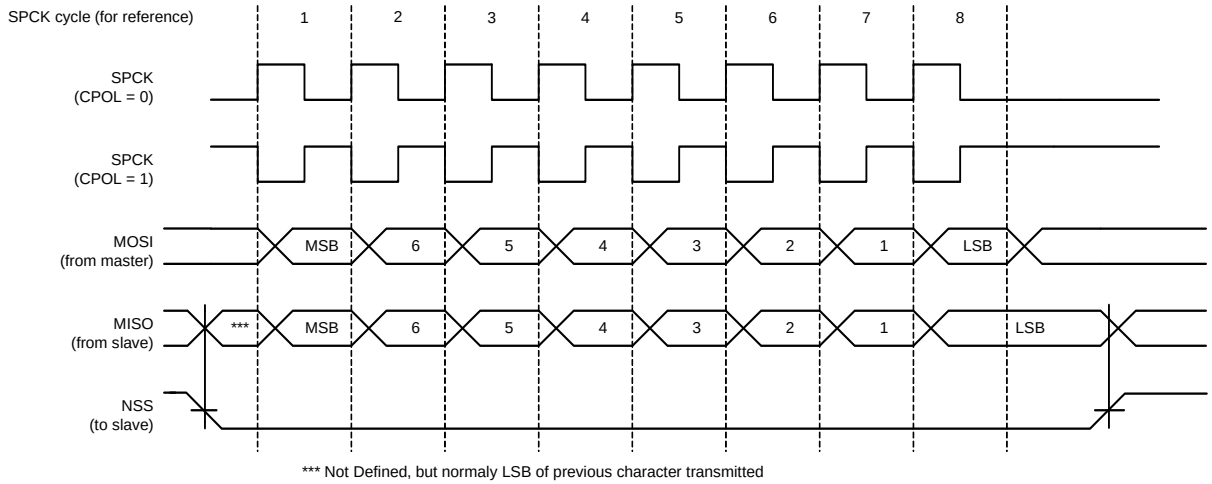


Figure 21-4. SPI Transfer Format (NCPHA = 0, 8 bits per transfer)



21.7.3 Master Mode Operations

When configured in master mode, the SPI uses the internal programmable baud rate generator as clock source. It fully controls the data transfers to and from the slave(s) connected to the SPI bus. The SPI drives the chip select line to the slave and the serial clock signal (SPCK).

The SPI features two holding registers, the Transmit Data Register (TDR) and the Receive Data Register (RDR), and a single Shift Register. The holding registers maintain the data flow at a constant rate.

After enabling the SPI, a data transfer begins when the processor writes to the TDR register. The written data is immediately transferred in the Shift Register and transfer on the SPI bus starts. While the data in the Shift Register is shifted on the MOSI line, the MISO line is sampled and shifted in the Shift Register. Transmission cannot occur without reception.

Before writing to the TDR, the Peripheral Chip Select field in TDR (TDR.PCS) must be written in order to select a slave.

If new data is written to TDR during the transfer, it stays in it until the current transfer is completed. Then, the received data is transferred from the Shift Register to RDR, the data in TDR is loaded in the Shift Register and a new transfer starts.

The transfer of a data written in TDR in the Shift Register is indicated by the Transmit Data Register Empty bit in the Status Register (SR.TDRE). When new data is written in TDR, this bit is cleared. The SR.TDRE bit is used to trigger the Transmit Peripheral DMA Controller channel.

The end of transfer is indicated by the Transmission Registers Empty bit in the SR register (SR.TXEMPTY). If a transfer delay (CSRn.DLYBCT) is greater than zero for the last transfer, SR.TXEMPTY is set after the completion of said delay. The CLK_SPI can be switched off at this time.

During reception, received data are transferred from the Shift Register to the reception FIFO. The FIFO can contain up to 4 characters (both Receive Data and Peripheral Chip Select fields). While a character of the FIFO is unread, the Receive Data Register Full bit in SR remains high (SR.RDRF). Characters are read through the RDR register. If the four characters stored in the FIFO are not read and if a new character is stored, this sets the Overrun Error Status bit in the SR register (SR.OVRES). The procedure to follow in such a case is described in Section 21.7.3.8.

- **IDLE: Master Interface is Idle**
  This bit is one when no command is in progress, and no command waiting to be issued.
  Otherwise, this bit is cleared.
- **CCOMP: Command Complete**
  This bit is one when the current command has completed successfully.
  This bit is zero if the command failed due to conditions such as a NAK receved from slave.
  This bit is cleared by writing 1 to the corresponding bit in the Status Clear Register (SCR).
- **CRDY: Ready for More Commands**
  This bit is one when CMDR and/or NCMDR is ready to receive one or more commands.
  This bit is cleared when this is no longer true.
- **TXRDY: THR Data Ready**
  This bit is one when THR is ready for one or more data bytes.
  This bit is cleared when this is no longer true (i.e. THR is full or transmission has stopped).
- **RXRDY: RHR Data Ready**
  This bit is one when RX data are ready to be read from RHR.
  This bit is cleared when this is no longer true.

22.10 Module Configuration

The specific configuration for each TWIM instance is listed in the following tables.The module bus clocks listed here are connected to the system bus clocks. Please refer to the Power Manager chapter for details.

Table 22-7. Module Clock Name

Module Name	Clock Name	Description
TWIM0	CLK_TWIM0	Clock for the TWIM0 bus interface
TWIM1	CLK_TWIM1	Clock for the TWIM1 bus interface

Table 22-8. Register Reset Values

Register	Reset Value
VERSION	0x00000110
PARAMETER	0x00000000

23.9.9 Interrupt Disable Register

Name: IDR

Access Type: Write-only

Offset: 0x20

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
BTF	REP	STO	SMBDAM	SMBHHM	SMBALERTM	GCM	SAM

15	14	13	12	11	10	9	8
-	BUSERR	SMBPECERR	SMBTOUT	-	-	-	NAK

7	6	5	4	3	2	1	0
ORUN	URUN	-	-	TCOMP	-	TXRDY	RXRDY

Writing a zero to a bit in this register has no effect.
Writing a one to a bit in this register will clear the corresponding bit in IMR.

30.9.9 Parameter Register

Name: PARAMETER

Access Type: Read-only

Offset: 0x30

Reset Value: -

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-
23	22	21	20	19	18	17	16
-	-	-	-	WIMPL3	WIMPL2	WIMPL1	WIMPL0
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
ACIMPL7	ACIMPL6	ACIMPL5	ACIMPL4	ACIMPL3	ACIMPL2	ACIMPL1	ACIMPL0

- **WIMPLn: Window Pair n Implemented**
  0: Window Pair not implemented.
  1: Window Pair implemented.
- **ACIMPLn: Analog Comparator n Implemented**
  0: Analog Comparator not implemented.
  1: Analog Comparator implemented.

Table 31-2. Pin Selection Guide

CAT Module Pin Name	QTouch Method Pin Name	QMatrix Method Pin Name	Selection Bit in PINMODEx Register
CSB8	SNSK8	X9	SP8
CSA9	SNS9	Y4	SP9
CSB9	SNSK9	YK4	SP9
CSA10	SNS10	X10	SP10
CSB10	SNSK10	X11	SP10
CSA11	SNS11	Y5	SP11
CSB11	SNSK11	YK5	SP11
CSA12	SNS12	X12	SP12
CSB12	SNSK12	X13	SP12
CSA13	SNS13	Y6	SP13
CSB13	SNSK13	YK6	SP13
CSA14	SNS14	X14	SP14
CSB14	SNSK14	X15	SP14
CSA15	SNS15	Y7	SP15
CSB15	SNSK15	YK7	SP15
CSA16	SNS16	X16	SP16
CSB16	SNSK16	X17	SP16

31.5.2 Clocks

The clock for the CAT module, CLK_CAT, is generated by the Power Manager (PM). This clock is turned on by default, and can be enabled and disabled in the PM. The user must ensure that CLK_CAT is enabled before using the CAT module.

QMatrix operations also require the CAT generic clock, GCLK_CAT. This generic clock is generated by the System Control Interface (SCIF), and is shared between the CAT and the Analog Comparator Interface. The user must ensure that the GCLK_CAT is enabled in the SCIF before using QMatrix functionality in the CAT module. For proper QMatrix operation, the frequency of GCLK_CAT must be less than half the frequency of CLK_CAT. If only QTouch functionality is used, then GCLK_CAT is unnecessary.

31.5.3 Interrupts

The CAT interrupt request line is connected to the interrupt controller. Using CAT interrupts requires the interrupt controller to be programmed first.

31.5.4 Peripheral Events

The CAT peripheral events are connected via the Peripheral Event System. Refer to the Peripheral Event System chapter for details.

31.5.5 Peripheral Direct Memory Access

The CAT module provides handshake capability for a Peripheral DMA Controller. One handshake controls transfers from the Acquired Count Register (ACOUNT) to memory. A second handshake requests burst lengths for each (X,Y) pair to the Matrix Burst Length Register

32.7.2 Truth Table Register n

Name: TRUTHn

Access Type: Read/Write

Offset: 0x04+n*0x08

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
TRUTH[15:8]							

7	6	5	4	3	2	1	0
TRUTH[7:0]							

- **TRUTH: Truth Table Value**

  This value defines the output OUT as a function of inputs IN:
  OUT = TRUTH[IN]

This bit is set when the clock is disabled.

This bit is cleared when the clock is enabled.

- **BUSY: Synchronizer Busy**

  0: The asynchronous interface is ready to accept more data.

  1: The asynchronous interface is busy and will block writes to CTRL, BRR, and THR.

  This bit is set when the asynchronous interface becomes busy.

  This bit is cleared when the asynchronous interface becomes ready.

37. Ordering Information

Table 37-1. Ordering Information

Device	Ordering Code	Carrier Type	Package	Package Type	Temperature Operating Range
ATUC256L3U	ATUC256L3U-AUTES	ES	TQFP 64	JESD97 Classification E3	N/A
	ATUC256L3U-AUT	Tray			Industrial (-40°C to 85°C)
	ATUC256L3U-AUR	Tape & Reel			
	ATUC256L3U-Z3UTES	ES	QFN 64		N/A
	ATUC256L3U-Z3UT	Tray			Industrial (-40°C to 85°C)
	ATUC256L3U-Z3UR	Tape & Reel			
ATUC128L3U	ATUC128L3U-AUT	Tray	TQFP 64	JESD97 Classification E3	Industrial (-40°C to 85°C)
	ATUC128L3U-AUR	Tape & Reel			
	ATUC128L3U-Z3UT	Tray	QFN 64		
	ATUC128L3U-Z3UR	Tape & Reel			
ATUC64L3U	ATUC64L3U-AUT	Tray	TQFP 64	JESD97 Classification E3	Industrial (-40°C to 85°C)
	ATUC64L3U-AUR	Tape & Reel			
	ATUC64L3U-Z3UT	Tray	QFN 64		
	ATUC64L3U-Z3UR	Tape & Reel			