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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HCS12X
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	91
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.75V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s912xdq256f1mal

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http://freescale.com/

A full list of family members and options is included in the appendices.

Read page 29 first to understand the maskset specific chapters of this document

This document contains information for all constituent modules, with the exception of the S12X CPU. For S12X CPU information please refer to the CPU S12X Reference Manual.

2.3.1 Module Memory Map

Table 2-1 gives an overview on all CRG registers.

Table 2-1. CRG Memory Map

Address Offset	Use	Access
0x_00	CRG Synthesizer Register (SYNR)	R/W
0x_01	CRG Reference Divider Register (REFDV)	R/W
0x_02	CRG Test Flags Register (CTFLG)[1]	R/W
0x_03	CRG Flags Register (CRGFLG)	R/W
0x_04	CRG Interrupt Enable Register (CRGINT)	R/W
0x_05	CRG Clock Select Register (CLKSEL)	R/W
0x_06	CRG PLL Control Register (PLLCTL)	R/W
0x_07	CRG RTI Control Register (RTICTL)	R/W
0x_08	CRG COP Control Register (COPCTL)	R/W
0x_09	CRG Force and Bypass Test Register (FORBYP)[2]	R/W
0x_0A	CRG Test Control Register (CTCTL)[3]	R/W
0x_0B	CRG COP Arm/Timer Reset (ARMCOP)	R/W

1 CTFLG is intended for factory test purposes only.

2 FORBYP is intended for factory test purposes only.

3 CTCTL is intended for factory test purposes only.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

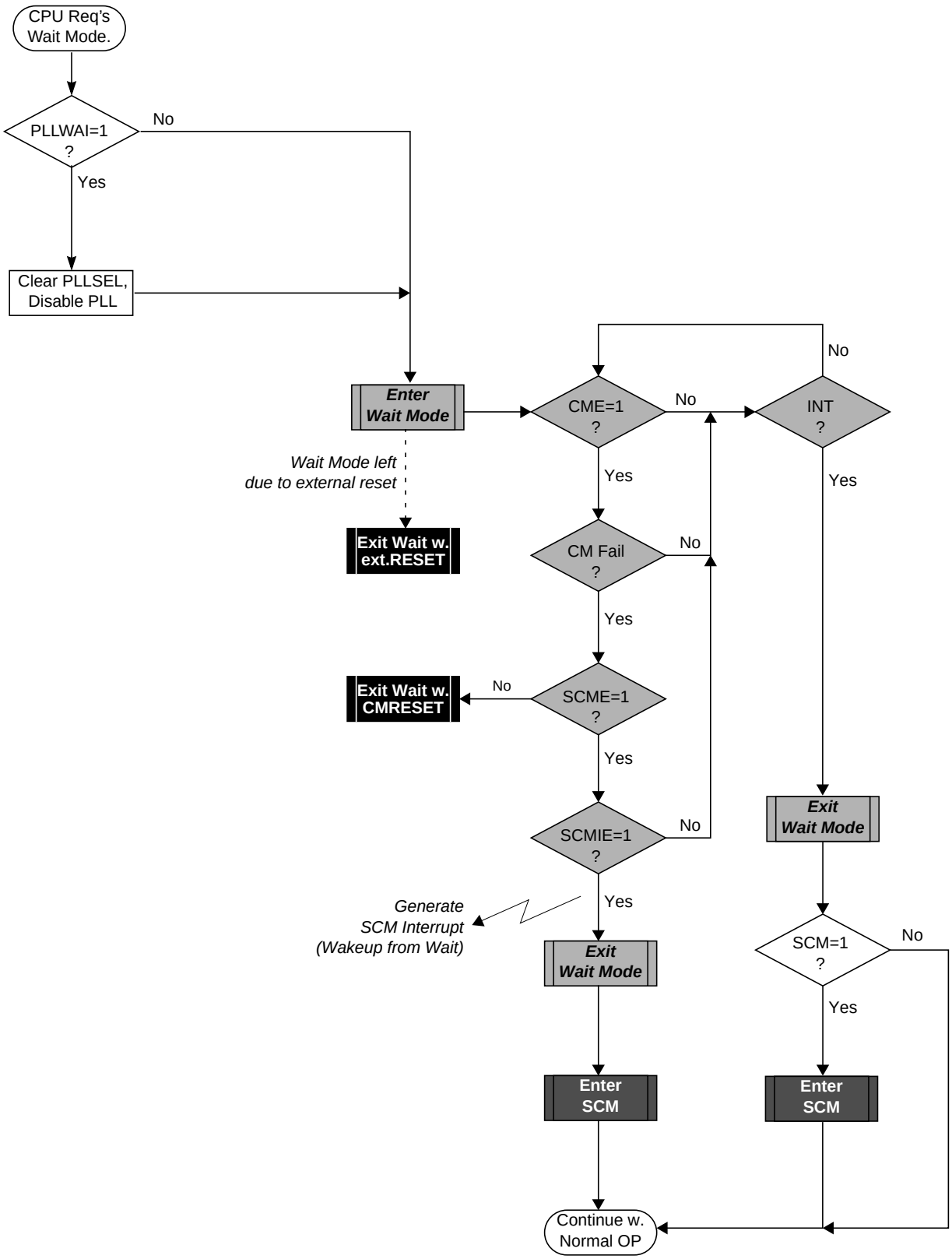

Figure 2-21. Wait Mode Entry/Exit Sequence

Special XGATE channel that is not associated with any peripheral service request. A Software Channel is triggered by its Software Trigger Bit which is implemented in the XGATE module.

XGATE Semaphore

A set of hardware flip-flops that can be exclusively set by either the S12X_CPU or the XGATE. (see 6.4.4/6-204)

XGATE Thread

A code sequence which is executed by the XGATE's RISC core after receiving an XGATE request.

XGATE Debug Mode

A special mode in which the XGATE's RISC core is halted for debug purposes. This mode enables the XGATE's debug features (see 6.6/6-206).

XGATE Software Error

The XGATE is able to detect a number of error conditions caused by erratic software (see 6.4.5/6-205). These error conditions will cause the XGATE to seize program execution and flag an Interrupt to the S12X_CPU.

Word

A 16 bit entity.

Byte

An 8 bit entity.

6.1.2 Features

The XGATE module includes these features:

- Data movement between various targets (i.e Flash, RAM, and peripheral modules)
- Data manipulation through built in RISC core
- Provides up to 112 XGATE channels
  - 104 hardware triggered channels
  - 8 software triggered channels
- Hardware semaphores which are shared between the S12X_CPU and the XGATE module
- Able to trigger S12X_CPU interrupts upon completion of an XGATE transfer
- Software error detection to catch erratic application code

6.1.3 Modes of Operation

There are four run modes on S12X devices.

- Run mode, wait mode, stop mode

  The XGATE is able to operate in all of these three system modes. Clock activity will be automatically stopped when the XGATE module is idle.
- Freeze mode (BDM active)

LDH — Load Immediate 8 bit Constant (High Byte) — LDH

Operation

IMM8 ⇒ RD.H;

Loads an eight bit immediate constant into the high byte of register RD. The low byte is not affected.

CCR Effects

N	Z	V	C
—	—	—	—

N: Not affected.
Z: Not affected.
V: Not affected.
C: Not affected.

Code and CPU Cycles

Source Form	Address Mode	Machine Code							Cycles
LDH RD, #IMM8	IMM8	1	1	1	1	1	RD	IMM8	P

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
TC6 (High)	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	W								
TC6 (Low)	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	W								
TC7 (High)	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	W								
TC7 (Low)	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	W								
PACTL	R	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PA0VI	PAI
	W								
PAFLG	R	0	0	0	0	0	0	PA0VF	PAIF
	W								
PACN3	R	PACNT7(15)	PACNT6(14)	PACNT5(13)	PACNT4(12)	PACNT3(11)	PACNT2(10)	PACNT1(9)	PACNT0(8)
	W								
PACN2	R	PACNT7	PACNT6	PACNT5	PACNT4	PACNT3	PACNT2	PACNT1	PACNT0
	W								
PACN1	R	PACNT7(15)	PACNT6(14)	PACNT5(13)	PACNT4(12)	PACNT3(11)	PACNT2(10)	PACNT1(9)	PACNT0(8)
	W								
PACN0	R	PACNT7	PACNT6	PACNT5	PACNT4	PACNT3	PACNT2	PACNT1	PACNT0
	W								
MCCTL	R	MCZI	MODMC	RDMCL	0	0	MCEN	MCPR1	MCPR0
	W				ICLAT	FLMC			
MCFLG	R	MCZF	0	0	0	POLF3	POLF2	POLF1	POLF0
	W								
ICPAR	R	0	0	0	0	PA3EN	PA2EN	PA1EN	PA0EN
	W								
DLYCT	R	DLY7	DLY6	DLY5	DLY4	DLY3	DLY2	DLY1	DLY0
	W								
ICOVW	R	NOVW7	NOVW6	NOVW5	NOVW4	NOVW3	NOVW2	NOVW1	NOVW0
	W								

= Unimplemented or Reserved

Figure 7-2. ECT Register Summary (Sheet 3 of 5)

7.3.2.9 Timer Control Register 3/Timer Control Register 4 (TCTL3/TCTL4)

	7	6	5	4	3	2	1	0
R W	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
Reset	0	0	0	0	0	0	0	0

Figure 7-13. Timer Control Register 3 (TCTL3)

	7	6	5	4	3	2	1	0
R W	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
Reset	0	0	0	0	0	0	0	0

Figure 7-14. Timer Control Register 4 (TCTL4)

Read or write: Anytime

All bits reset to zero.

Table 7-11. TCTL3/TCTL4 Field Descriptions

Field	Description
EDG[7:0]B 7, 5, 3, 1	**Input Capture Edge Control** — These eight pairs of control bits configure the input capture edge detector circuits for each input capture channel. The four pairs of control bits in TCTL4 also configure the input capture edge control for the four 8-bit pulse accumulators PAC0–PAC3.EDG0B and EDG0A in TCTL4 also determine the active edge for the 16-bit pulse accumulator PACB. See Table 7-12.
EDG[7:0]A 6, 4, 2, 0	

Table 7-12. Edge Detector Circuit Configuration

EDGxB	EDGxA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge (rising or falling)

7.3.2.23 Input Control Overwrite Register (ICOVW)

	7	6	5	4	3	2	1	0
R W	NOVW7	NOVW6	NOVW5	NOVW4	NOVW3	NOVW2	NOVW1	NOVW0
Reset	0	0	0	0	0	0	0	0

Figure 7-45. Input Control Overwrite Register (ICOVW)

Read: Anytime

Write: Anytime

All bits reset to zero.

Table 7-29. ICOVW Field Descriptions

Field	Description
7:0 NOVW[7:0]	**No Input Capture Overwrite** 0 The contents of the related capture register or holding register can be overwritten when a new input capture or latch occurs. 1 The related capture register or holding register cannot be written by an event unless they are empty (see Section 7.4.1.1, “IC Channels”). This will prevent the captured value being overwritten until it is read or latched in the holding register.

"MSCAN Control Register 0 (CANCTL0)"). In case of a transmission, the CPU can only read the time stamp after the respective transmit buffer has been flagged empty.

The timer value, which is used for stamping, is taken from a free running internal CAN bit clock. A timer overrun is not indicated by the MSCAN. The timer is reset (all bits set to 0) during initialization mode. The CPU can only read the time stamp registers.

	7	6	5	4	3	2	1	0
R	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
W								
Reset:	x	x	x	x	x	x	x	x

Figure 10-37. Time Stamp Register — High Byte (TSRH)

	7	6	5	4	3	2	1	0
R	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
W								
Reset:	x	x	x	x	x	x	x	x

Figure 10-38. Time Stamp Register — Low Byte (TSRL)

Read: Anytime when TXEx flag is set (see Section 10.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 10.3.2.11, "MSCAN Transmit Buffer Selection Register (CANTBSEL)").

Write: Unimplemented

10.4 Functional Description

10.4.1 General

This section provides a complete functional description of the MSCAN. It describes each of the features and modes listed in the introduction.

Table 10-34. Time Segment Syntax

Syntax	Description
SYNC_SEG	System expects transitions to occur on the CAN bus during this period.
Transmit Point	A node in transmit mode transfers a new value to the CAN bus at this point.
Sample Point	A node in receive mode samples the CAN bus at this point. If the three samples per bit option is selected, then this point marks the position of the third sample.

The synchronization jump width (see the Bosch CAN specification for details) can be programmed in a range of 1 to 4 time quanta by setting the SJW parameter.

The SYNC_SEG, TSEG1, TSEG2, and SJW parameters are set by programming the MSCAN bus timing registers (CANBTR0, CANBTR1) (see Section 10.3.2.3, "MSCAN Bus Timing Register 0 (CANBTR0)" and Section 10.3.2.4, "MSCAN Bus Timing Register 1 (CANBTR1)").

Table 10-35 gives an overview of the CAN compliant segment settings and the related parameter values.

NOTE

It is the user's responsibility to ensure the bit time settings are in compliance with the CAN standard.

Table 10-35. CAN Standard Compliant Bit Time Segment Settings

Time Segment 1	TSEG1	Time Segment 2	TSEG2	Synchronization Jump Width	SJW
5 .. 10	4 .. 9	2	1	1 .. 2	0 .. 1
4 .. 11	3 .. 10	3	2	1 .. 3	0 .. 2
5 .. 12	4 .. 11	4	3	1 .. 4	0 .. 3
6 .. 13	5 .. 12	5	4	1 .. 4	0 .. 3
7 .. 14	6 .. 13	6	5	1 .. 4	0 .. 3
8 .. 15	7 .. 14	7	6	1 .. 4	0 .. 3
9 .. 16	8 .. 15	8	7	1 .. 4	0 .. 3

10.4.4 Modes of Operation

10.4.4.1 Normal Modes

The MSCAN module behaves as described within this specification in all normal system operation modes.

10.4.4.2 Special Modes

The MSCAN module behaves as described within this specification in all special system operation modes.

20.3.2.2 Debug Status Register (DBGSR)

Address: 0x0021

	7	6	5	4	3	2	1	0
R	TBF	EXTF	0	0	0	SSF2	SSF1	SSF0
W								
Reset	—	0	0	0	0	0	0	0
POR	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 20-4. Debug Status Register (DBGSR)

Read: Anytime

Write: Never

Table 20-6. DBGSR Field Descriptions

Field	Description
7 TBF	**Trace Buffer Full** — The TBF bit indicates that the trace buffer has stored 64 or more lines of data since it was last armed. If this bit is set, then all 64 lines will be valid data, regardless of the value of DBGCNT bits CNT[6:0]. The TBF bit is cleared when ARM in DBGC1 is written to a one. The TBF is cleared by the power on reset initialization. Other system generated resets have no affect on this bit
6 EXTF	**External Tag Hit Flag** — The EXTF bit indicates if a tag hit condition from an external $\overline{\text{TAGHI}}$/$\overline{\text{TAGLO}}$ tag was met since arming. This bit is cleared when ARM in DBGC1 is written to a one. 0 External tag hit has not occurred 1 External tag hit has occurred
2–0 SSF[2:0]	**State Sequencer Flag Bits** — The SSF bits indicate in which state the State Sequencer is currently in. During a debug session on each transition to a new state these bits are updated. If the debug session is ended by software clearing the ARM bit, then these bits retain their value to reflect the last state of the state sequencer before disarming. If a debug session is ended by an internal trigger, then the state sequencer returns to state0 and these bits are cleared to indicate that state0 was entered during the session. On arming the module the state sequencer enters state1 and these bits are forced to SSF[2:0] = 001. See Table 20-7**.**

Table 20-7. SSF[2:0] — State Sequence Flag Bit Encoding

SSF[2:0]	Current State
000	State0 (disarmed)
001	State1
010	State2
011	State3
100	Final State
101,110,111	Reserved

21.1.3 Block Diagram

Figure 21-1 is a block diagram of the XEBI with all related I/O signals.

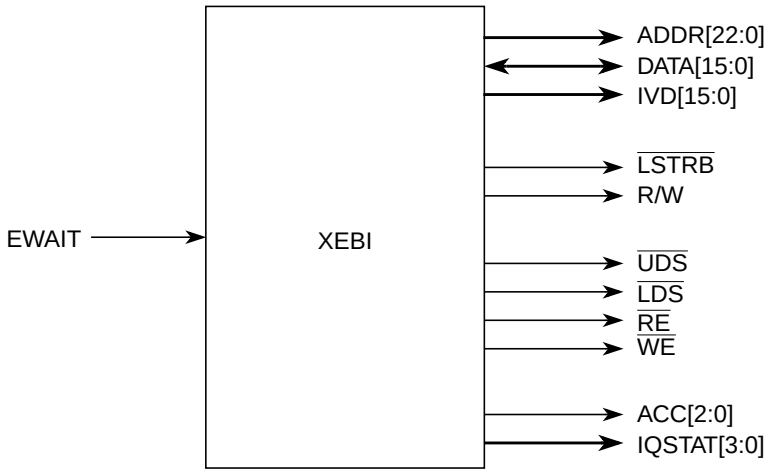

Figure 21-1. XEBI Block Diagram

21.2 External Signal Description

The user is advised to refer to the SoC section for port configuration and location of external bus signals.

NOTE

The following external bus related signals are described in other sections:
$\overline{CS2}$, $\overline{CS1}$, $\overline{CS0}$ (chip selects) — S12X_MMC section
ECLK, ECLKX2 (free-running clocks) — PIM section
$\overline{TAGHI}$, $\overline{TAGLO}$ (tag inputs) — PIM section, S12X_DBG section

Table 21-1 outlines the pin names and gives a brief description of their function. Refer to the SoC section and PIM section for reset states of these pins and associated pull-ups or pull-downs.

22.3 Memory Map and Register Definition

This section provides a detailed description of all PIM registers.

22.3.1 Module Memory Map

Table 22-2 shows the register map of the port integration module.

Table 22-2. PIM Memory Map (Sheet 1 of 3)

Address	Use	Access
0x0000	Port A Data Register (PORTA)	Read / Write
0x0001	Port B Data Register (PORTB)	Read / Write
0x0002	Port A Data Direction Register (DDRA)	Read / Write
0x0003	Port B Data Direction Register (DDRB)	Read / Write
0x0004	Port C Data Register (PORTC)	Read / Write
0x0005	Port D Data Register (PORTD)	Read / Write
0x0006	Port C Data Direction Register (DDRC)	Read / Write
0x0007	Port D Data Direction Register (DDRD)	Read / Write
0x0008	Port E Data Register (PORTE)	Read / Write[1]
0x0009	Port E Data Direction Register (DDRE)	Read / Write[1]
0x000A : 0x000B	Non-PIM Address Range	—
0x000C	Pull-up Up Control Register (PUCR)	Read / Write[1]
0x000D	Reduced Drive Register (RDRIV)	Read / Write[1]
0x000E : 0x001B	Non-PIM Address Range	—
0x001C	ECLK Control Register (ECLKCTL)	Read / Write[1]
0x001D	PIM Reserved	—
0x001E	IRQ Control Register (IRQCR)	Read / Write[1]
0x001F	PIM Reserved	—
0x0020 : 0x0031	Non-PIM Address Range	—
0x0032	Port K Data Register (PORTK)	Read / Write
0x0033	Port K Data Direction Register (DDRK)	Read / Write
0x0034 : 0x023F	Non-PIM Address Range	—
0x0240	Port T Data Register (PTT)	Read / Write

22.3.2.53 Port H Interrupt Flag Register (PIFH)

	7	6	5	4	3	2	1	0
R W	PIFH7	PIFH6	PIFH5	PIFH4	PIFH3	PIFH2	PIFH1	PIFH0
Reset	0	0	0	0	0	0	0	0

Figure 22-55. Port H Interrupt Flag Register (PIFH)

Read: Anytime.

Write: Anytime.

Each flag is set by an active edge on the associated input pin. This could be a rising or a falling edge based on the state of the PPSH register. To clear this flag, write logic level “1” to the corresponding bit in the PIFH register. Writing a “0” has no effect.

Table 22-50. PIFH Field Descriptions

Field	Description
7–0 PIFH[7:0]	**Interrupt Flags Port H** 0 No active edge pending. Writing a “0” has no effect. 1 Active edge on the associated bit has occurred (an interrupt will occur if the associated enable bit is set). Writing a logic level “1” clears the associated flag.

23.0.5.35 Port M Polarity Select Register (PPSM)

	7	6	5	4	3	2	1	0
R W	PPSM7	PPSM6	PPSM5	PPSM4	PPSM3	PPSM2	PPSM1	PPSM0
Reset	0	0	0	0	0	0	0	0

Figure 23-37. Port M Polarity Select Register (PPSM)

Read: Anytime.

Write: Anytime.

This register selects whether a pull-down or a pull-up device is connected to the pin. If CAN is active, a pull-up device can be activated on the related RXCAN inputs, but not a pull-down.

Table 23-36. PPSM Field Descriptions

Field	Description
7–0 PPSM[7:0]	**Pull Select Port M** 0 A pull-up device is connected to the associated port M pin, if enabled by the associated bit in register PERM and if the port is used as general purpose or RXCAN input. 1 A pull-down device is connected to the associated port M pin, if enabled by the associated bit in register PERM and if the port is used as a general purpose but not as RXCAN.

23.0.5.36 Port M Wired-OR Mode Register (WOMM)

	7	6	5	4	3	2	1	0
R W	WOMM7	WOMM6	WOMM5	WOMM4	WOMM3	WOMM2	WOMM1	WOMM0
Reset	0	0	0	0	0	0	0	0

Figure 23-38. Port M Wired-OR Mode Register (WOMM)

Read: Anytime.

Write: Anytime.

This register configures the output pins as wired-OR. If enabled the output is driven active low only (open-drain). A logic level of “1” is not driven. It applies also to the CAN outputs and allows a multipoint connection of several serial modules. This bit has no influence on pins used as inputs.

Table 23-37. WOMM Field Descriptions

Field	Description
7–0 WOMM[7:0]	**Wired-OR Mode Port M** 0 Output buffers operate as push-pull outputs. 1 Output buffers operate as open-drain outputs.

26.4.2.1 Erase Verify Command

The erase verify operation will verify that the EEPROM memory is erased.

An example flow to execute the erase verify operation is shown in Figure 26-18. The erase verify command write sequence is as follows:

1. Write to an EEPROM address to start the command write sequence for the erase verify command. The address and data written will be ignored.
2. Write the erase verify command, 0x05, to the ECMD register.
3. Clear the CBEIF flag in the ESTAT register by writing a 1 to CBEIF to launch the erase verify command.

After launching the erase verify command, the CCIF flag in the ESTAT register will set after the operation has completed unless a new command write sequence has been buffered. The number of bus cycles required to execute the erase verify operation is equal to the number of words in the EEPROM memory plus 14 bus cycles as measured from the time the CBEIF flag is cleared until the CCIF flag is set. Upon completion of the erase verify operation, the BLANK flag in the ESTAT register will be set if all addresses in the EEPROM memory are verified to be erased. If any address in the EEPROM memory is not erased, the erase verify operation will terminate and the BLANK flag in the ESTAT register will remain clear.

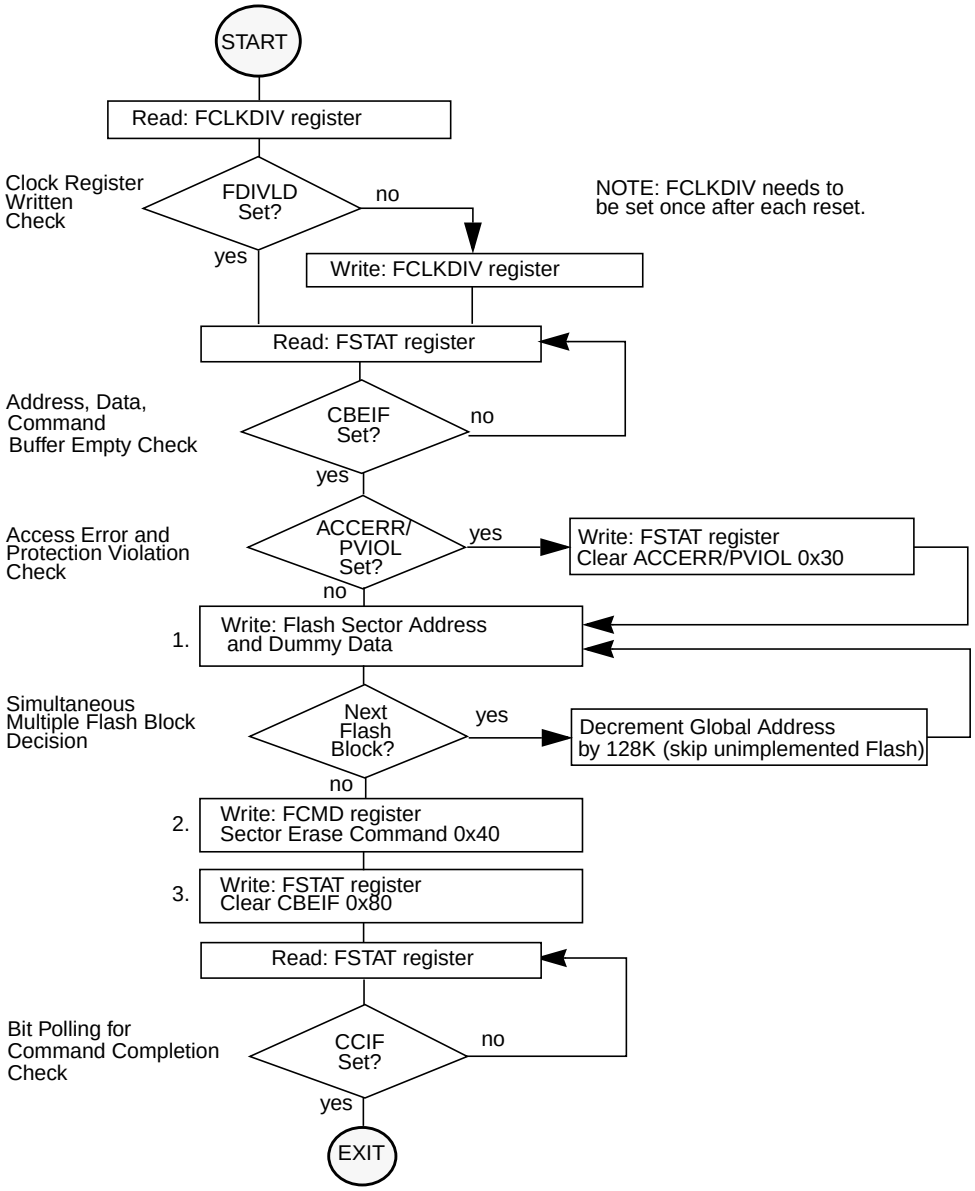

Figure 28-29. Example Sector Erase Command Flow

- Security feature to prevent unauthorized access to the Flash memory
- Code integrity check using built-in data compression

29.1.3 Modes of Operation

Program, erase, erase verify, and data compress operations (please refer to Section 29.4.1, “Flash Command Operations” for details).

29.1.4 Block Diagram

A block diagram of the Flash module is shown in Figure 29-1.

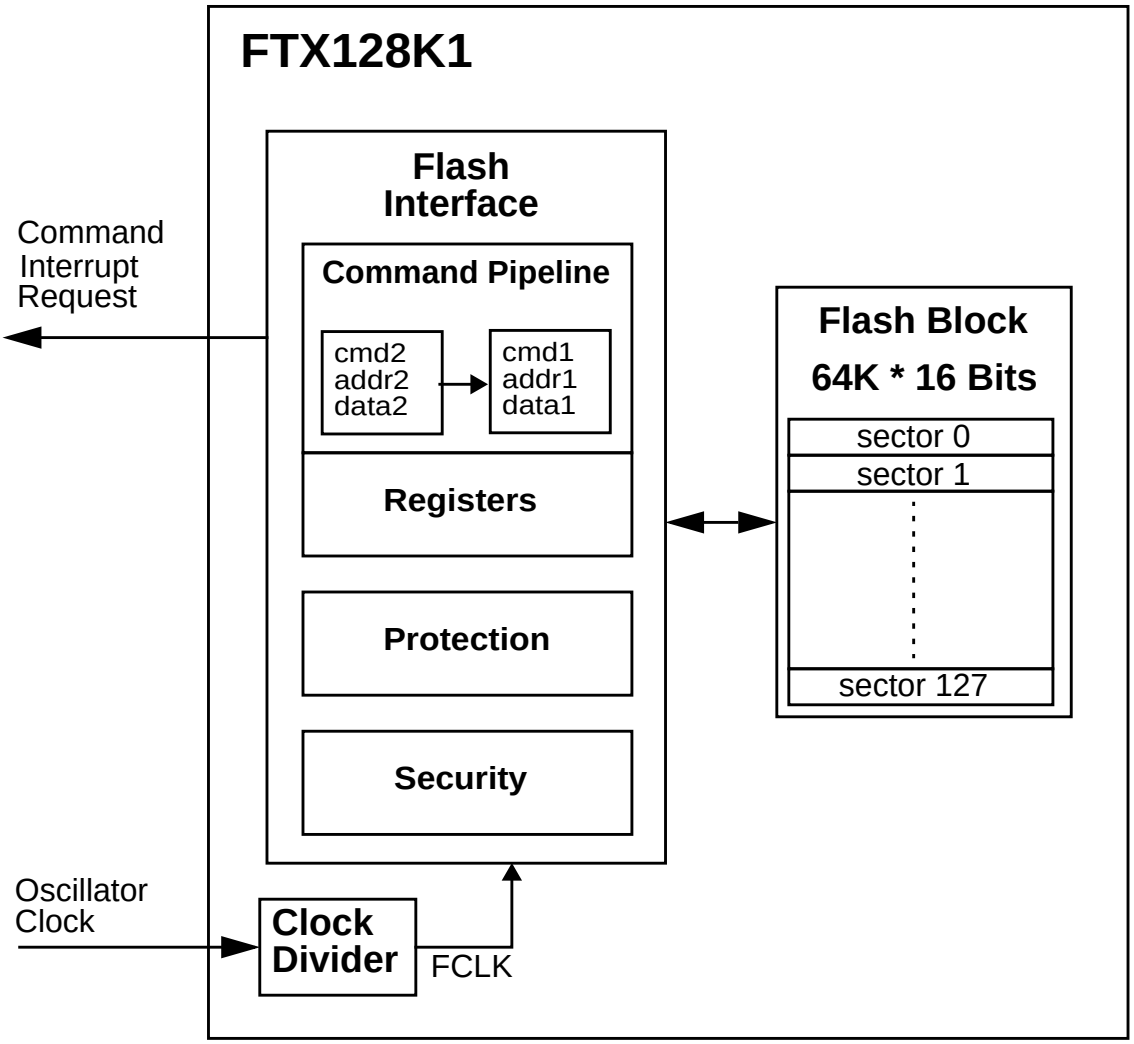

Figure 29-1. FTX128K1 Block Diagram

29.2 External Signal Description

The Flash module contains no signals that connect off-chip.

Table A-20. MC9S12XDP512 - Capacitive Loads

Num	Characteristic	Symbol	Min	Recommended	Max	Unit
1	VDD external capacitive load	C_{DDext}	400	440	12000	nF
2	VDDPLL external capacitive load	$C_{DDPLLext}$	90	220	5000	nF

0x0080–0x00AF Analog-to-Digital Converter 10-bit 16-Channels (ATD1) Map (Sheet 1 of 3)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0080	ATD1CTL0	R	0	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
		W								
0x0081	ATD1CTL1	R	ETRIG SEL	0	0	0	ETRIG CH3	ETRIG CH2	ETRIG CH1	ETRIG CH0
		W								
0x0082	ATD1CTL2	R	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIGE	ASCIE	ASCIF
		W								
0x0083	ATD1CTL3	R	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
		W								
0x0084	ATD1CTL4	R	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
		W								
0x0085	ATD1CTL5	R	DJM	DSGN	SCAN	MULT	CD	CC	CB	CA
		W								
0x0086	ATD1STAT0	R	SCF	0	ETORF	FIFOR	CC3	CC2	CC1	CC0
		W								
0x0087	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0088	ATD1TEST0	R	U	U	U	U	U	U	U	U
		W	Reserved For Factory Test							
0x0089	ATD1TEST1	R	U	U	U	U	U	U	U	SC
		W								
0x008A	ATD1STAT2	R	CCF15	CCF14	CCF13	CCF12	CCF11	CCF10	CCF9	CCF8
		W								
0x008B	ATD1STAT1	R	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
		W								
0x008C	ATD1DIEN0	R	IEN15	IEN14	IEN13	IEN12	IEN11	IEN10	IEN9	IEN8
		W								
0x008D	ATD1DIEN	R	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
		W								
0x008E	ATD1PTAD0	R	PTAD15	PTAD14	PTAD13	PTAD12	PTAD11	PTAD10	PTAD9	PTAD8
		W								
0x008F	ATD1PTAD1	R	PTAD7	PTAD6	PTAD5	PTAD4	PTAD3	PTAD2	PTAD1	PTAD0
		W								
0x0090	ATD1DR0H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x0091	ATD1DR0L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x0092	ATD1DR1H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x0093	ATD1DR1L	R	Bit7	Bit6	0	0	0	0	0	0
		W								
0x0094	ATD1DR2H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x0095	ATD1DR2L	R	Bit7	Bit6	0	0	0	0	0	0
		W								