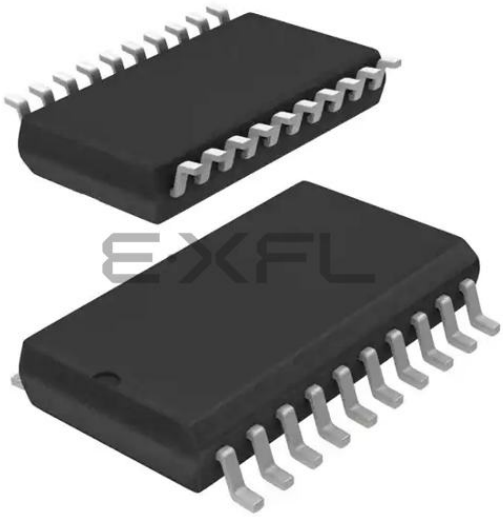

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SIO
Peripherals	POR, Temp Sensor, WDT
Number of I/O	14
Program Memory Size	6KB (6K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	224 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc705jj7cdw

Addr.	Register		Bit 7	6	5	4	3	2	1	Bit 0
$0018	Programmable Timer Register High (TMRH) See page 107.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$0019	Programmable Timer Register Low (TMRL) See page 107.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	1	1	1	1	1	1	0	0
$001A	Alternate Counter Register High (ACRH) See page 108.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$001B	Alternate Counter Register Low (ACRL) See page 108.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	1	1	1	1	1	1	0	0
$001C	EPROM Programming Register (EPROG) See page 119.	Read:	0	0	0	0	0	ELAT	MPGM	EPGM
		Write:		R	R	R	R			
		Reset:	0	0	0	0	0	0	0	0
$001D	Analog Counter Register (ACR) See page 77.	Read:	CHG	ATD2	ATD1	ICEN	CPIE	CP2EN	CP1EN	ISEN
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$001E	Analog Status Register (ASR) See page 77.	Read:	CPF2	CPF1	0	0	COE1	VOFF	CMP2	CMP1
		Write:			CPFR2	CPFR1				R
		Reset:	0	0	0	0	0	0	0	0
$001F	Reserved		R	R	R	R	R	R	R	R
↓										
$1FEF	Reserved		R	R	R	R	R	R	R	R
$1FF0	COP and Security Register (COPR) See pages 27, 92, 104, and 122.	Read:		OPT						
		Write:	EPMSEC							COPC
		Reset:	Unaffected by reset							

= Unimplemented R = Reserved U = Unaffected

1. Features related to port C are only available on the 28-pin MC68HC705JP7 devices.

Figure 2-3. Register Summary (Sheet 3 of 3)

4.4 Software Interrupt

The software interrupt (SWI) instruction causes a non-maskable interrupt.

4.5 External Interrupts

These sources can generate external interrupts:

- $\overline{IRQ}/V_{PP}$ pin
- PA3–PA0 pins

Setting the I bit in the condition code register or clearing the IRQE bit in the interrupt status and control register disables these external interrupts.

4.5.1 $\overline{IRQ}/V_{PP}$ Pin

An interrupt signal on the $\overline{IRQ}/V_{PP}$ pin latches an external interrupt request. To help clean up slow edges, the input from the $\overline{IRQ}/V_{PP}$ pin is processed by a Schmitt trigger gate. When the CPU completes its current instruction, it tests the IRQ latch. If the IRQ latch is set, the CPU then tests the I bit in the condition code register and the IRQE bit in the IRQ status and control register (ISCR). If the I bit is clear and the IRQE bit is set, then the CPU begins the interrupt sequence. The CPU clears the IRQ latch while it fetches the interrupt vector, so that another external interrupt request can be latched during the interrupt service routine. As soon as the I bit is cleared during the return from interrupt, the CPU can recognize the new interrupt request. Figure 4-3 shows the logic for external interrupts.

NOTE

If the $\overline{IRQ}/V_{PP}$ pin is not in use, it should be connected to the V_{DD} pin.

The $\overline{IRQ}/V_{PP}$ pin can be negative edge-triggered only or negative edge- and low level-triggered. External interrupt sensitivity is programmed with the LEVEL bit in the mask option register (MOR).

With the edge- and level-sensitive trigger MOR option, a falling edge or a low level on the $\overline{IRQ}/V_{PP}$ pin latches an external interrupt request. The edge- and level-sensitive trigger MOR option allows connection to the $\overline{IRQ}/V_{PP}$ pin of multiple wired-OR interrupt sources. As long as any source is holding the IRQ low, an external interrupt request is present, and the CPU continues to execute the interrupt service routine.

With the edge-sensitive-only trigger option, a falling edge on the $\overline{IRQ}/V_{PP}$ pin latches an external interrupt request. A subsequent interrupt request can be latched only after the voltage level on the $\overline{IRQ}/V_{PP}$ pin returns to a logic 1 and then falls again to logic 0.

NOTE

The response of the $\overline{IRQ}/V_{PP}$ pin can be affected if the external interrupt capability of the PA0 through PA3 pins is enabled. If the port A pins are enabled as external interrupts, then any high level on a PA0–PA3 pin will cause the IRQ changes and state to be ignored until all of the PA0–PA3 pins have returned to a low level.

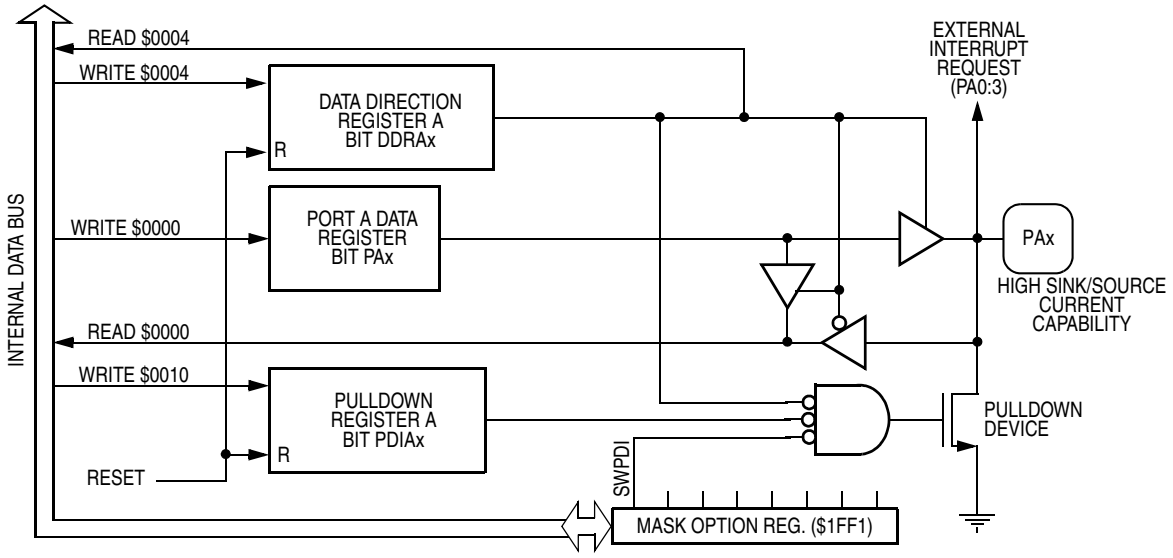


Figure 7-4. Port A I/O Circuit

7.3 Port B

Port B is an 8-bit, general-purpose, bidirectional I/O port with these features:

- Programmable pulldown devices
- PB0–PB4 are shared with the analog subsystem.
- PB3 and PB4 are shared with the 16-bit programmable timer.
- PB4 can be driven directly by the output of comparator 1.
- PB5–PB7 are shared with the simple serial interface (SIOP).
- High current sinking capability on the PB4 pin
- High current sourcing capability on the PB4 pin

7.3.1 Port B Data Register

The port B data register (PORTB) contains a bit for each of the port B pins. When a port B pin is programmed to be an output, the state of its data register bit determines the state of the output pin. When a port B pin is programmed to be an input, reading the port B data register returns the logic state of the pin. Reset has no effect on port B data.

Address:	$0001							
	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Reset:	Unaffected by reset							
Alternate:	SCK	SDI	SDO	AN4	AN3	AN2	AN1	AN0
Alternate:	SCK	SDI	SDO	TCMP	TCAP	AN2	AN1	AN0
Alternate:	SCK	SDI	SDO	CMP1	TCAP	AN2	AN1	AN0

Figure 7-5. Port B Data Register (PORTB)

7.3.9 PB7/SCK Logic

The PB7/SCK pin can be used as a simple I/O port pin or be controlled by the SIOP serial interface as shown in Figure 7-12. The operations of the PB7/SCK pin are summarized in Table 7-3.

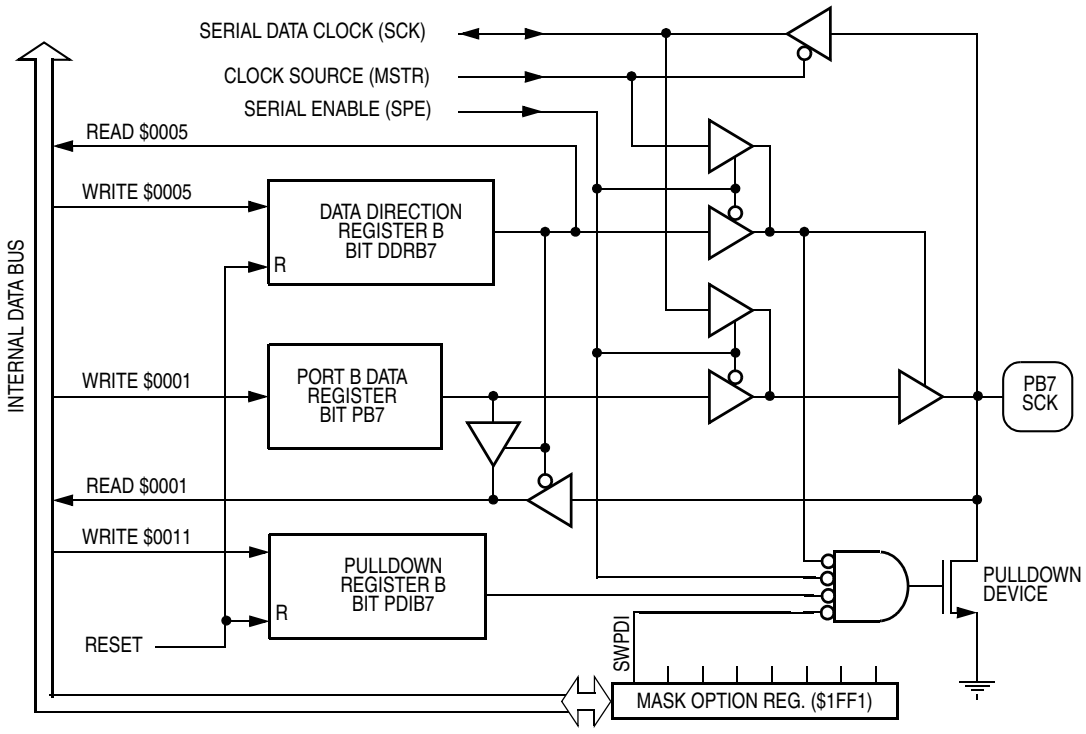


Figure 7-12. PB7/SCK Pin I/O Circuit

When using the PB7/SCK pin, these interactions must be noted:

1. If the SIOP function is required, then the SPE bit in the SCR must be set. This causes the PB7/SCK pin buffer to be controlled by the MSTR control bit in the SCR. The pulldown device is disabled in these cases.
   a. If the MSTR bit is set, then the PB7/SCK pin buffer will be enabled and driven by the serial data clock (SCK) from the SIOP.
   b. If the MSTR bit is clear, then the PB7/SCK pin buffer will be disabled, allowing the PB7/SCK pin to drive the serial data clock (SCK) into the SIOP.
2. If the SIOP function is in control of the PB7/SCK pin, the DDRB7 and PB7 data register bits are still accessible to the CPU and can be altered or read without affecting the SIOP functionality. However, if the DDRB7 bit is cleared, reading the PB7 data register will return the current state of the PB7/SCK pin.
3. If the SIOP function is terminated by clearing the SPE bit in the SCR, then the last conditions stored in the DDRB7, PDIB7, and PB7 register bits will then control the PB7/SCK pin.
4. If the PB7/SCK pin is to be a digital input, then both the SPE bit in the SCR and the DDRB7 bit must be cleared. Depending on the external application, the pulldown device may also be disabled by setting the PDIB7 pulldown inhibit bit.

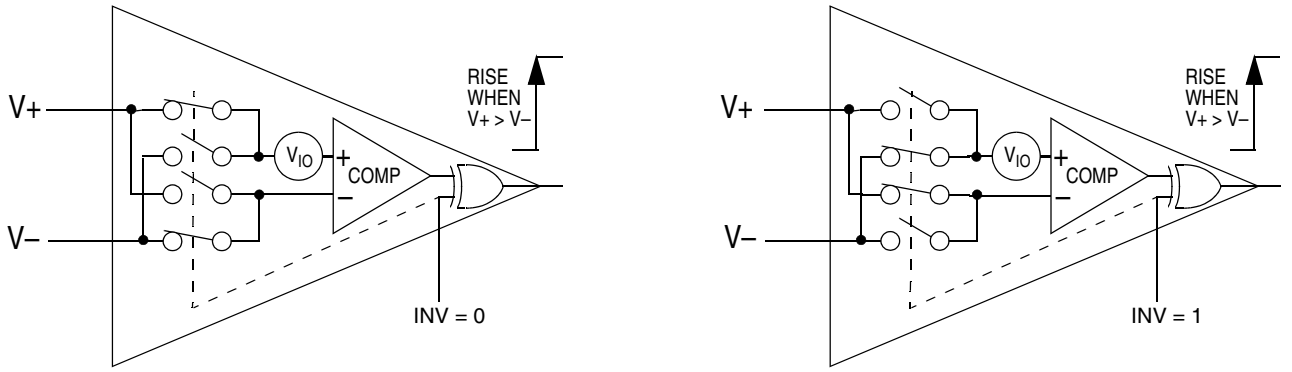


Figure 8-4. INV Bit Action

NOTE

Either comparator may generate an output flag when the inputs are exchanged due to a change in the state of the INV bit. It is therefore recommended that the INV bit not be changed while waiting for a comparator flag. Further, any changes to the state of the INV bit should be followed by writing a logic 1 to both the CPFR1 and CPFR2 bits to clear any extraneous CPF1 or CPF2 flags that may have occurred.

VREF

This read/write bit connects the channel select bus to V_{DD} for making a reference voltage measurement. It cannot be selected if any of the other input sources to the channel select bus are selected as shown in Table 8-2. This bit is cleared by a reset of the device.

1 = Channel select bus connected to V_{DD} if all MUX1:4 are cleared.

0 = Channel select bus cannot be connected to V_{DD}.

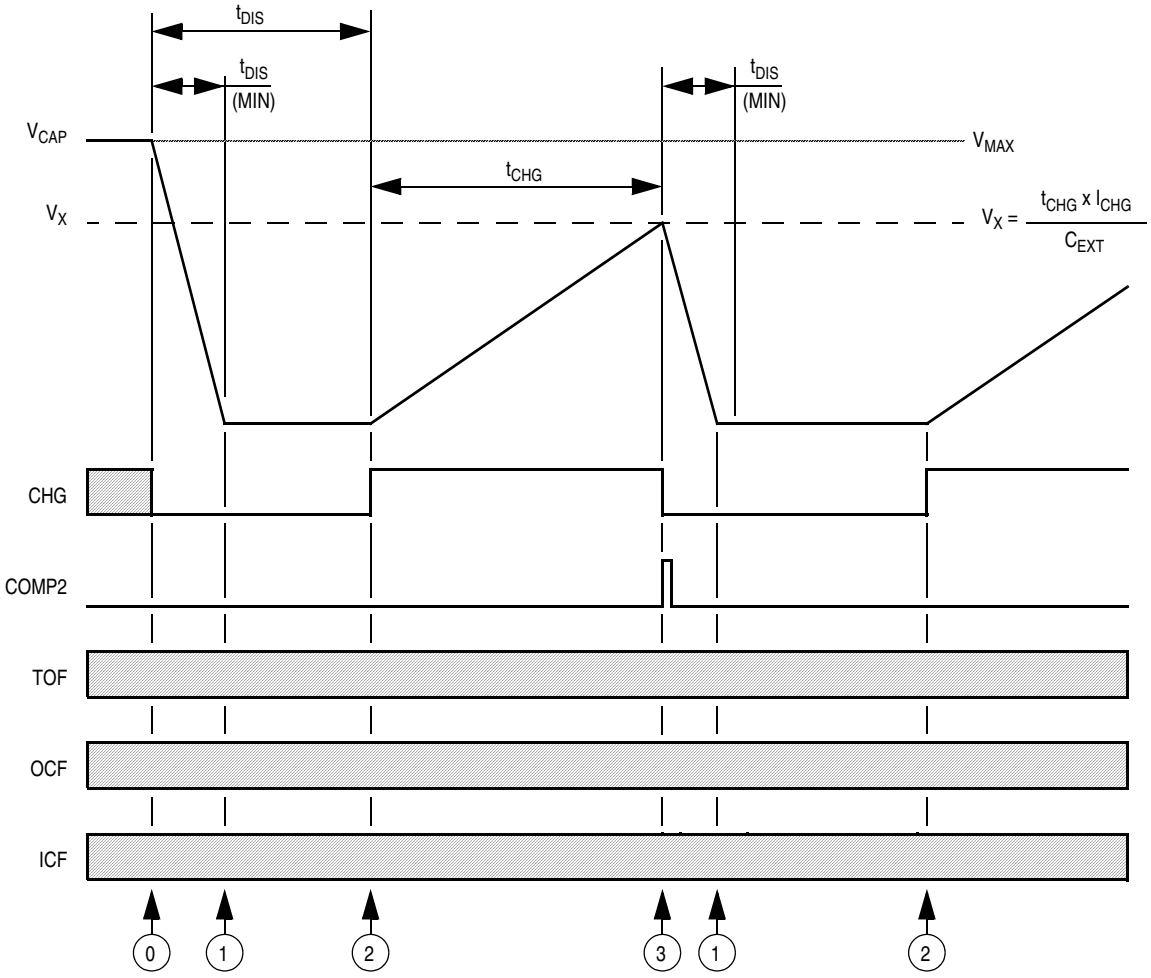
MUX1:4

These are read/write bits that connect the analog subsystem pins to the channel select bus and voltage comparator 2 for purposes of making a voltage measurement. They can be selected individually or combined with any of the other input sources to the channel select bus as shown in Table 8-2.

NOTE

The V_{AOFF} voltage source shown in Figure 8-1 depicts a small offset voltage generated by the total chip current passing through the package bond wires and lead frame that are attached to the single V_{SS} pin. This offset raises the internal V_{SS} reference (AV_{SS}) in the analog subsystem with respect to the external V_{SS} pin. Turning on the V_{SS} MUX to the channel select bus connects it to this internal AV_{SS} reference line.

When making A/D conversions, this AV_{SS} offset gets placed on the external ramping capacitor since the discharge device on the PB0/AN0 pin discharges the external capacitor to the internal AV_{SS} line. Under these circumstances, the positive input (+) to comparator 2 will always be higher than the negative input (–) until the negative input reaches the AV_{SS} offset voltage plus any offset in comparator 2.



Point	Action	Software/Hardware Action	Dependent Variable(s)
0	Begin initial discharge and select mode 1 by clearing CHG and ATD2 and setting ATD1 in the ACR.	Software write	Software
1	V_{CAP} falls to V_{SS}.	Wait out minimum t_{DIS} time.	V_{MAX}, I_{DIS}, C_{EXT}
2	Stop discharge and begin charge by setting CHG control bit in ACR.	Software write	Software
3	V_{CAP} rises to V_X and comparator 2 output trips, setting CPF2 and CMP2, which clears CHG control bit in the ACR. Reset CPF2 by writing a 1 to CPFR2.	Wait out t_{CHG} time. CPF2 clears CHG control bit.	V_X, I_{CHG}, C_{EXT}

Figure 8-9. A/D Conversion — Manual/Auto Discharge Control (Mode 1)

8.6.2 Ratiometric Voltage Readings

The ratiometric value of a voltage measurement can be calculated in software by first taking a reference reading from a reference source and then comparing subsequent unknown voltages to that reading as a percentage of the reference value. The accuracy of ratiometric readings will depend on the variety of sources, but will generally be better than for absolute readings. Many of these error sources can be taken into account using the features of the analog subsystem and appropriate software as described in Table 8-7. As with absolute measurements, most of the errors can be reduced by frequent comparisons to the reference voltage, use of the inverted comparator inputs, and averaging of multiple samples.

Table 8-7. Ratiometric Voltage Reading Errors

Error Source	Accuracy Improvements Possible	
	In Hardware	In Software
Change in reference voltage	Not required for ratiometric	Compare unknown with recent measurement from reference
Change in magnitude of ramp current source	Not adjustable	Compare unknown with recent measurement from reference
Non-linearity of ramp current source vs. voltage	Not adjustable	Calibration and storage of voltages at 1/4, 1/2, 3/4, and FS
Frequency shift in internal low-power oscillator	Not required for ratiometric	Compare unknown with recent measurement from reference
Sampling capacitor leakage	Use faster conversion times	Compare unknown with recent measurement from reference
Internal voltage divider ratio	Not adjustable	Compare unknown with recent measurement from reference
Input offset voltage of comparator 2	Not adjustable	Sum two readings on reference or unknown using INV and $\overline{INV}$ control bit and divide by 2 (average of both)
Noise internal to MCU	Close decoupling at V_{DD} and V_{SS} pins and reduce supply source impedance	Average multiple readings on both the reference and the unknown voltage

8.6.2.1 Internal Ratiometric Reference

If readings are to be ratiometric to V_{DD}, the reference measurement point can be internally selected. In this case the reference reading can be taken by setting the V_{REF} bit and clearing the MUX1:4 bits in the AMUX register which connects the channel selection bus to the V_{DD} pin. In order to stay within the V_{MAX} range, the DHOLD bit should be used to select the 1/2 divided input.

8.6.2.2 External Ratiometric Reference

If readings are to be ratiometric to some external source, the reference measurement point can be connected to any one of the channel selected pins from PB1–PB4. In this case, the reference reading can be taken by setting the MUX bit in the AMUX which connects channel selection bus to the pin connected to the external reference source. If the external reference is greater than V_{DD} –1.5 volts, then the DHOLD bit should be used to select the 1/2 divided input.

8.7.2 Voltage Comparator 2

Voltage comparator 2 can be used as a simple comparator if its charge current source and discharge device are disabled by clearing the ISEN bit in the ACR. If the ISEN bit is set, the internal ramp discharge device connected to PB0/AN0 may become active and try to pull down any voltage source that may be connected to that pin. Also, since voltage comparator 2 is always connected to two of the port B I/O pins, these pins should be configured as inputs and have their software programmable pulldowns disabled.

8.8 Current Source Features

The internal current source connected to the PB0/AN0 pin supplies about 100 µA of current when the discharge device is disabled and the current source is active. Therefore, this current source can be used in an application if the ISEN enable bit is set to power up the current source and by setting the A/D conversion method to manual mode 0 (ATD1 and ATD2 cleared) and the charge current enabled (CHG set).

8.9 Internal Temperature Sensing Diode Features

An internal diode is forward biased to V_{SS} and will have its voltage change, V_D, for each degree centigrade rise in the temperature of the device. This temperature sensing diode is powered up from a current source only during the time that the diode is selected. When on, this current source typically adds about 30 µA to the I_{DD} current.

The temperature sensing diode can be selected by setting both the HOLD and DHOLD bits in the AMUX register (see 8.2 Analog Multiplex Register).

8.10 Sample and Hold

When using the internal sample capacitor to capture a voltage for later conversion, the HOLD or DHOLD bit must be cleared first before changing any channel selection. If both the HOLD (or DHOLD) bit and the channel selection are changed on the same write cycle, the sample may be corrupted during the switching transitions.

NOTE

The sample capacitor can be affected by excessive noise created with respect to the device's V_{SS} pin such that it may appear to leak down or charge up depending on the voltage level stored on the sample capacitor. It is recommended to avoid switching large currents through the port pins while a voltage is to remain stored on the sample capacitor.

The additional option of adding an offset voltage to the bottom of the sample capacitor allows unknown voltages near V_{SS} to be sampled and then shifted up past the comparator offset and the device offset caused by a single V_{SS} return pin. This offset also provides a means to measure the internal V_{SS} level regardless of the comparator offset to determine N_{OFF} as described in 8.6 Voltage Measurement Methods. In either case the OPT bit must be set in the COPR located at $1FF0 as in Figure 8-12 and the VOFF bit must be set in the ASR. It is not necessary to switch the VOFF bit during conversions, since the offset is controlled by the HOLD and DHOLD bits when the VOFF is active. Refer to 8.2 Analog Multiplex Register for more details on the design and decoding of the sample and hold circuit.

The SIOP subsystem shares its input/output pins with port B. When the SIOP is enabled (SPE bit set in the SCR), the port B data direction and data registers are bypassed by the SIOP. The port B data direction and data registers will remain accessible and can be altered by the application software, but these actions will not affect the SIOP transmitted or received data.

9.2 SIOP Signal Format

The SIOP subsystem can be software configured for master or slave operation. No external mode selection inputs are available (for instance, no slave select pin).

9.2.1 Serial Clock (SCK)

The state of the SCK output remains a fixed logic level during idle periods between data transfers. The edges of SCK indicate the beginning of each output data transfer and latch any incoming data received. The first bit of transmitted data is output from the SDO pin on the first falling edge of SCK. The first bit of received data is accepted at the SDI pin on the first rising edge of SCK after the first falling edge. The transfer is terminated upon the eighth rising edge of SCK.

The idle state of the SCK is determined by the state of the CPHA bit in the SCR. When the CPHA is clear, SCK will remain idle at a logic 1 as shown in Figure 9-2. When the CPHA is set, SCK will remain idle at a logic 0 as shown in Figure 9-3. In both cases, the SDO changes data on the falling edge of the SCK, and the SDI latches data in on the rising edge of SCK.

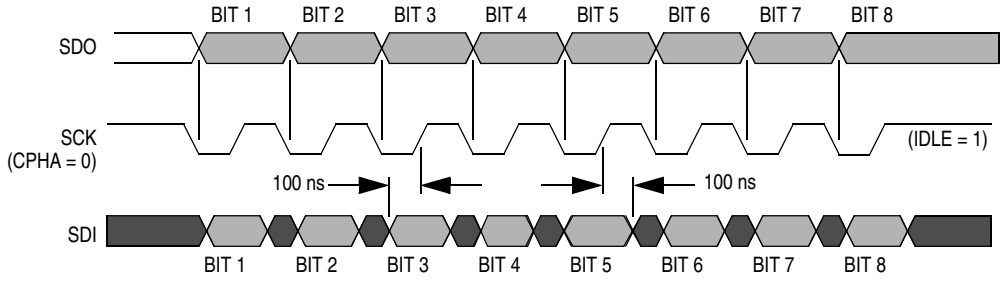


Figure 9-2. SIOP Timing Diagram (CPHA = 0)

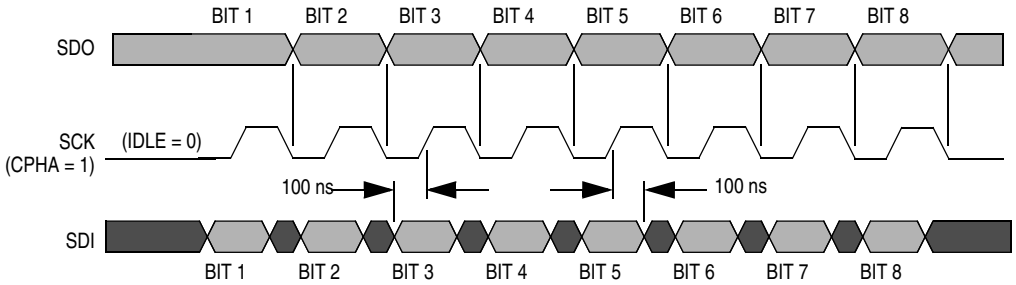


Figure 9-3. SIOP Timing Diagram (CPHA = 1)

The only difference in the master and slave modes of operation is the sourcing of the SCK. In master mode, SCK is driven from an internal source within the MCU. In slave mode, SCK is driven from a source external to the MCU. The SCK frequency is based on one of four divisions of the oscillator clock that is selected by the SPR0 and SPR1 bits in the SCR.

TOF — Timer Overflow Flag

The TOF bit is automatically set when the 16-bit timer counter rolls over from $FFFF to $0000. Clear the TOF bit by reading the timer status register with the TOF set and then accessing the low byte (TMRL, $0019) of the timer registers. Resets have no effect on TOF.

11.8 Timer Operation during Wait Mode

During wait mode, the 16-bit timer continues to operate normally and may generate an interrupt to trigger the MCU out of wait mode.

11.9 Timer Operation during Stop Mode

When the MCU enters stop mode, the free-running counter stops counting (the internal processor clock is stopped). It remains at that particular count value until stop mode is exited by applying a low signal to the $\overline{IRQ}/V_{PP}$ pin, at which time the counter resumes from its stopped value as if nothing had happened. If stop mode is exited via an external reset (logic low applied to the $\overline{RESET}$ pin), the counter is forced to $FFFC.

If a valid input capture edge occurs during stop mode, the input capture detect circuitry will be armed. This action does not set any flags or wake up the MCU, but when the MCU does wake up there will be an active input capture flag (and data) from the first valid edge. If the stop mode is exited by an external reset, no input capture flag or data will be present even if a valid input capture edge was detected during stop mode.

11.10 Timer Operation during Halt Mode

When the MCU enters halt mode, the functions and states of the 16-bit programmable timer are the same as for wait mode described in 11.8 Timer Operation during Wait Mode.

PEPGM — PEPROM Program Control Bit

This read/write bit controls the switches that apply the programming voltage from the $\overline{IRQ}/V_{PP}$ pin to the selected PEPROM bit cell. When the PEPGM bit is set, the selected bit cell will be programmed to a logic 1, regardless of the state of the PEDATA bit. Reset clears the PEPGM bit.

1 = Programming voltage applied to array bit
0 = Programming voltage not applied to array bit

PEPRZF — PEPROM Row Zero Flag

This read-only bit is set when the PEPROM bit select register selects the first row (row zero) of the PEPROM array. Selecting any other row clears PEPRZF. Monitoring PEPRZF can reduce the code needed to access one byte of eight PEPROM locations. Reset clears the PEPROM bit select register, thereby setting the PEPRZF bit by default.

1 = Row zero selected
0 = Row zero not selected

Table 12-1. PEPROM Bit Selection

PEBSR	PEPROM Bit Selected	
$00	Row 0	Column 0
$01	Row 1	Column 0
|	|	|
V	V	V
$07	Row 7	Column 0
$08	Row 0	Column 1
$09	Row 1	Column 1
|	|	|
V	V	V
$37	Row 7	Column 6
$38	Row 0	Column 7
$39	Row 1	Column 7
|	|	|
V	V	V
$3E	Row 6	Column 7
$3F	Row 7	Column 7

12.3 PEPROM Programming

Factory-provided software for programming the PEPROM is available on the World Wide Web at:
http://www.freescale.com

NOTE

While the PEPGM bit is set and the V_{PP} voltage level is applied to the $\overline{IRQ}/V_{PP}$ pin, do not access bits that are to be left unprogrammed (erased).

To program the PEPROM bits properly, the V_{DD} voltage must be greater than 4.5 Vdc.

The PEPROM can also be programmed by user software with the V_{PP} voltage level applied to the $\overline{IRQ}/V_{PP}$ pin. This sequence shows how to program each PEPROM bit:

1. Select a PEPROM bit by writing to the PEBSR.
2. Set the PEPGM bit in the PESCR.
3. Wait for the programming time, t_{EPGM}.
4. Clear the PEPGM bit.
5. Move to next PEPROM bit to be programmed in step 1.

13.3.1 MOR Programming

The contents of the MOR should be programmed using the programmer board. To program any bits in the MOR, the desired bit states must be written to the MOR address and then the MPGM bit in the EPROG register must be used. The following sequence will program the MOR:

1. Write the desired data to the MOR location ($1FF1).
2. Apply the programming voltage to the $\overline{IRQ}/V_{PP}$ pin.
3. Set the MPGM bit in the EPROG.
4. Wait for the programming time, t_{MPGM}.
5. Clear the MPGM bit in the EPROG.
6. Remove the programming voltage from the $\overline{IRQ}/V_{PP}$ pin.

Once the MOR bits have been programmed, some of the options may experience glitches in operation after removal of the programming voltage. It is recommended that the part be reset before trying to verify the contents of the user EPROM or the MOR itself.

NOTE

The contents of the EPROM or the MOR cannot be accessed if the EPMSEC bit in the COPR register has been set.

13.3.2 EPMSEC Programming

The EPMSEC bit is programmable. To program the EPMSEC bit, the desired state must be written to the COP address and then the MPGM bit in the EPROG register must be used. The following sequence will program the EPMSEC bit:

1. Write the desired data to bit 7 of the COPR location ($1FF0).
2. Apply the programming voltage to the $\overline{IRQ}/V_{PP}$ pin.
3. Set the MPGM bit in the EPROG.
4. Wait for the programming time, t_{MPGM}.
5. Clear the MPGM bit in the EPROG.
6. Remove the programming voltage from the $\overline{IRQ}/V_{PP}$ pin.

Once the EPMSEC bit has been programmed to a logic 1, access to the contents of the EPROM and MOR in the expanded non-user modes will be denied. It is therefore recommended that the user EPROM and MOR in the part first be programmed and fully verified before setting the EPMSEC bit.

13.4 EPROM Erasing

MCUs with windowed packages permit EPROM erasing with ultraviolet light. Erase the EPROM by exposing it to 15 Ws/cm^2 of ultraviolet light with a wavelength of 2537 angstroms. Position the ultraviolet light source 1 inch from the window. Do not use a shortwave filter. The erased state of an EPROM bit is a logic 0.

NOTE

Unlike many commercial EPROMs, an erased EPROM byte in the MCU will read as $00. All unused locations should be programmed as 0s.

14.3.3 Jump/Branch Instructions

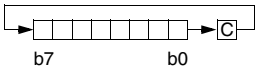
Jump instructions allow the CPU to interrupt the normal sequence of the program counter. The unconditional jump instruction (JMP) and the jump-to-subroutine instruction (JSR) have no register operand. Branch instructions allow the CPU to interrupt the normal sequence of the program counter when a test condition is met. If the test condition is not met, the branch is not performed.

The BRCLR and BRSET instructions cause a branch based on the state of any readable bit in the first 256 memory locations. These 3-byte instructions use a combination of direct addressing and relative addressing. The direct address of the byte to be tested is in the byte following the opcode. The third byte is the signed offset byte. The CPU finds the effective branch destination by adding the third byte to the program counter if the specified bit tests true. The bit to be tested and its condition (set or clear) is part of the opcode. The span of branching is from –128 to +127 from the address of the next location after the branch instruction. The CPU also transfers the tested bit to the carry/borrow bit of the condition code register.

Table 14-3. Jump and Branch Instructions

Instruction	Mnemonic
Branch if Carry Bit Clear	BCC
Branch if Carry Bit Set	BCS
Branch if Equal	BEQ
Branch if Half-Carry Bit Clear	BHCC
Branch if Half-Carry Bit Set	BHCS
Branch if Higher	BHI
Branch if Higher or Same	BHS
Branch if $\overline{IRQ}/V_{PP}$ Pin High	BIH
Branch if $\overline{IRQ}/V_{PP}$ Pin Low	BIL
Branch if Lower	BLO
Branch if Lower or Same	BLS
Branch if Interrupt Mask Clear	BMC
Branch if Minus	BMI
Branch if Interrupt Mask Set	BMS
Branch if Not Equal	BNE
Branch if Plus	BPL
Branch Always	BRA
Branch if Bit Clear	BRCLR
Branch Never	BRN
Branch if Bit Set	BRSET
Branch to Subroutine	BSR
Unconditional Jump	JMP
Jump to Subroutine	JSR

Table 14-6. Instruction Set Summary (Sheet 5 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
ROR *opr* RORA RORX ROR *opr*,X ROR ,X	Rotate Byte Right through Carry Bit		—	—	↕	↕	↕	DIR INH INH IX1 IX	36 46 56 66 76	dd ff 	5 3 3 6 5
RSP	Reset Stack Pointer	SP ← $00FF	—	—	—	—	—	INH	9C		2
RTI	Return from Interrupt	SP ← (SP) + 1; Pull (CCR) SP ← (SP) + 1; Pull (A) SP ← (SP) + 1; Pull (X) SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	↕	↕	↕	↕	þ	INH	80		6
RTS	Return from Subroutine	SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)						INH			
SBC #*opr* SBC *opr* SBC *opr* SBC *opr*,X SBC *opr*,X SBC ,X	Subtract Memory Byte and Carry Bit from Accumulator	A ← (A) – (M) – (C)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A2 B2 C2 D2 E2 F2	ii dd hh ll ee ff ff 	2 3 4 5 4 3
SEC	Set Carry Bit	C ← 1	—	—	—	—	1	INH	99		2
SEI	Set Interrupt Mask	I ← 1	—	1	—	—	—	INH	9B		2
STA *opr* STA *opr* STA *opr*,X STA *opr*,X STA ,X	Store Accumulator in Memory	M ← (A)	—	—	↕	↕	—	DIR EXT IX2 IX1 IX	B7 C7 D7 E7 F7	dd hh ll ee ff ff 	4 5 6 5 4
STOP	Stop Oscillator and Enable $\overline{\text{IRQ}}$ Pin		—	0	—	—	—	INH	8E		2
STX *opr* STX *opr* STX *opr*,X STX *opr*,X STX ,X	Store Index Register In Memory	M ← (X)	—	—	↕	↕	—	DIR EXT IX2 IX1 IX	BF CF DF EF FF	dd hh ll ee ff ff 	4 5 6 5 4
SUB #*opr* SUB *opr* SUB *opr* SUB *opr*,X SUB *opr*,X SUB ,X	Subtract Memory Byte from Accumulator	A ← (A) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A0 B0 C0 D0 E0 F0	ii dd hh ll ee ff ff 	2 3 4 5 4 3
SWI	Software Interrupt	PC ← (PC) + 1; Push (PCL) SP ← (SP) – 1; Push (PCH) SP ← (SP) – 1; Push (X) SP ← (SP) – 1; Push (A) SP ← (SP) – 1; Push (CCR) SP ← (SP) – 1; I ← 1 PCH ← Interrupt Vector High Byte PCL ← Interrupt Vector Low Byte	—	1	—	—	—	INH	83		10

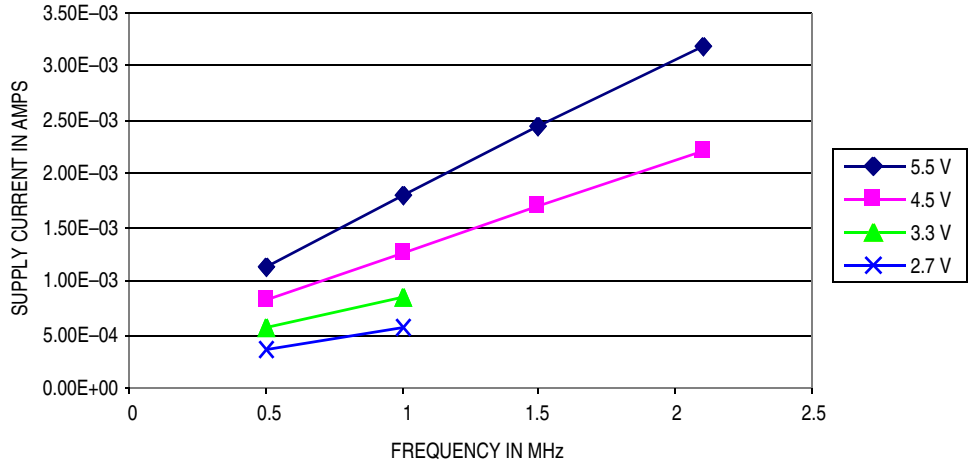


Figure 15-1. Typical Run I_{DD} versus Internal Clock Frequency at 25°C

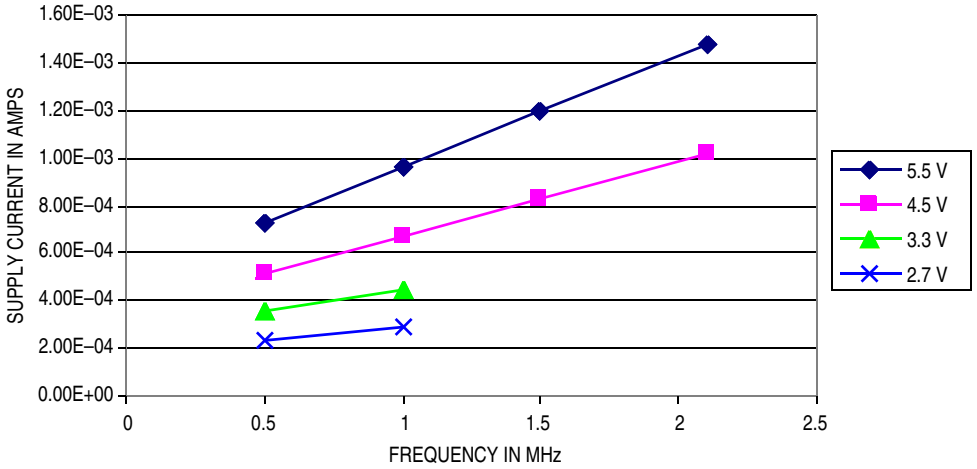


Figure 15-2. Typical Wait I_{DD} versus Internal Clock Frequency at 25°C

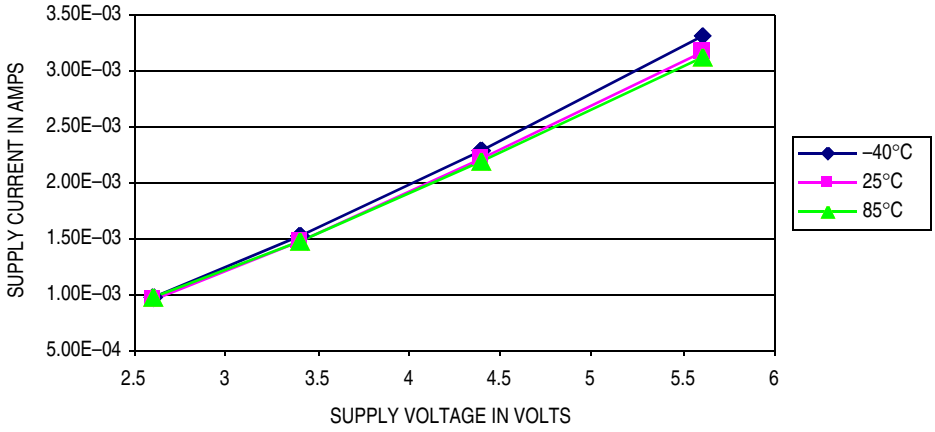


Figure 15-3. Typical Run I_{DD} with External Oscillator

15.15 SIOP Timing (V_{DD} = 3.0 Vdc)

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Frequency of operation Master Slave	 $f_{SIOP(M)}$ $f_{SIOP(S)}$	 0.25 x f_{OP} dc	 0.25 x f_{OP} —	 0.25 x f_{OP} 525	kHz
Cycle time Master Slave	 $t_{SCK(M)}$ $t_{SCK(M)}$	 4.0 x t_{cyc} —	 4.0 x t_{cyc} —	 4.0 x t_{cyc} 1.9	µs
Clock (SCK) low time (f_{OP} = 2.1 MHz)	t_{SCKL}	1905	—	—	ns
SDO data valid time	t_V	—	—	400	ns
SDO hold time	t_{HO}	0	—	—	ns
SDI setup time	t_S	200	—	—	ns
SDI hold time	t_H	200	—	—	ns

1. +2.7 ≤ V_{DD} ≤ +3.3 V, V_{SS} = 0 V, $T_L \le T_A \le T_H$, unless otherwise noted

15.16 Reset Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Low-voltage reset Rising recovery voltage Falling reset voltage LVR hysteresis	 V_{LVRR} V_{LVRF} V_{LVRH}	 2.4 2.3 30	 3.4 3.3 70	 4.4 4.3 —	 V V mV
POR recovery voltage[2]	V_{POR}	0	—	100	mV
POR V_{DD} slew rate[2] Rising[2] Falling[2]	 S_{VDDR} S_{VDDF}	 — —	 — —	 0.1 0.05	V/µs
$\overline{\text{RESET}}$ pulse width (when bus clock active)	t_{RL}	1.5	—	—	t_{CYC}
$\overline{\text{RESET}}$ pulldown pulse width from internal reset	t_{RPD}	3	—	4	t_{CYC}

1. +2.7 ≤ V_{DD} ≤ +3.3 V, V_{SS} = 0 V, $T_L \le T_A \le T_H$, unless otherwise noted
2. By design, not tested

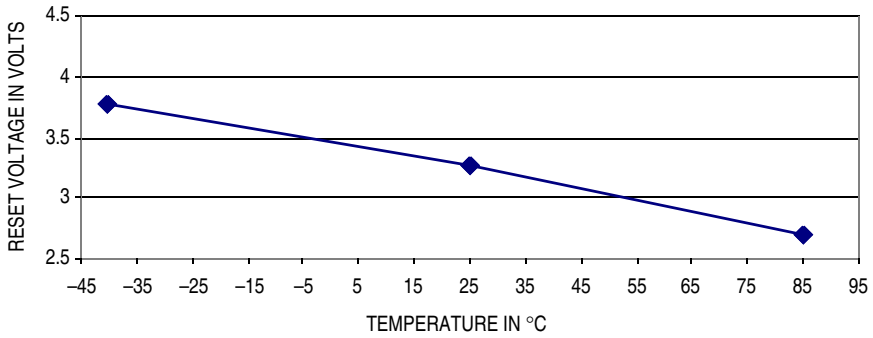
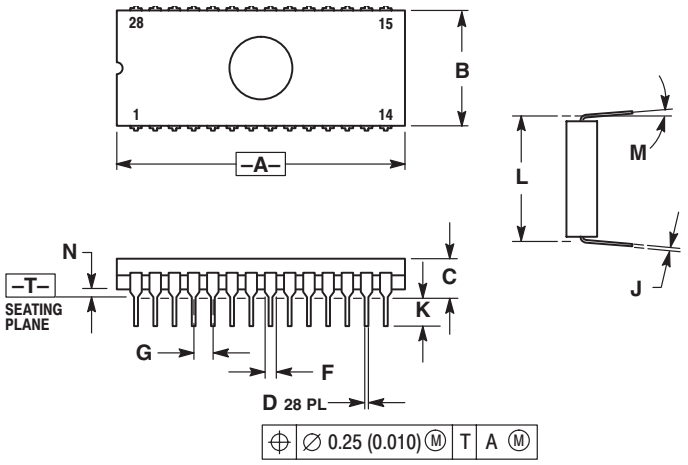


Figure 15-12. Typical Falling Low Voltage Reset

16.7 28-Pin Windowed Ceramic Integrated Circuit (Case 733A)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A AND B INCLUDE MENISCUS.
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.490	36.45	37.84
B	0.500	0.605	12.70	15.36
C	0.160	0.240	4.06	6.09
D	0.015	0.022	0.38	0.55
F	0.050	0.065	1.27	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.20	0.30
K	0.125	0.160	3.17	4.06
L	0.600 BSC		15.24 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.050	0.51	1.27

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