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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SIO
Peripherals	POR, Temp Sensor, WDT
Number of I/O	22
Program Memory Size	6KB (6K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	224 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc705jp7cdw

6.3.2 Wait Mode

The WAIT instruction puts the MCU in a low-power wait mode which consumes more power than the stop mode and affects the MCU as follows:

- Enables interrupts by clearing the I bit in the condition code register
- Enables external interrupts by setting the IRQE bit in the IRQ status and control register
- Stops the CPU clock which drives the address and data buses, but allows the selected oscillator to continue to clock the core timer, programmable timer, analog subsystem, and SIOP

The WAIT instruction does not affect any other bits, registers, or I/O lines.

These conditions restart the CPU bus clock and bring the MCU out of wait mode:

- An external interrupt signal on the $\overline{IRQ}/V_{PP}$ pin — A high-to-low transition on the $\overline{IRQ}/V_{PP}$ pin loads the program counter with the contents of locations $1FFA and $1FFB.
- An external interrupt signal on a port A external interrupt pin — If selected by PIRQ bit in the MOR, a low-to-high transition on a PA3–PA0 pin loads the program counter with the contents of locations $1FFA and $1FFB.
- A core timer interrupt — A core timer overflow or a real-time interrupt loads the program counter with the contents of locations $1FF8 and $1FF9.
- A programmable timer interrupt — A programmable timer interrupt driven by an input capture, output compare, or timer overflow loads the program counter with the contents of locations $1FF6 and $1FF7.
- An SIOP interrupt — An SIOP interrupt driven by the completion of transmitted or received 8-bit data loads the program counter with the contents of locations $1FF4 and $1FF5.
- An analog subsystem interrupt — An analog subsystem interrupt driven by a voltage comparison loads the program counter with the contents of locations $1FF2 and $1FF3.
- A COP watchdog reset — A timeout of the COP watchdog resets the MCU and loads the program counter with the contents of locations $1FFE and $1FFF. Software can enable real-time interrupts so that the MCU can periodically exit the wait mode to reset the COP watchdog.
- An external reset — A logic 0 on the $\overline{RESET}$ pin resets the MCU and loads the program counter with the contents of locations $1FFE and $1FFF.

When the MCU exits the wait mode, there is no delay before code executes like occurs when exiting the stop or halt modes.

6.3.3 Halt Mode

The STOP instruction puts the MCU in halt mode if selected by the SWAIT bit in the MOR. Halt mode is identical to wait mode, except that a variable recovery delay occurs when the MCU exits halt mode. A recovery time of from 1 to 16 or from 1 to 4064 internal bus cycles can be selected by the DELAY bit in the MOR.

If the SWAIT bit is set in the MOR to put the MCU in halt mode, the COP watchdog cannot be turned off inadvertently by a STOP instruction.

Address: $001D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	CHG	ATD2	ATD1	ICEN	CPIE	CP2EN	CP1EN	ISEN
Reset:	0	0	0	0	0	0	0	0

Figure 8-5. Analog Control Register (ACR)

CHG

The CHG enable bit allows direct control of the charge current source and the discharge device and also reflects the state of the discharge device. This bit is cleared by a reset of the device.

1 = If the ISEN bit is also set, the charge current source is sourcing current out of the PB0/AN0 pin. Writing a logic 1 enables the charging current out of the PB0/AN0 pin.

0 = The discharge device is sinking current into the PB0/AN0 pin. Writing a logic 0 disables the charging current and enables the discharging current into the PB0/AN0 pin, if the ISEN bit is also set.

ATD1–ATD2

The ATD1–ATD2 enable bits select one of the four operating modes used for making A/D conversions via the single-slope method.These four modes are given in Table 8-3. These bits have no effect if the ISEN enable bit is cleared. These bits are cleared by a reset of the device and thereby return the analog subsystem to the manual A/D conversion method.

Table 8-3. A/D Conversion Options

A/D Option Mode	Charge Control	A/D Options				Current Flow to/from PB0/AN0
		ISEN	ATD2	ATD1	CHG	
Disabled	Current source and discharge disabled	0	X	X	X	Current control disabled, no source or sink current
		1	0	0	1	Begin sourcing current when the CHG bit is set and continue to source current until the CHG bit is cleared.
		1	1	0	1	The CHG bit remains set until the next time ICF occurs.
3	Automatic charge and discharge (OCF–ICF) synchronized to timer	1	1	1	0	The CHG bit remains cleared until the next time OCF occurs.
		1	1	1	1	The CHG bit remains set until the next time ICF occurs.

ICEN

This is a read/write bit that enables a voltage comparison to trigger the input capture register of the programmable timer when the CPF2 flag bit is set. Therefore, an A/D conversion could be started by receiving an OCF or TOF from the programmable timer and then terminated when the voltage on the external ramping capacitor reaches the level of the unknown voltage. The time of termination will be stored in the 16-bit buffer located at $0014 and $0015. This bit is automatically set whenever mode 2 or 3 is selected by setting the ATD2 control bit. This bit is cleared by a reset of the device.

1 = Connects the CPF2 flag bit to the timer input capture register
0 = Connects the PB3/AN3 pin to the timer input capture register

NOTE

For the input capture to occur when the output of comparator 2 goes high, the IEDG bit in the TCR must also be set.

When the ICEN bit is set, the input capture function of the programmable timer is not connected to the PB3/AN3/TCAP pin but is driven by the CPF2 output flag from comparator 2. To return to capturing times from external events, the ICEN bit must first be cleared before the timed event occurs.

CPIE

This is a read/write bit that enables an analog interrupt when either of the CPF1 or CPF2 flag bits is set to a logic 1. This bit is cleared by a reset of the device.

1 = Enables analog interrupts when comparator flag bits are set
0 = Disables analog interrupts when comparator flag bits are set

NOTE

If both the ICEN and CPIE bits are set, they will both generate an interrupt by different paths. One will be the programmable timer interrupt due to the input capture and the other will be the analog interrupt due to the output of comparator 2 going high. In this case, the input capture interrupt will be entered first due to its higher priority. The analog interrupt will then need to be serviced even if the comparator 2 output has been reset or the input capture flag (ICF) has been cleared.

CP2EN

The CP2EN enable bit controls power to voltage comparator 2 in the analog subsystem. Powering down a comparator will drop the supply current. This bit is cleared by a reset of the device.

1 = Writing a logic 1 powers up voltage comparator 2.
0 = Writing a logic 0 powers down voltage comparator 2.

NOTE

Voltage comparators power up slower than digital logic and their outputs may go through indeterminate states which might set their respective flags (CPF1, CPF2). It is therefore recommended to power up the charge current source first (ISEN), then to power up any comparators, and finally clear the flag bits by writing a logic 1 to the respective CPFR1 or CPFR2 bits in the ACR.

CP1EN

The CP1EN enable bit will power down the voltage comparator 1 in the analog subsystem. Powering down a comparator will drop the supply current. This bit is cleared by a reset of the device.

1 = Writing a logic 1 powers up voltage comparator 1
0 = Writing a logic 0 powers down voltage comparator 1

8.7 Voltage Comparator Features

The two internal comparators can be used as simple voltage comparators if set up as described in Table 8-8. Both comparators can be active in the wait mode and can directly restart the part by means of the analog interrupt. Both comparators can also be active in the stop mode, but cannot directly restart the part. However, the comparators can directly drive PB4 which can then be connected externally to activate either a port interrupt on the PA0:3 pins or the $\overline{IRQ}/V_{PP}$ pin.

Table 8-8. Voltage Comparator Setup Conditions

Comparator	Current Source Enable	Discharge Device Disable	Port B Pin as Inputs	Port B Pin Pulldowns Disabled	Prog. Timer Input Capture Source
1	Not affected	Not affected	DDRB2 = 0 DDRB3 = 0	PDIB2 = 1 PDIB3 = 1	Not affected
2	ISEN = 0	ISEN = 0	DDRB0 = 0 DDRB1 = 0	PDIB0 = 1 PDIB1 = 1	ICEN = 0 IEDG = 1

8.7.1 Voltage Comparator 1

Voltage comparator 1 is always connected to two of the port B I/O pins. These pins should be configured as inputs and have their software programmable pulldowns disabled. Also, the negative input of voltage comparator 1 is connected to the PB3/AN3/TCAP and shared with the input capture function of the 16-bit programmable timer. Therefore, the timer input capture interrupt should be disabled so that changes in the voltage on the PB3/AN3/TCAP pin do not cause unwanted input capture interrupts.

The output of comparator 1 can be connected to the port logic driving the PB4/AN4/TCMP/CMP1 pin such that the output of the comparator is ORed with the PB4 data bit and the OLVL bit from the 16-bit timer. This capability requires that the OPT bit is set in the COPR at location $1FF0 as in Figure 8-12, and the COE1 bit is set in the ASR at location $001E.

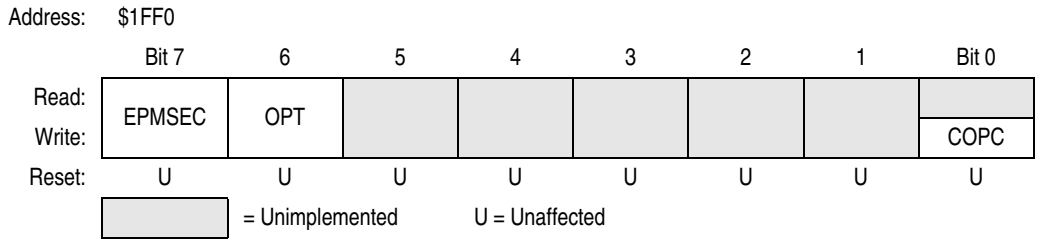


Figure 8-12. COP and Security Register (COPR)

OPT — Optional Features Bit

The OPT bit enables two additional features: direct drive by comparator 1 output to PB4 and voltage offset capability to sample capacitor in analog subsystem.

1 = Optional features enabled
0 = Optional features disabled

Chapter 9
Simple Synchronous Serial Interface

9.1 Introduction

The simple synchronous serial I/O port (SIOP) subsystem is designed to provide efficient serial communications with peripheral devices or other MCUs. SIOP is implemented as a 3-wire master/slave system with serial clock (SCK), serial data input (SDI), and serial data output (SDO). A block diagram of the SIOP is shown in Figure 9-1.

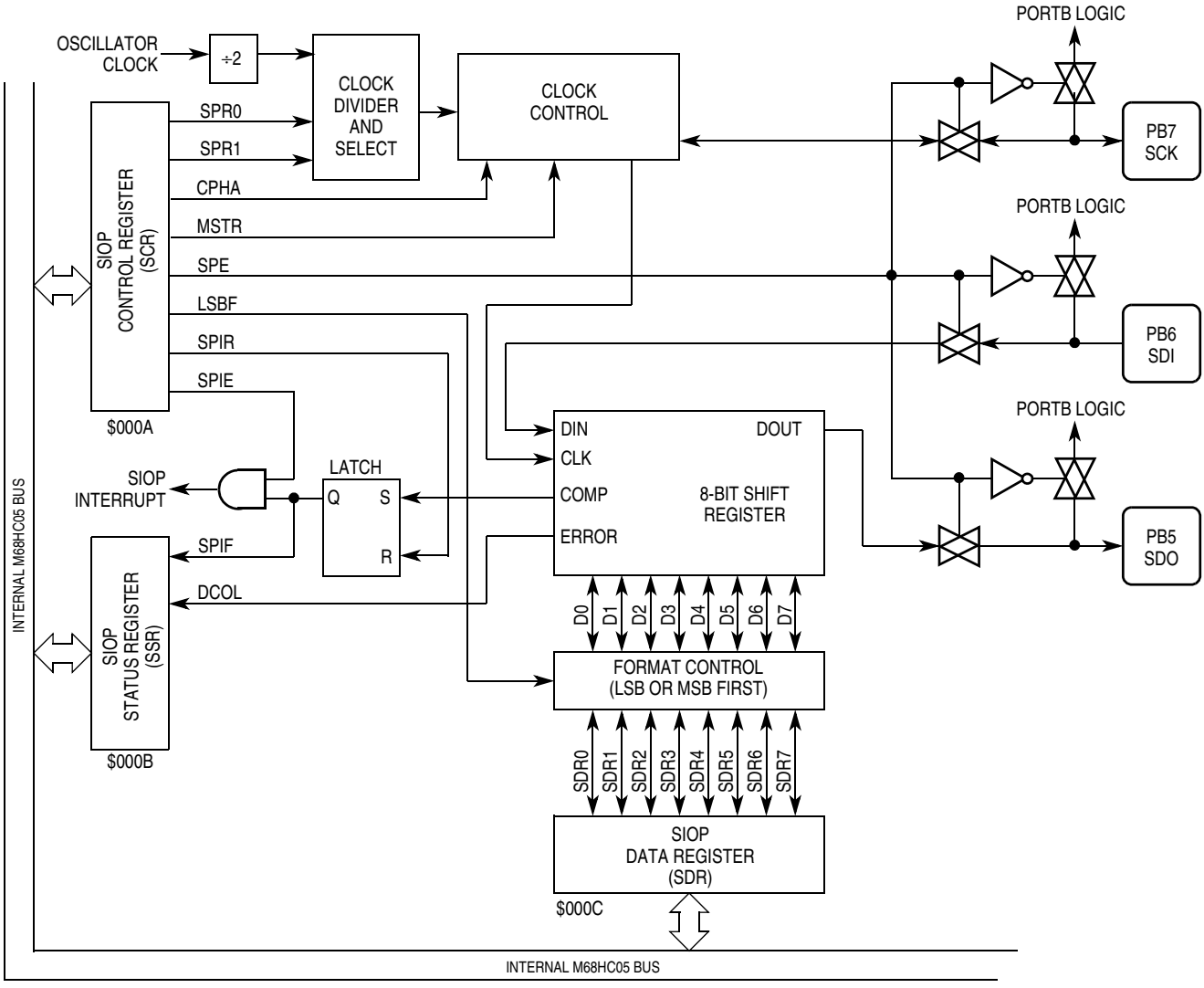


Figure 9-1. SIOP Block Diagram

9.3.3 SIOP Data Register

The SIOP data register (SDR) is located at address $000C and serves as both the transmit and receive data register. Writing to this register will initiate a message transmission if the node is in master mode. The SIOP subsystem is not double buffered and any write to this register will destroy the previous contents. The SDR can be read at any time. However, if a transfer is in progress the results may be ambiguous. Writing to the SDR while a transfer is in progress can cause invalid data to be transmitted and/or received. Figure 9-6 shows the position of each bit in the register. This register is not affected by reset.

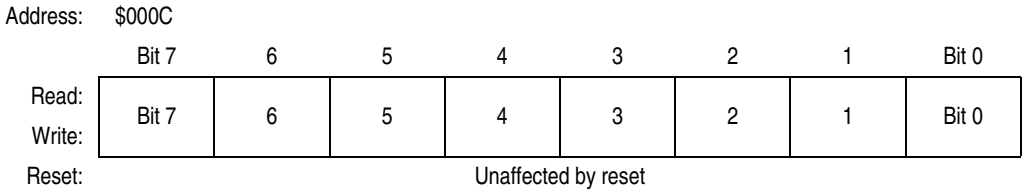


Figure 9-6. SIOP Data Register (SDR)

Chapter 10
Core Timer

10.1 Introduction

This section describes the operation of the core timer and the computer operating properly (COP) watchdog as shown by the block diagram in Figure 10-1.

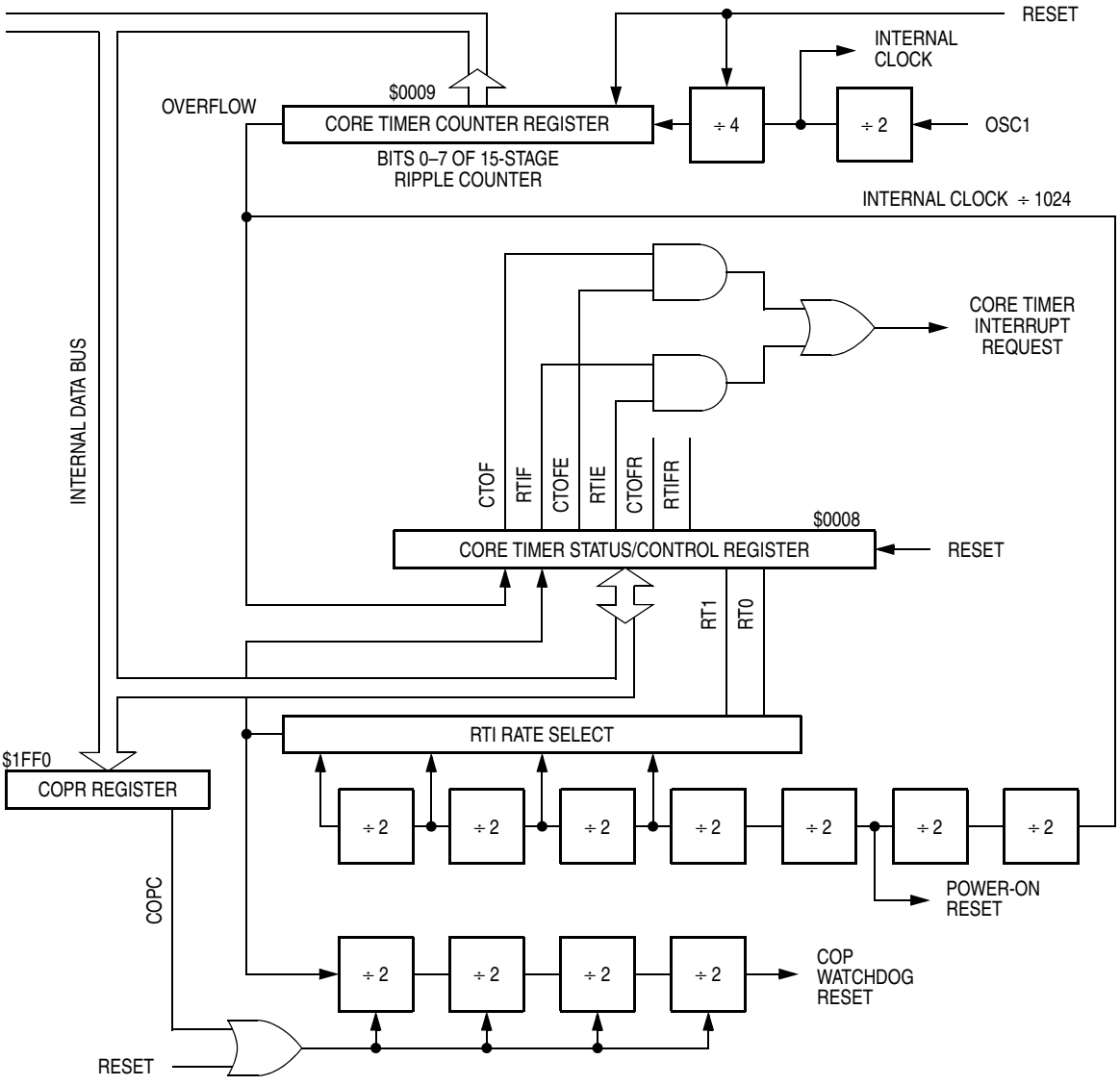


Figure 10-1. Core Timer Block Diagram

Chapter 11
Programmable Timer

11.1 Introduction

The MC68HC705JJ7/MC68HC705JP7 MCU contains a 16-bit programmable timer with an input capture function and an output compare function as shown by the block diagram in Figure 11-1.

The basis of the capture/compare timer is a 16-bit free-running counter which increases in count with every four internal bus clock cycles. The counter is the timing reference for the input capture and output compare functions. The input capture and output compare functions provide a means to latch the times at which external events occur, to measure input waveforms, and to generate output waveforms and timing delays. Software can read the value in the 16-bit free-running counter at any time without affecting the counter sequence.

The input/output (I/O) registers for the input capture and output compare functions are pairs of 8-bit registers, because of the 16-bit timer architecture used. Each register pair contains the high and low bytes of that function. Generally, accessing the low byte of a specific timer function allows full control of that function; however, an access of the high byte inhibits that specific timer function until the low byte is also accessed.

Because the counter is 16 bits long and preceded by a fixed divide-by-four prescaler, the counter rolls over every 262,144 internal clock cycles (every 524,288 oscillator clock cycles). Timer resolution with a 4-MHz crystal oscillator is 2 microseconds/count.

The interrupt capability, the input capture edge, and the output compare state are controlled by the timer control register (TCR) located at $0012, and the status of the interrupt flags can be read from the timer status register (TSR) located at $0013.

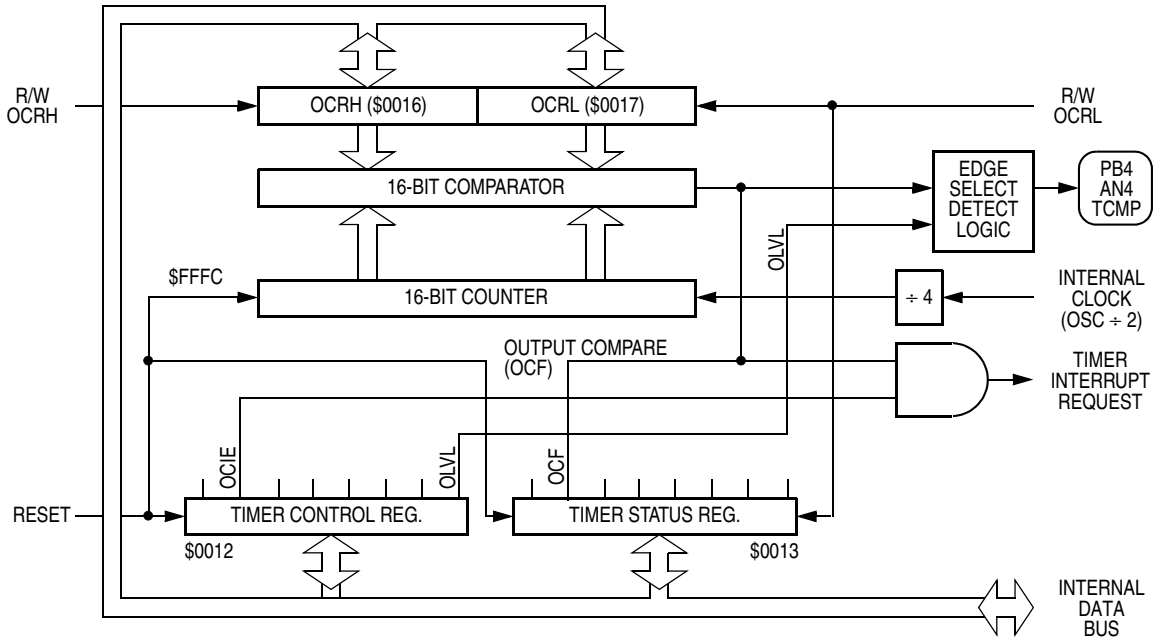


Figure 11-8. Timer Output Compare Block Diagram

Figure 11-9. Output Compare Registers (OCRH and OCRL)

Writing to the OCRH before writing to the OCRL inhibits timer compares until the OCRL is written. Reading or writing to the OCRL after reading the TCR will clear the output compare flag bit (OCF). The output compare OLVL state will be clocked to its output latch regardless of the state of the OCF.

To prevent OCF from being set between the time it is read and the time the output compare registers are updated, use this procedure:

1. Disable interrupts by setting the I bit in the condition code register.
2. Write to the OCRH. Compares are now inhibited until OCRL is written.
3. Read the TSR to arm the OCF for clearing.
4. Enable the output compare registers by writing to the OCRL. This also clears the OCF flag bit in the TSR.
5. Enable interrupts by clearing the I bit in the condition code register.

A software example of this procedure is shown in Table 11-1.

TOF — Timer Overflow Flag

The TOF bit is automatically set when the 16-bit timer counter rolls over from $FFFF to $0000. Clear the TOF bit by reading the timer status register with the TOF set and then accessing the low byte (TMRL, $0019) of the timer registers. Resets have no effect on TOF.

11.8 Timer Operation during Wait Mode

During wait mode, the 16-bit timer continues to operate normally and may generate an interrupt to trigger the MCU out of wait mode.

11.9 Timer Operation during Stop Mode

When the MCU enters stop mode, the free-running counter stops counting (the internal processor clock is stopped). It remains at that particular count value until stop mode is exited by applying a low signal to the $\overline{IRQ}/V_{PP}$ pin, at which time the counter resumes from its stopped value as if nothing had happened. If stop mode is exited via an external reset (logic low applied to the $\overline{RESET}$ pin), the counter is forced to $FFFC.

If a valid input capture edge occurs during stop mode, the input capture detect circuitry will be armed. This action does not set any flags or wake up the MCU, but when the MCU does wake up there will be an active input capture flag (and data) from the first valid edge. If the stop mode is exited by an external reset, no input capture flag or data will be present even if a valid input capture edge was detected during stop mode.

11.10 Timer Operation during Halt Mode

When the MCU enters halt mode, the functions and states of the 16-bit programmable timer are the same as for wait mode described in 11.8 Timer Operation during Wait Mode.

Chapter 12
Personality EPROM (PEPROM)

12.1 Introduction

This section describes how to program the 64-bit personality erasable programmable read-only memory (PEPROM). Figure 12-1 shows the structure of the PEPROM subsystem.

NOTE

In packages with no quartz window, the PEPROM functions as one-time programmable ROM (OTPROM).

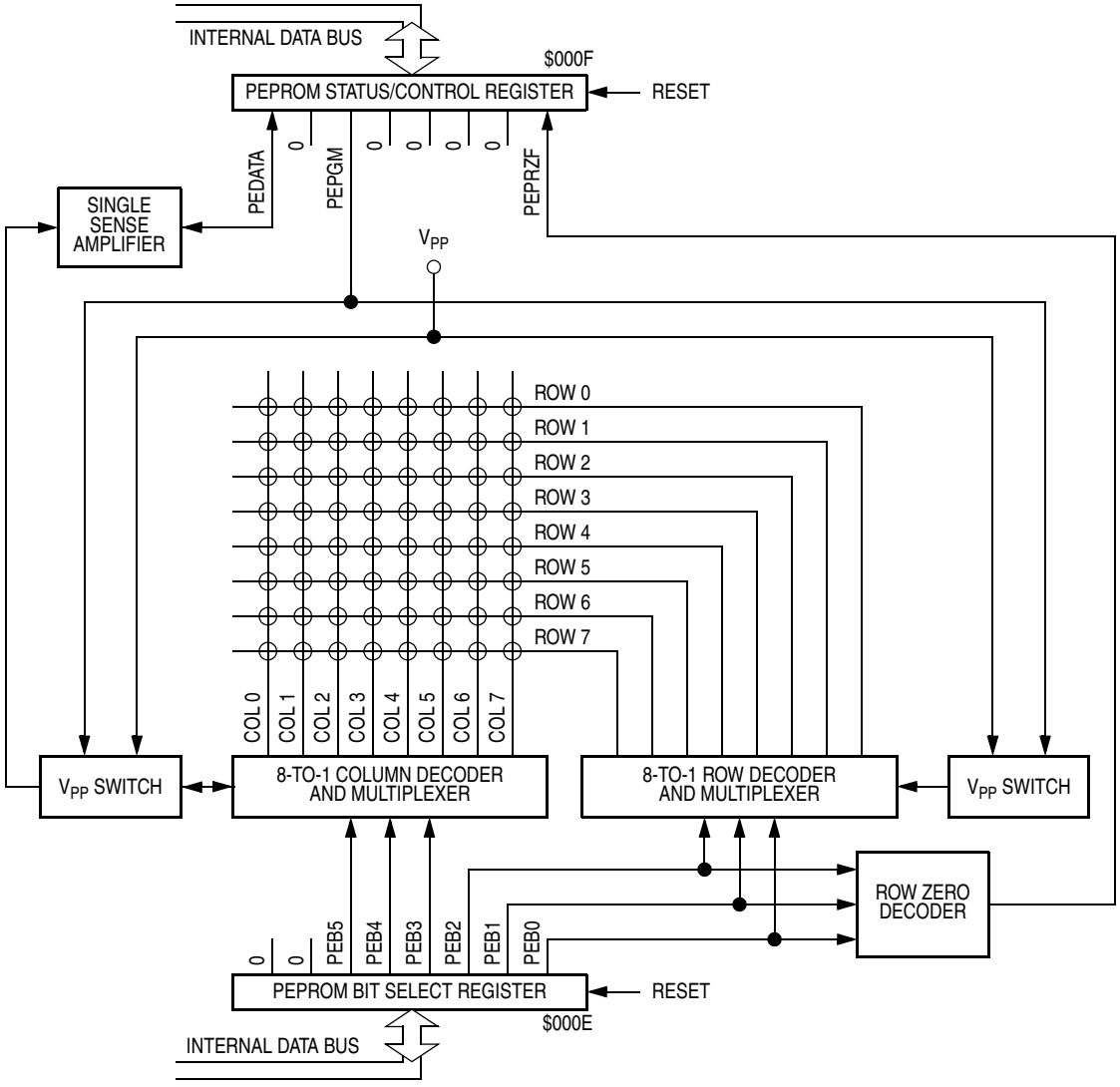


Figure 12-1. Personality EPROM Block Diagram

13.2.3 EPROM Security Bit

An EPROM programmable bit is provided at the location of the COP watchdog register at $1FF0 as shown in Figure 13-3. This bit allows control of access to the EPROM array. Any accesses of the EPROM locations will return undefined results when the EPMSEC bit is set. Refer to 13.3.2 EPMSEC Programming for programming instructions.

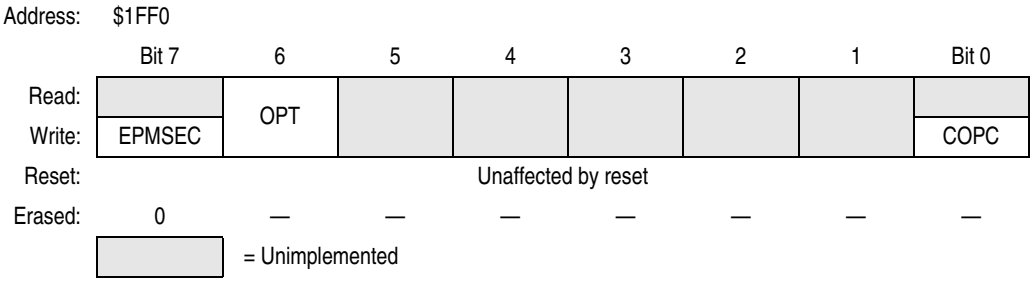


Figure 13-3. EPROM Security in COP and Security Register (COPR)

EPMSEC — EPROM Security[1]

This EPROM write-only bit enables the access to the EPROM array.

1 = Access to the EPROM array in non-user modes is denied.

0 = Access to the EPROM array in non-user modes is enabled.

13.3 EPROM Programming

A programming board is available from Freescale to download to the on-chip EPROM/OTPROM using the factory-provided programming software. Factory-provided software for programming the PEPROM is available on the World Wide Web at:

http://www.freescale.com

The programming software copies to the 6144-byte space located at EPROM addresses $0700–$1EFF and to the 16-byte space at addresses $1FF0–$1FFF which includes the mask option register at address $1FF1, and the security bit at address $1FF0.

NOTE

To program the EPROM/OTPROM, MOR, or EPMSEC bits properly, the V_{DD} voltage must be greater than 4.5 volts.

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the EPROM/OTPROM difficult for unauthorized users.

14.3.2 Read-Modify-Write Instructions

These instructions read a memory location or a register, modify its contents, and write the modified value back to the memory location or to the register.

NOTE

Do not use read-modify-write operations on write-only registers.

Table 14-2. Read-Modify-Write Instructions

Instruction	Mnemonic
Arithmetic Shift Left (Same as LSL)	ASL
Arithmetic Shift Right	ASR
Bit Clear	BCLR(1)
Bit Set	BSET(1)
Clear Register	CLR
Complement (One's Complement)	COM
Decrement	DEC
Increment	INC
Logical Shift Left (Same as ASL)	LSL
Logical Shift Right	LSR
Negate (Two's Complement)	NEG
Rotate Left through Carry Bit	ROL
Rotate Right through Carry Bit	ROR
Test for Negative or Zero	TST(2)

1. Unlike other read-modify-write instructions, BCLR and BSET use only direct addressing.
2. TST is an exception to the read-modify-write sequence because it does not write a replacement value.

14.4 Instruction Set Summary

Table 14-6. Instruction Set Summary (Sheet 1 of 6)

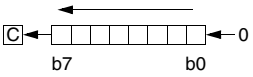
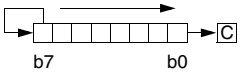
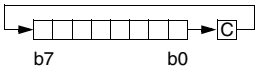
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
ADC #*opr* ADC *opr* ADC *opr* ADC *opr*,X ADC *opr*,X ADC ,X	Add with Carry	A ← (A) + (M) + (C)	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A9 B9 C9 D9 E9 F9	ii dd hh ll ee ff ff	2 3 4 5 4 3
ADD #*opr* ADD *opr* ADD *opr* ADD *opr*,X ADD *opr*,X ADD ,X	Add without Carry	A ← (A) + (M)	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	AB BB CB DB EB FB	ii dd hh ll ee ff ff	2 3 4 5 4 3
AND #*opr* AND *opr* AN*D opr* AND *opr*,X AND *opr*,X AND ,X	Logical AND	A ← (A) ∧ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A4 B4 C4 D4 E4 F4	ii dd hh ll ee ff ff	2 3 4 5 4 3
ASL *opr* ASLA ASLX ASL *opr*,X ASL ,X	Arithmetic Shift Left (Same as LSL)		—	—	↕	↕	↕	DIR INH INH IX1 IX	38 48 58 68 78	dd ff 	5 3 3 6 5
ASR *opr* ASRA ASRX ASR *opr*,X ASR ,X	Arithmetic Shift Right		—	—	↕	↕	↕	DIR INH INH IX1 IX	37 47 57 67 77	dd ff 	5 3 3 6 5
BCC *rel*	Branch if Carry Bit Clear	PC ← (PC) + 2 + *rel* ? C = 0	—	—	—	—	—	REL	24	rr	3
BCLR *n opr*	Clear Bit n	Mn ← 0	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5
BCS *rel*	Branch if Carry Bit Set (Same as BLO)	PC ← (PC) + 2 + *rel* ? C = 1	—	—	—	—	—	REL	25	rr	3
BEQ *rel*	Branch if Equal	PC ← (PC) + 2 + *rel* ? Z = 1	—	—	—	—	—	REL	27	rr	3
BHCC *rel*	Branch if Half-Carry Bit Clear	PC ← (PC) + 2 + *rel* ? H = 0	—	—	—	—	—	REL	28	rr	3
BHCS *rel*	Branch if Half-Carry Bit Set	PC ← (PC) + 2 + *rel* ? H = 1	—	—	—	—	—	REL	29	rr	3
BHI *rel*	Branch if Higher	PC ← (PC) + 2 + *rel* ? C ∨ Z = 0	—	—	—	—	—	REL	22	rr	3

Table 14-6. Instruction Set Summary (Sheet 5 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
ROR *opr* RORA RORX ROR *opr*,X ROR ,X	Rotate Byte Right through Carry Bit		—	—	↕	↕	↕	DIR INH INH IX1 IX	36 46 56 66 76	dd ff 	5 3 3 6 5
RSP	Reset Stack Pointer	SP ← $00FF	—	—	—	—	—	INH	9C		2
RTI	Return from Interrupt	SP ← (SP) + 1; Pull (CCR) SP ← (SP) + 1; Pull (A) SP ← (SP) + 1; Pull (X) SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	↕	↕	↕	↕	þ	INH	80		6
RTS	Return from Subroutine	SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)						INH			
SBC #*opr* SBC *opr* SBC *opr* SBC *opr*,X SBC *opr*,X SBC ,X	Subtract Memory Byte and Carry Bit from Accumulator	A ← (A) – (M) – (C)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A2 B2 C2 D2 E2 F2	ii dd hh ll ee ff ff 	2 3 4 5 4 3
SEC	Set Carry Bit	C ← 1	—	—	—	—	1	INH	99		2
SEI	Set Interrupt Mask	I ← 1	—	1	—	—	—	INH	9B		2
STA *opr* STA *opr* STA *opr*,X STA *opr*,X STA ,X	Store Accumulator in Memory	M ← (A)	—	—	↕	↕	—	DIR EXT IX2 IX1 IX	B7 C7 D7 E7 F7	dd hh ll ee ff ff 	4 5 6 5 4
STOP	Stop Oscillator and Enable $\overline{\text{IRQ}}$ Pin		—	0	—	—	—	INH	8E		2
STX *opr* STX *opr* STX *opr*,X STX *opr*,X STX ,X	Store Index Register In Memory	M ← (X)	—	—	↕	↕	—	DIR EXT IX2 IX1 IX	BF CF DF EF FF	dd hh ll ee ff ff 	4 5 6 5 4
SUB #*opr* SUB *opr* SUB *opr* SUB *opr*,X SUB *opr*,X SUB ,X	Subtract Memory Byte from Accumulator	A ← (A) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A0 B0 C0 D0 E0 F0	ii dd hh ll ee ff ff 	2 3 4 5 4 3
SWI	Software Interrupt	PC ← (PC) + 1; Push (PCL) SP ← (SP) – 1; Push (PCH) SP ← (SP) – 1; Push (X) SP ← (SP) – 1; Push (A) SP ← (SP) – 1; Push (CCR) SP ← (SP) – 1; I ← 1 PCH ← Interrupt Vector High Byte PCL ← Interrupt Vector Low Byte	—	1	—	—	—	INH	83		10

15.5 Supply Current Characteristics (V_{DD} = 4.5 to 5.5 Vdc)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
RUN[3] **(**analog a**nd LVR** disabled**)**					
Internal low-power oscillator at 100 kHz	I_{DD}	—	150	568	µA
Internal low-power oscillator at 500 kHz		—	375	1100	µA
External oscillator running at 4.2 MHz		—	3.00	5.20	mA
WAIT[4] **(**ana**log and LVR** disabled**)**					
Internal low-power oscillator at 100 kHz	I_{DD}	—	45	85	µA
Internal low-power oscillator at 500 kHz		—	75	375	µA
External oscillator running at 4.2 MHz		—	1.00	2.20	mA
STOP[5] **(**analo**g and LVR** disabled**)**					
Typical	I_{DD}	—	2	10	µA
–40°C to 85°C		—	4	20	
Incremental I_{DD} for enabled mod**ules**					
LVR	I_{DD}	—	5	15	µA
Analog subsystem		—	380	475	

1. V_{DD} = 4.5 to 5.5 Vdc, V_{SS} = 0 V, $T_L \le T_A \le T_H$, unless otherwise noted. All values shown reflect average measurements.
2. Typical values at midpoint of voltage range, 25°C only
3. Run (Operating) I_{DD}, Wait I_{DD}: Measured using external square wave clock source to OSC1 pin or internal oscillator, all inputs 0.2 Vdc from either supply rail (V_{DD} or V_{SS}); no dc loads, less than 50 pF on all outputs, C_L = 20 pF on OSC2.
4. Wait I_{DD} is affected linearly by the OSC2 capacitance.
5. Stop I_{DD}: All ports configured as inputs, V_{IL} = 0.2 Vdc, V_{IH} = V_{DD} –0.2 Vdc, OSC1 = V_{DD}.

15.6 Supply Current Characteristics (V_{DD} = 2.7 to 3.3 Vdc)

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
RUN[3] **(**analog an**d LVR** disabled**)**					
Internal low-power oscillator at 100 kHz	I_{DD}	—	70	320	µA
Internal low-power oscillator at 500 kHz		—	320	800	µA
External oscillator running at 2.1 MHz		—	1.25	2.60	mA
WAIT[4] **(**analog a**nd LVR** disabled**)**					
Internal low-power oscillator at 100 kHz	I_{DD}	—	20	65	µA
Internal low-power oscillator at 500 kHz		—	40	250	µA
External oscillator running at 2.1 MHz		—	0.50	1.10	mA
STOP[5] **(**analog **and LVR** disabled**)**					
25°C	I_{DD}	—	1	5	µA
–40°C to 85°C		—	2	10	
Incremental I_{DD} for enabled modul**es**					
LVR	I_{DD}	—	5	15	µA
Analog subsystem		—	380	475	

1. V_{DD} = 2.7 to 3.3 Vdc, V_{SS} = 0 V, $T_L \le T_A \le T_H$, unless otherwise noted. All values shown reflect average measurements.
2. Typical values at midpoint of voltage range, 25°C only.
3. Run (Operating) I_{DD}, Wait I_{DD}: Measured using external square wave clock source to OSC1 pin or internal oscillator, all inputs 0.2 Vdc from either supply rail (V_{DD} or V_{SS}); no dc loads, less than 50 pF on all outputs, C_L = 20 pF on OSC2.
4. Wait I_{DD} is affected linearly by the OSC2 capacitance.
5. Stop I_{DD}: All ports configured as inputs, V_{IL} = 0.2 Vdc, V_{IH} = V_{DD} –0.2 Vdc, OSC1 = V_{DD}.

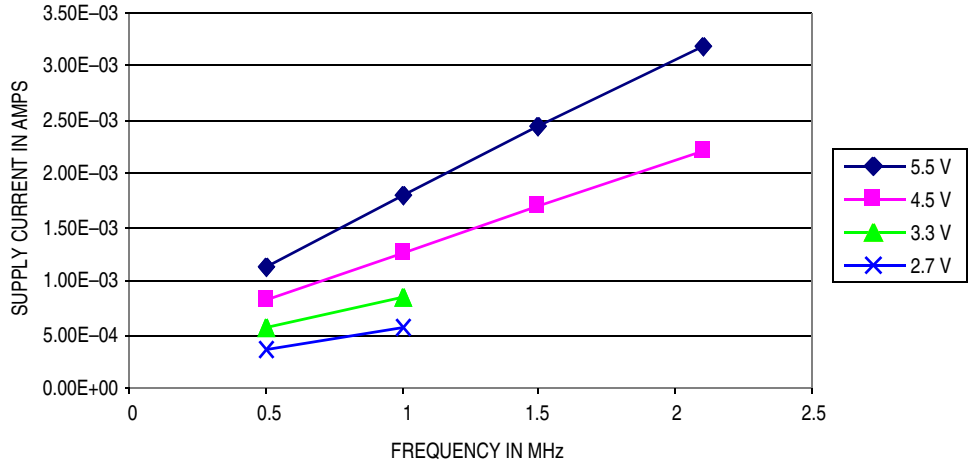


Figure 15-1. Typical Run I_{DD} versus Internal Clock Frequency at 25°C

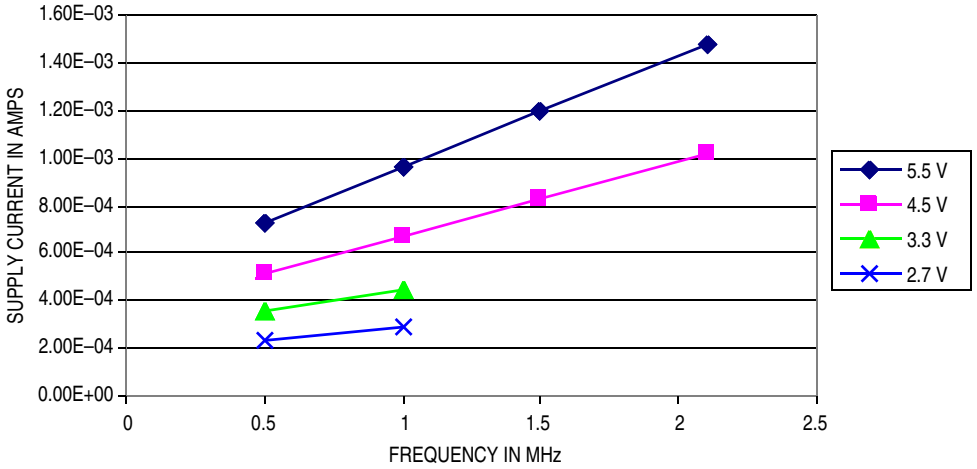


Figure 15-2. Typical Wait I_{DD} versus Internal Clock Frequency at 25°C

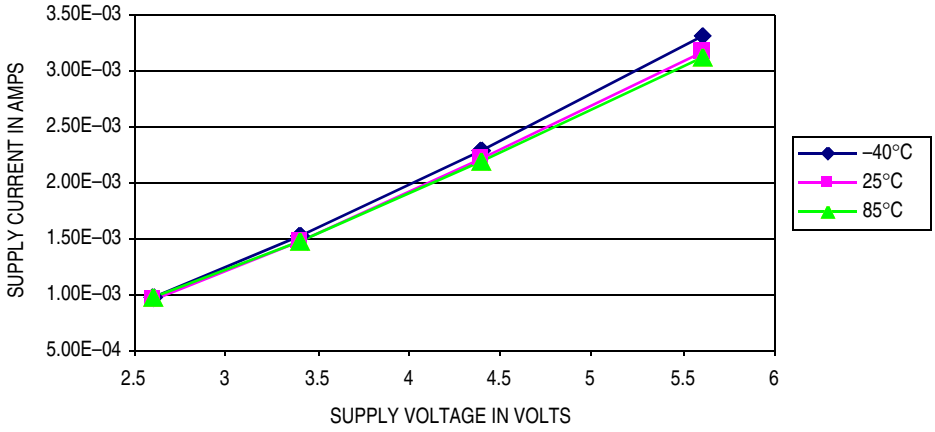


Figure 15-3. Typical Run I_{DD} with External Oscillator

15.12 Control Timing (3.0 Vdc)

Characteristic[1]	Symbol	Min	Max	Unit
Frequency of oscillation (OSC)				
RC oscillator option	f_{OSC}	—	2.1	MHz
Crystal oscillator option		0.1	2.1	MHz
External clock source		dc	2.1	MHz
Internal low-power oscillator				
Standard product (100 kHz nominal)		60	140	kHz
Mask option (500 kHz nominal, see Note 3))		300	700	kHz
Internal operating frequency, crystal, or external clock ($f_{OSC}/2$)				
RC oscillator option	f_{OP}	—	1.05	MHz
Crystal oscillator option		0.05	1.05	MHz
External clock source		dc	1.05	MHz
Internal low-power oscillator				
Standard product (100 kHz nominal)		30	70	kHz
Mask option (500 kHz nominal[2])		150	350	kHz
Cycle time ($1/f_{OP}$)				
External oscillator or clock source	t_{cyc}	952	—	ns
Internal low-power oscillator				
Standard product (100 kHz nominal)		14.29	33.33	µs
Mask option (500 kHz nominal[2])		2.86	6.67	µs
16-bit timer				
Resolution	t_{RESL}	4.0	—	t_{cyc}
Input capture (TCAP) pulse width	t_{TH}, t_{TL}	284	—	ns
Interrupt pulse width low (edge-triggered)	t_{ILIH}	284	—	ns
Interrupt pulse period	t_{ILIL}	[3]	—	t_{cyc}
OSC1 pulse width (external clock input)	t_{OH}, t_{OL}	110	—	ns
Analog subsystem response				
Voltage comparators				
Switching time (10 mV overdrive, either input)	t_{CPROP}	—	2	µs
Comparator power-up delay (bias circuit already powered up)	t_{CDELAY}	—	2	µs
External current source (PB0/AN0)				
Switching time (I_{DIS} to I_{RAMP})	t_{ISTART}	—	1	µs
Power-up delay (bias circuit already powered up)	t_{IDELAY}	—	2	µs
Bias circuit power-up delay	t_{BDELAY}	—	2	µs

1. $+2.7 \le V_{DD} \le +3.3$ V, $V_{SS} = 0$ V, $T_L \le T_A \le T_H$, unless otherwise noted
2. The 500 kHz nominal mask option is available through special order only. Contact your local Freescale sales representative for detailed ordering information. Not offered with the RC oscillator option.
3. The minimum period, t_{ILIL}, should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{cyc}.