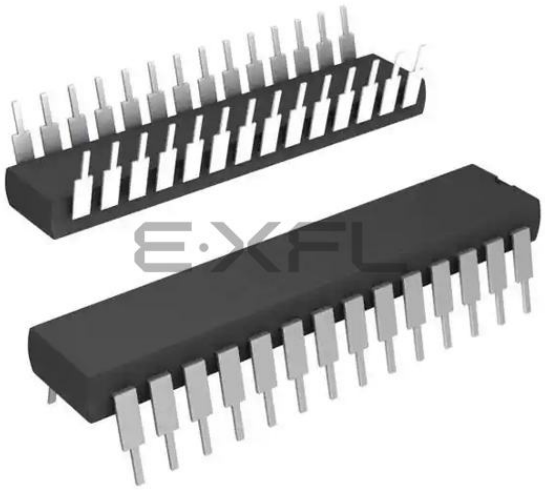


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SIO
Peripherals	POR, Temp Sensor, WDT
Number of I/O	22
Program Memory Size	6KB (6K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	224 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc705jp7cpe

MC68HC705JJ7 MC68HRC705SJ7
MC68HC705SJ7 MC68HC705JP7
MC68HRC705JJ7 MC68HC705SP7

Advance Information Data Sheet

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://www.freescale.com/

List of Chapters

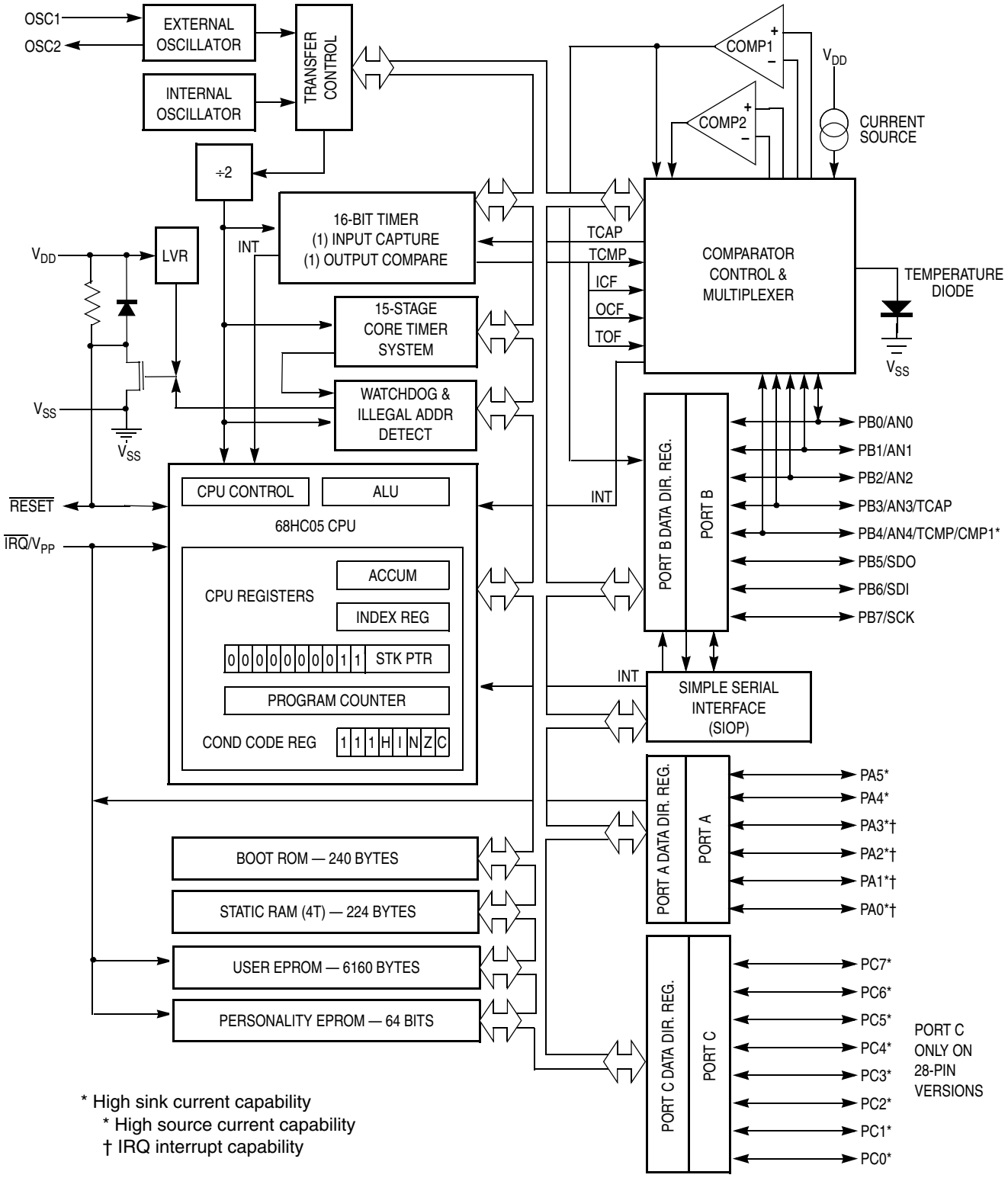


Figure 1-1. User Mode Block Diagram

2.4 User and Interrupt Vector Mapping

The interrupt vectors are contained in the upper memory addresses above $1FF0 as shown in Figure 2-4.

Address	Register Name
$1FF0	COP Register and EPROM Security
$1FF1	Mask Option Register
$1FF2	Analog Interrupt Vector (MSB)
$1FF3	Analog Interrupt Vector (LSB)
$1FF4	Serial Interrupt Vector (MSB)
$1FF5	Serial Interrupt Vector ((LSB)
$1FF6	Timer Interrupt Vector (MSB)
$1FF7	Timer Interrupt Vector (LSB)
$1FF8	Core Timer Interrupt Vector (MSB)
$1FF9	Core Timer Interrupt Vector (LSB)
$1FFA	External IRQ Vector (MSB)
$1FFB	External IRQ Vector (LSB)
$1FFC	SWI Vector (MSB)
$1FFD	SWI Vector (LSB)
$1FFE	Reset Vector (MSB)
$1FFF	Reset Vector (LSB)

Figure 2-4. Vector Mapping

2.5 Random-Access Memory (RAM)

The 224 addresses from $0020 to $00FF serve as both the user RAM and the stack RAM. The central processor unit (CPU) uses five RAM bytes to save all CPU register contents before processing an interrupt. During a subroutine call, the CPU uses two bytes to store the return address. The stack pointer decrements during pushes and increments during pulls.

NOTE

Be careful when using nested subroutines or multiple interrupt levels. The CPU may overwrite data in the RAM during a subroutine or during the interrupt stacking operation.

2.6 Erasable Programmable Read-Only Memory (EPROM)

The EPROM is located in three areas of the memory map:

- Addresses $0700–$1EFF contain 6144 bytes of user EPROM.
- Addresses $1FF0–$1FF1 contain 2 bytes of EPROM reserved for user vectors and COP and security register (COPR), and the mask option register. Only bit 7 of $1FF0 is a programmable bit.
- Addresses $1FF2–$1FFF contain 14 bytes of interrupt vectors.

2.7 COP Register

As shown in Figure 2-5, a register location is provided at $1FF0 to set the EPROM security[1], select the optional features, and reset the COP watchdog timer. The OPT bit controls the function of the PB4 port pin and the availability to add an offset to any measured analog voltages. See 8.4 Analog Status Register for more information

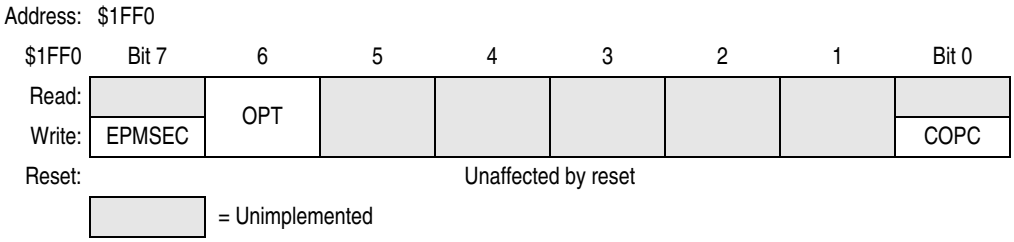


Figure 2-5. COP and Security Register (COPR)

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the EPROM/OTPROM difficult for unauthorized users.

3.6 Condition Code Register

The condition code register is an 8-bit register whose three most significant bits are permanently fixed at 111 as shown in Figure 3-6. The condition code register contains the interrupt mask and four flags that indicate the results of the instruction just executed. The following paragraphs describe the functions of the condition code register.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	1	1	1	H	I	N	C	Z
Write:								
Reset:	1	1	1	U	1	U	U	U

U = Unaffected

Figure 3-6. Condition Code Register (CCR)

Half-Carry Flag (H)

The CPU sets the half-carry flag when a carry occurs between bits 3 and 4 of the accumulator during an ADD or ADC operation. The half-carry flag is required for binary coded decimal (BCD) arithmetic operations. Reset has no effect on the half-carry flag.

Interrupt Mask (I)

Setting the interrupt mask disables interrupts. If an interrupt request occurs while the interrupt mask is a logic 0, the CPU saves the CPU registers on the stack, sets the interrupt mask, and then fetches the interrupt vector. If an interrupt request occurs while the interrupt mask is set, the interrupt request is latched. The CPU processes the latched interrupt as soon as the interrupt mask is cleared again. A return-from-interrupt (RTI) instruction pulls the CPU registers from the stack, restoring the interrupt mask to its cleared state. After a reset, the interrupt mask is set and can be cleared only by a CLI instruction.

Negative Flag (N)

The CPU sets the negative flag when an arithmetic operation, logical operation, or data manipulation produces a negative result. Reset has no affect on the negative flag.

Zero Flag (Z)

The CPU sets the zero flag when an arithmetic operation, logical operation, or data manipulation produces a result of $00. Reset has no affect on the zero flag.

Carry/Borrow Flag (C)

The CPU sets the carry/borrow flag when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some logical operations and data manipulation instructions also clear or set the carry/borrow flag. Reset has no effect on the carry/borrow flag.

3.7 Arithmetic/Logic Unit (ALU)

The ALU performs the arithmetic and logical operations defined by the instruction set. The binary arithmetic circuits decode instructions and set up the ALU for the selected operation. Most binary arithmetic is based on the addition algorithm, carrying out subtraction as negative addition. Multiplication is not performed as a discrete operation but as a chain of addition and shift operations within the ALU. The multiply instruction (MUL) requires 11 internal clock cycles to complete this chain of operations.

4.7 Programmable Timer Interrupts

The 16-bit programmable timer can generate an interrupt whenever the following events occur:

- Input capture
- Output compare
- Timer counter overflow

Setting the I bit in the condition code register disables timer interrupts. The controls for these interrupts are in the timer control register (TCR) located at $0012 and in the status bits in the timer status register (TSR) located at $0013.

4.7.1 Input Capture Interrupt

An input capture interrupt occurs if the input capture flag (ICF) becomes set while the input capture interrupt enable bit (ICIE) is also set. The ICF flag bit is in the TSR, and the ICIE enable bit is located in the TCR. The ICF flag bit is cleared by a read of the TSR with the ICF flag bit set, and then followed by a read of the LSB of the input capture register (ICRL) or by reset. The ICIE enable bit is unaffected by reset.

4.7.2 Output Compare Interrupt

An output compare interrupt occurs if the output compare flag (OCF) becomes set while the output compare interrupt enable bit (OCIE) is also set. The OCF flag bit is in the TSR and the OCIE enable bit is in the TCR. The OCF flag bit is cleared by a read of the TSR with the OCF flag bit set, and then followed by an access to the LSB of the output compare register (OCRL) or by reset. The OCIE enable bit is unaffected by reset.

4.7.3 Timer Overflow Interrupt

A timer overflow interrupt occurs if the timer overflow flag (TOF) becomes set while the timer overflow interrupt enable bit (TOIE) is also set. The TOF flag bit is in the TSR and the TOIE enable bit is in the TCR. The TOF flag bit is cleared by a read of the TSR with the TOF flag bit set, and then followed by an access to the LSB of the timer registers (TMRL) or by reset. The TOIE enable bit is unaffected by reset.

4.8 Serial Interrupts

The simple serial interface can generate the following interrupts:

- Receive sequence complete
- Transmit sequence complete

Setting the I bit in the condition code register disables serial interrupts. The controls for these interrupts are in the serial control register (SCR) located at $000A and in the status bits in the serial status register (SSR) located at $000B.

A transfer complete interrupt occurs if the serial interrupt flag (SPIF) becomes set while the serial interrupt enable bit (SPIE) is also set. The SPIF flag bit is in the serial status register (SSR) located at $000B, and the SPIE enable bit is located in the serial control register (SCR) located at $000A. The SPIF flag bit is cleared by a read of the SSR with the SPIF flag bit set, and then followed by a read or write to the serial data register (SDR) located at $000C. The SPIF flag bit can also be reset by writing a one to the SPIR bit in the SCR.

5.4.2 Computer Operating Properly (COP) Reset

A timeout of the COP watchdog generates a COP reset. The COP watchdog is part of a software error detection system and must be cleared periodically to start a new timeout period. To clear the COP watchdog and prevent a COP reset, write a logic 0 to the COPC bit of the COPR register at location $1FF0. The COPC bit, shown in Figure 5-2, is a write-only bit.

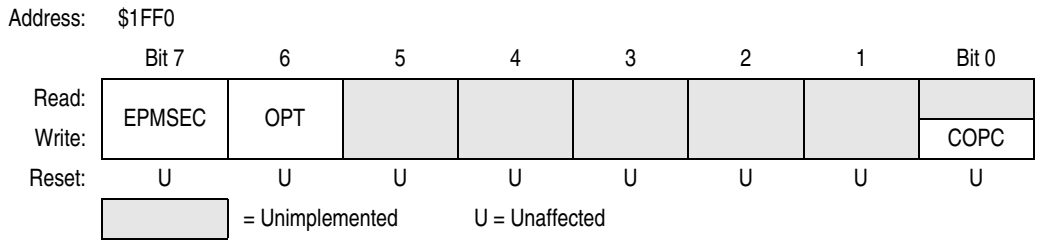


Figure 5-2. COP and Security Register (COPR)

EPMSEC — EPROM Security[1] Bit

The EPMSEC bit is an EPROM, write-only security bit to protect the contents of the user EPROM code stored in locations $0700–$1FFF.

OPT — Optional Features Bit

The OPT bit enables two additional features: direct drive by comparator 1 output to PB4 and voltage offset capability to sample capacitor in analog subsystem.

1 = Optional features enabled
0 = Optional features disabled

NOTE

See 8.7.1 Voltage Comparator 1 and 8.10 Sample and Hold for further descriptions of the OPT bit.

COPC — COP Clear Bit

COPC is a write-only bit. Periodically writing a logic 0 to COPC prevents the COP watchdog from resetting the MCU. Reset clears the COPC bit.

1 = No effect on COP watchdog timer
0 = Reset COP watchdog timer

The COP watchdog reset will assert the pulldown device to pull the $\overline{\text{RESET}}$ pin low for three to four cycles of the internal bus.

The COP watchdog reset function can be enabled or disabled by programming the COPEN bit in the MOR.

5.4.3 Low-Voltage Reset (LVR)

The LVR activates the RST reset signal to reset the device when the voltage on the V_{DD} pin falls below the LVR trip voltage. The LVR will assert the pulldown device to pull the $\overline{\text{RESET}}$ pin low for three to four cycles of the internal bus.

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the EPROM/OTPROM difficult for unauthorized users.

PB0-PB7 — Port B Data Bits

These read/write bits are software programmable. Data direction of each bit is under the control of the corresponding bit in data direction register B. Reset has no effect on port B data.

7.3.2 Data Direction Register B

The contents of the port B data direction register (DDRB) determine whether each port B pin is an input or an output. Writing a logic 1 to a DDRB bit enables the output buffer for the associated port B pin. A DDRB bit set to a logic 1 also disables the pulldown device for that pin. Writing a logic 0 to a DDRB bit disables the output buffer for the associated port B pin. A reset initializes all DDRB bits to logic 0s, configuring all port B pins as inputs.

Address: $0005

	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
Reset:	0	0	0	0	0	0	0	0

Figure 7-6. Data Direction Register B (DDRB)

DDRB7–DDRB0 — Port B Data Direction Bits

These read/write bits control port B data direction. Reset clears the bits DDRB7–DDRB0.

1 = Corresponding port B pin configured as output and pulldown device disabled
0 = Corresponding port B pin configured as input

7.3.3 Pulldown Register B

All port B pins can have software programmable pulldown devices enabled or disabled globally by the SWPDI bit in the MOR. These pulldown devices are individually controlled by the write-only pulldown register B (PDRB) shown in Figure 7-7. Clearing the PDIB7–PDIB0 bits in the PDRB turns on the pulldown devices if the port B pin is an input. Reading the PDRB returns undefined results since it is a write-only register. Reset clears the PDIB7–PDIB0 bits, which turns on all the port B pulldown devices.

Address: $0011

	Bit 7	6	5	4	3	2	1	Bit 0
Read:								
Write:	PDIB7	PDIB6	PDIB5	PDIB4	PDIB3	PDIB2	PDIB1	DIB0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 7-7. Pulldown Register B (PDRB)

PDIB7–PDIB0 — Port B Pulldown Inhibit Bits

Writing to these write-only bits controls the port B pulldown devices. Reading these pulldown register B bits returns undefined data. Reset clears bits PDIB7–PDIB0.

1 = Corresponding port B pin pulldown device turned off
0 = Corresponding port B pin pulldown device turned on if pin has been programmed by the DDRB to be an input

Therefore, input voltages cannot be resolved if they are less than the sum of the AV_{SS} offset and the comparator offset, because they will always yield a low output from the comparator.

Table 8-2. Channel Select Bus Combinations

Analog Multiplex Register					Channel Select Bus Connected to:					
VREF	MUX4	MUX3	MUX2	MUX1	V_{DD}	PB4/AN4/ TCMP	PB3/AN3/ TCAP	PB2/AN2	PB1/AN1	V_{SS}
0	0	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	On
X[1]	0	0	0	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	On	Hi-Z
X[1]	0	0	1	0	Hi-Z	Hi-Z	Hi-Z	On	Hi-Z	Hi-Z
X[1]	0	0	1	1	Hi-Z	Hi-Z	Hi-Z	On	On	Hi-Z
X[1]	0	1	0	0	Hi-Z	Hi-Z	On	Hi-Z	Hi-Z	Hi-Z
X[1]	0	1	0	1	Hi-Z	Hi-Z	On	Hi-Z	On	Hi-Z
X[1]	0	1	1	0	Hi-Z	Hi-Z	On	On	Hi-Z	Hi-Z
X[1]	0	1	1	1	Hi-Z	Hi-Z	On	On	On	Hi-Z
X[1]	1	0	0	0	Hi-Z	On	Hi-Z	Hi-Z	Hi-Z	Hi-Z
X[1]	1	0	0	1	Hi-Z	On	Hi-Z	Hi-Z	On	Hi-Z
X[1]	1	0	1	0	Hi-Z	On	Hi-Z	On	Hi-Z	Hi-Z
X[1]	1	0	1	1	Hi-Z	On	Hi-Z	On	On	Hi-Z
X[1]	1	1	0	0	Hi-Z	On	On	Hi-Z	Hi-Z	Hi-Z
X[1]	1	1	0	1	Hi-Z	On	On	Hi-Z	On	Hi-Z
X[1]	1	1	1	0	Hi-Z	On	On	On	Hi-Z	Hi-Z
X[1]	1	1	1	1	Hi Z	On	On	On	On	Hi Z

1. Don/t care

8.3 Analog Control Register

The analog control register (ACR) controls the power-up, interrupt, and flag operation. The analog subsystem draws current while it is operating. The resulting power consumption can be reduced by powering down the analog subsystem when not in use (refer to 15.5 Supply Current Characteristics (V_{DD} = 4.5 to 5.5 Vdc)). This can be done by clearing three enable bits (ISEN, CP1EN, and CP2EN) in the ACR at $001D. Since these bits are cleared following a reset, the voltage comparators and the charge current source will be powered down following a reset of the device.

The control bits in the ACR are shown in Figure 8-5. All the bits in this register are cleared by a reset of the device.

ICEN

This is a read/write bit that enables a voltage comparison to trigger the input capture register of the programmable timer when the CPF2 flag bit is set. Therefore, an A/D conversion could be started by receiving an OCF or TOF from the programmable timer and then terminated when the voltage on the external ramping capacitor reaches the level of the unknown voltage. The time of termination will be stored in the 16-bit buffer located at $0014 and $0015. This bit is automatically set whenever mode 2 or 3 is selected by setting the ATD2 control bit. This bit is cleared by a reset of the device.

1 = Connects the CPF2 flag bit to the timer input capture register
0 = Connects the PB3/AN3 pin to the timer input capture register

NOTE

For the input capture to occur when the output of comparator 2 goes high, the IEDG bit in the TCR must also be set.

When the ICEN bit is set, the input capture function of the programmable timer is not connected to the PB3/AN3/TCAP pin but is driven by the CPF2 output flag from comparator 2. To return to capturing times from external events, the ICEN bit must first be cleared before the timed event occurs.

CPIE

This is a read/write bit that enables an analog interrupt when either of the CPF1 or CPF2 flag bits is set to a logic 1. This bit is cleared by a reset of the device.

1 = Enables analog interrupts when comparator flag bits are set
0 = Disables analog interrupts when comparator flag bits are set

NOTE

If both the ICEN and CPIE bits are set, they will both generate an interrupt by different paths. One will be the programmable timer interrupt due to the input capture and the other will be the analog interrupt due to the output of comparator 2 going high. In this case, the input capture interrupt will be entered first due to its higher priority. The analog interrupt will then need to be serviced even if the comparator 2 output has been reset or the input capture flag (ICF) has been cleared.

CP2EN

The CP2EN enable bit controls power to voltage comparator 2 in the analog subsystem. Powering down a comparator will drop the supply current. This bit is cleared by a reset of the device.

1 = Writing a logic 1 powers up voltage comparator 2.
0 = Writing a logic 0 powers down voltage comparator 2.

NOTE

Voltage comparators power up slower than digital logic and their outputs may go through indeterminate states which might set their respective flags (CPF1, CPF2). It is therefore recommended to power up the charge current source first (ISEN), then to power up any comparators, and finally clear the flag bits by writing a logic 1 to the respective CPFR1 or CPFR2 bits in the ACR.

CP1EN

The CP1EN enable bit will power down the voltage comparator 1 in the analog subsystem. Powering down a comparator will drop the supply current. This bit is cleared by a reset of the device.

1 = Writing a logic 1 powers up voltage comparator 1
0 = Writing a logic 0 powers down voltage comparator 1

CPFR2

Writing a logic 1 to this write-only flag clears the CPF2 flag in the ASR. Writing a logic 0 to this bit has no effect. Reading the CPFR2 bit will return a logic 0. By default, this bit looks cleared following a reset of the device.

1 = Clears the CPF2 flag bit
0 = No effect

CPFR1

Writing a logic 1 to this write-only flag clears the CPF1 flag in the ASR. Writing a logic 0 to this bit has no effect. Reading the CPFR1 bit will return a logic 0. By default, this bit looks cleared after a reset of the device.

1 = Clears the CPF1 flag bit
0 = No effect

NOTE

The CPFR1 and CPFR2 bits should be written with logic 1s following a power-up of either comparator. This will clear out any latched CPF1 or CPF2 flag bits which might have been set during the slower power-up sequence of the analog circuitry.

If both inputs to a comparator are above the maximum common-mode input voltage (V_{DD} –1.5 V), the output of the comparator is indeterminate and may set the comparator flag. Applying a reset to the device may only temporarily clear this flag as long as both inputs of a comparator remain above the maximum common-mode input voltages.

VOFF

This read-write bit controls the addition of an offset voltage to the bottom of the sample capacitor. It is not active unless the OPT bit in the COPR at location $1FF0 is set. Any reads of the VOFF bit location return a logic 0 if the OPT bit is clear. During the time that the sample capacitor is connected to an input (either HOLD or DHOLD set), the bottom of the sample capacitor is connected to V_{SS}. The VOFF bit is cleared by a reset of the device. For more information, see 8.10 Sample and Hold.

1 = Enables approximately 100 mV offset to be added to the sample voltage when both the HOLD and DHOLD control bits are cleared
0 = Connects the bottom of the sample capacitor to V_{SS}

COE1

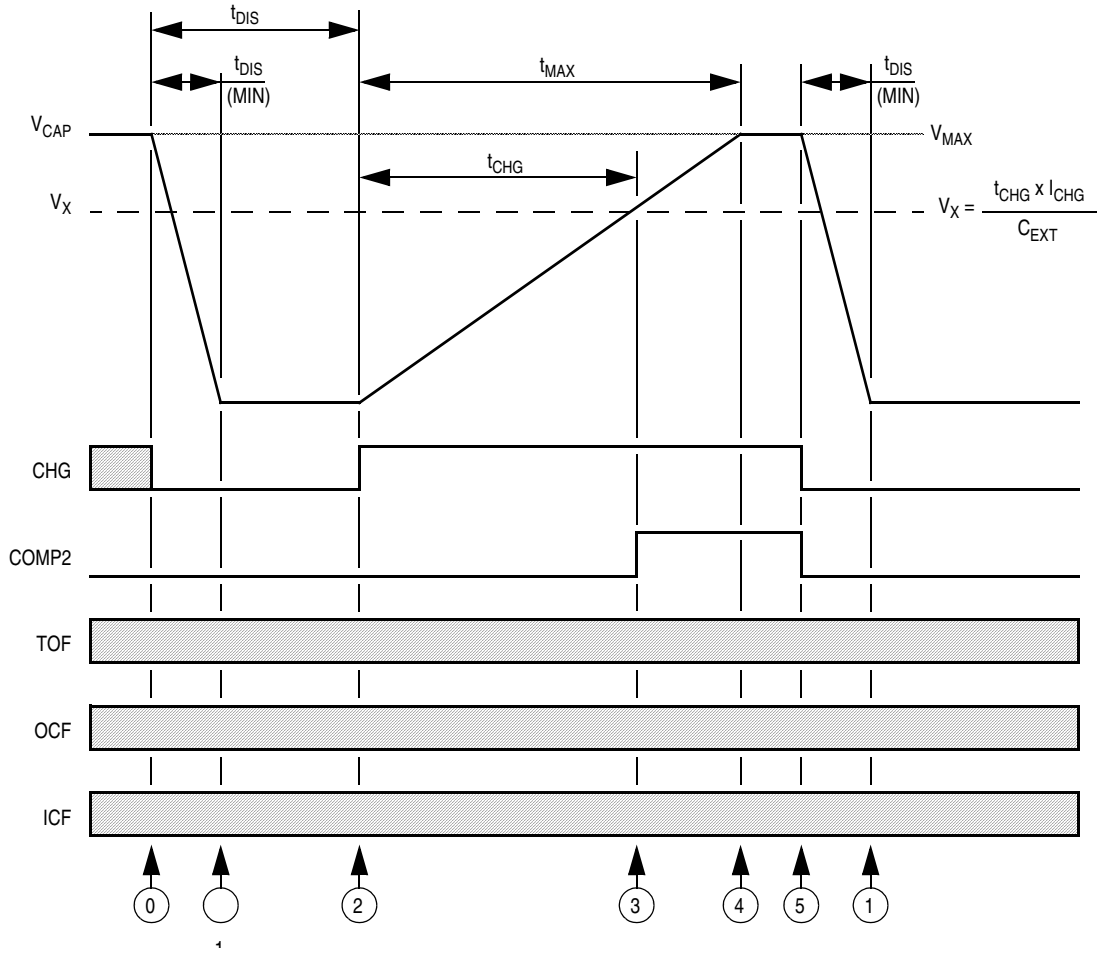
This read-write bit controls the output of comparator 1 to the PB4 pin. It is not active unless the OPT bit in the COPR at location $1FF0 is set. Any reads of the COE1 bit location return a logic 0 if the OPT bit is clear. The COE1 bit is cleared by a reset of the device.

1 = Enables the output of comparator 1 to be ORed with the PB4 data bit and OLVL bit, if the DDRB4 bit is also set
0 = Disables the output of comparator 1 from affecting the PB4 pin

CMP2

This read-only bit shows the state of comparator 2 during the time that the bit is read. This bit is therefore the current state of the comparator without any latched history. The CMP2 bit will be high if the voltage on the PB0/AN0 pin is greater than the voltage on the PB1/AN1 pin, regardless of the state of the INV bit in the AMUX register. Since a reset disables comparator 2, this bit returns a logic 0 following a reset of the device.

1 = The voltage on the positive input on comparator 2 is higher than the voltage on the negative input of comparator 2.
0 = The voltage on the positive input on comparator 2 is lower than the voltage on the negative input of comparator 2.



Point	Action	Software/Hardware Action	Dependent Variable(s)
0	Begin initial discharge and select mode 0 by clearing the CHG, ATD2, and ATD1 control bits in the ACR.	Software write	Software
1	V_{CAP} falls to V_{SS}.	Wait out minimum t_{DIS} time.	V_{MAX}, I_{DIS}, C_{EXT}
2	Stop discharge and begin charge by setting CHG control bit in ACR.	Software write	Software
3	V_{CAP} rises to V_X and comparator 2 output trips, setting CPF2 and CMP2.	Wait out t_{CHG} time.	V_X, I_{CHG}, C_{EXT}
4	V_{CAP} reaches V_{MAX}.	None	V_{MAX}, I_{CHG}, C_{EXT}
5	Begin next discharge by clearing the CHG control bit in the ACR. Reset CPF2 by writing a 1 to CPFR2.	Software write	Software

Figure 8-8. A/D Conversion — Full Manual Control (Mode 0)

Chapter 12
Personality EPROM (PEPROM)

12.1 Introduction

This section describes how to program the 64-bit personality erasable programmable read-only memory (PEPROM). Figure 12-1 shows the structure of the PEPROM subsystem.

NOTE

In packages with no quartz window, the PEPROM functions as one-time programmable ROM (OTPROM).

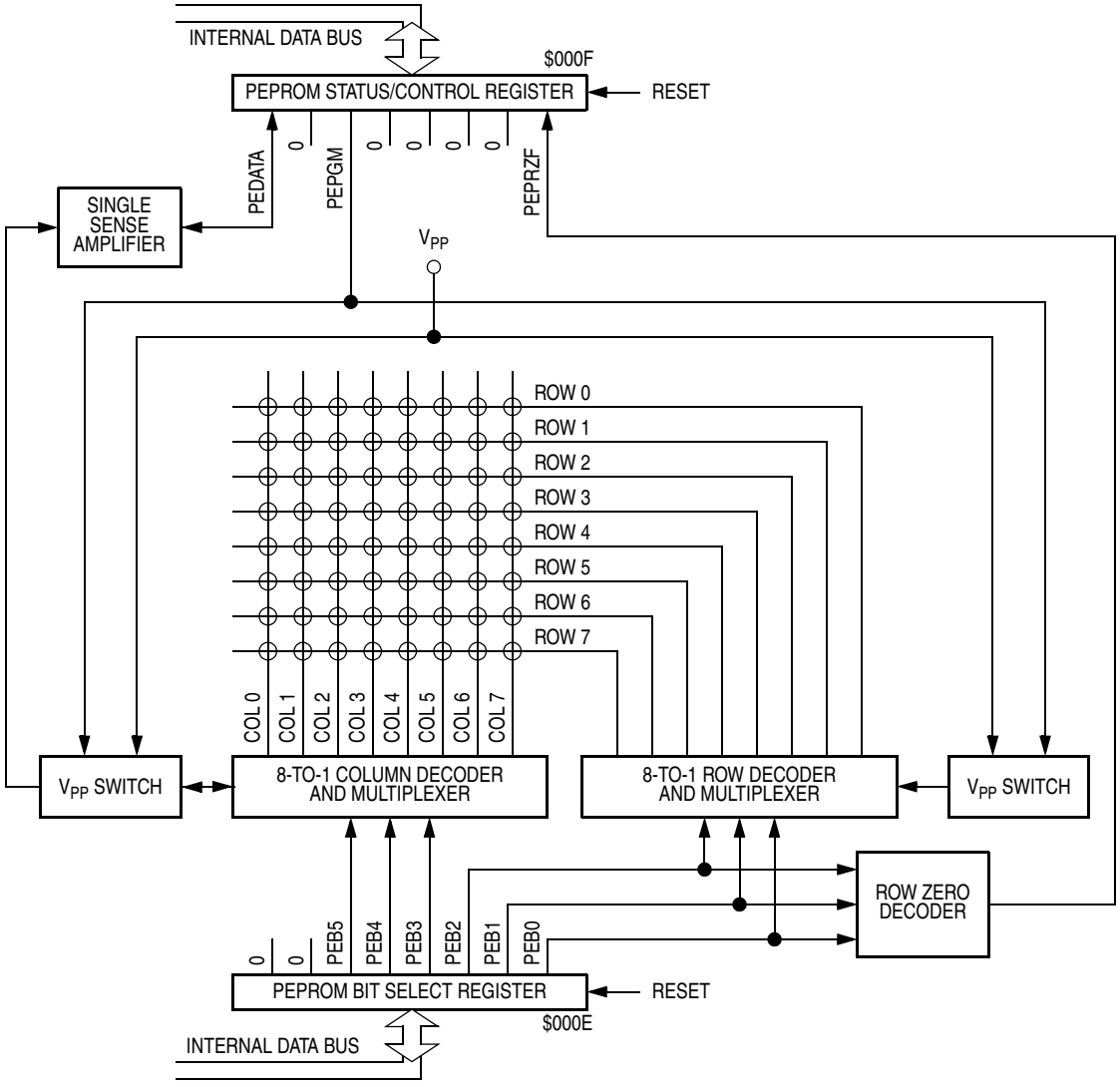


Figure 12-1. Personality EPROM Block Diagram

12.4 PEPROM Reading

This sequence shows how to read the PEPROM:

1. Select a bit by writing to the PEBSR.
2. Read the PEDATA bit in the PESCR.
3. Store the PEDATA bit in RAM or in a register.
4. Select another bit by changing the PEBSR.
5. Continue reading and storing the PEDATA bits until the required personality EPROM data is retrieved and stored.

Reading the PEPROM is easiest when each PEPROM column contains one byte. Selecting a row 0 bit selects the first bit, and incrementing the PEPROM bit select register (PEBSR) selects the next bit in row 1 from the same column. Incrementing PEBSR seven more times selects the remaining bits of the column and ends up selecting the bit in row 0 of the next column, thereby setting the row 0 flag, PEPRZF.

NOTE

A PEPROM byte that has been read can be transferred to the personality EPROM bit select register (PEBSR) as a temporary storage location such that subsequent reads of the PEBSR quickly yield that PEPROM byte.

12.5 PEPROM Erasing

MCUs with windowed packages permit PEPROM erasing with ultraviolet light. Erase the PEPROM by exposing it to 15 Ws/cm^2 of ultraviolet light with a wavelength of 2537 angstroms. Position the ultraviolet light source 1 inch from the window. Do not use a shortwave filter. The erased state of a PEPROM bit is a logic 0.

14.3 Instruction Types

The MCU instructions fall into the following five categories:

- Register/memory instructions
- Read-modify-write instructions
- Jump/branch instructions
- Bit manipulation instructions
- Control instructions

14.3.1 Register/Memory Instructions

These instructions operate on CPU registers and memory locations. Most of them use two operands. One operand is in either the accumulator or the index register. The CPU finds the other operand in memory.

Table 14-1. Register/Memory Instructions

Instruction	Mnemonic
Add Memory Byte and Carry Bit to Accumulator	ADC
Add Memory Byte to Accumulator	ADD
AND Memory Byte with Accumulator	AND
Bit Test Accumulator	BIT
Compare Accumulator	CMP
Compare Index Register with Memory Byte	CPX
EXCLUSIVE OR Accumulator with Memory Byte	EOR
Load Accumulator with Memory Byte	LDA
Load Index Register with Memory Byte	LDX
Multiply	MUL
OR Accumulator with Memory Byte	ORA
Subtract Memory Byte and Carry Bit from Accumulator	SBC
Store Accumulator in Memory	STA
Store Index Register in Memory	STX
Subtract Memory Byte from Accumulator	SUB

14.3.3 Jump/Branch Instructions

Jump instructions allow the CPU to interrupt the normal sequence of the program counter. The unconditional jump instruction (JMP) and the jump-to-subroutine instruction (JSR) have no register operand. Branch instructions allow the CPU to interrupt the normal sequence of the program counter when a test condition is met. If the test condition is not met, the branch is not performed.

The BRCLR and BRSET instructions cause a branch based on the state of any readable bit in the first 256 memory locations. These 3-byte instructions use a combination of direct addressing and relative addressing. The direct address of the byte to be tested is in the byte following the opcode. The third byte is the signed offset byte. The CPU finds the effective branch destination by adding the third byte to the program counter if the specified bit tests true. The bit to be tested and its condition (set or clear) is part of the opcode. The span of branching is from –128 to +127 from the address of the next location after the branch instruction. The CPU also transfers the tested bit to the carry/borrow bit of the condition code register.

Table 14-3. Jump and Branch Instructions

Instruction	Mnemonic
Branch if Carry Bit Clear	BCC
Branch if Carry Bit Set	BCS
Branch if Equal	BEQ
Branch if Half-Carry Bit Clear	BHCC
Branch if Half-Carry Bit Set	BHCS
Branch if Higher	BHI
Branch if Higher or Same	BHS
Branch if $\overline{IRQ}/V_{PP}$ Pin High	BIH
Branch if $\overline{IRQ}/V_{PP}$ Pin Low	BIL
Branch if Lower	BLO
Branch if Lower or Same	BLS
Branch if Interrupt Mask Clear	BMC
Branch if Minus	BMI
Branch if Interrupt Mask Set	BMS
Branch if Not Equal	BNE
Branch if Plus	BPL
Branch Always	BRA
Branch if Bit Clear	BRCLR
Branch Never	BRN
Branch if Bit Set	BRSET
Branch to Subroutine	BSR
Unconditional Jump	JMP
Jump to Subroutine	JSR

15.7 DC Electrical Characteristics (5.0 Vdc)

Characteristic[1], [2]	Symbol	Min	Typ[3]	Max	Unit
Output voltage I_{Load} = 10.0 µA I_{Load} = –10.0 µA	V_{OL} V_{OH}	— V_{DD} –0.1	— —	0.1 —	V
Output high voltage (I_{Load} = –0.8 mA) PB0–PB7 (I_{Load} = –4.0 mA) PA0–PA5, PB4, PC0–PC7[4]	V_{OH}	V_{DD} –0.8 V_{DD} –0.8	— —	— —	V
Output low voltage (I_{Load} = 1.6 mA) PB0–PB7, $\overline{RESET}$ (I_{Load} = 10 mA) PA0–PA5, PB4, PC0–PC7[4] (I_{Load} = 15 mA) PA0–PA5, PB4, PC0–PC7[4]	V_{OL}	— — —	— — —	0.4 0.4 1.5	V
High source current Total for all (6) PA0–PA5 pins and PB4 Total for all (8) PC0–PC7[4] pins	I_{OH}	— —	— —	20 30	mA
High sink current Total for all (6) PA0–PA5 pins and PB4 Total for all (8) PC0–PC7[4] pins	I_{OL}	— —	— —	40 60	mA
Input high voltage PA0–PA5, PB0–PB7, PC0–PC7[4], $\overline{RESET}$, OSC1, $\overline{IRQ}$/V_{PP}	V_{IH}	0.7 x V_{DD}	—	V_{DD}	V
Input low voltage PA0–PA5, PB0–PB7, PC0–PC7[4], $\overline{RESET}$, OSC1, $\overline{IRQ}$/V_{PP}	V_{IL}	V_{SS}	—	0.3 x V_{DD}	V
Input current OSC1, $\overline{IRQ}$/V_{PP}	I_{In}	–1	—	1	µA
Input current $\overline{RESET}$ (pullup, source) $\overline{RESET}$ (pulldown, sink)	I_{In}	10 –6	— —	— —	µA mA
I/O ports hi-Z leakage current (pulldowns off) PA0–PA6, PB0–PB7, PC0–PC7[4]	I_{OZ}	–2	—	2	µA
Input pulldown current PA0–PA5, PB0–PB7, PC0–PC7[4] (V_{In} ; V_{IH} = 0.7 x V_{DD}) PA0–PA5, PB0–PB7, PC0–PC7[4] (V_{In} ; V_{IL} = 0.3 x V_{DD})	I_{IL}	40 25	100 65	280 190	µA

1. +4.5 ≤ V_{DD} ≤ +5.5 V, V_{SS} = 0 V, $T_L \le T_A \le T_H$, unless otherwise noted
2. All values shown reflect average measurements.
3. Typical values at midpoint of voltage range, 25°C only.
4. PC0–PC7 parameters only apply to MC68HC705JP7.

15.13 PEPROM and EPROM Programming Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
PEPROM programming voltage ($\overline{IRQ}/V_{PP}$)	V_{PP}	16.0	16.5	17.0	V
PEPROM programming voltage ($\overline{IRQ}/V_{PP}$)	I_{PP}	—	3.0	5.0	mA
PEPROM programming time per bit	t_{EPGM}	4.0	—	—	ms
EPROM/MOR programming voltage ($\overline{IRQ}/V_{PP}$)	V_{PP}	16.0	16.5	17.0	V
EPROM/MOR programming current ($\overline{IRQ}/V_{PP}$)	I_{PP}	—	3.0	5.0	mA
EPROM programming time per byte	t_{EPGM}	4.0	—	—	ms
MOR programming time	t_{MPGM}	10.0	—	—	ms

1. $+4.5 \le V_{DD} \le +5.5$ V, $V_{SS} = 0$ V, $T_L \le T_A \le T_H$, unless otherwise noted

NOTE

To program the EPROM/OTPROM, MOR, or EPMSEC bits, the voltage on V_{DD} must be greater than 4.5 volts.