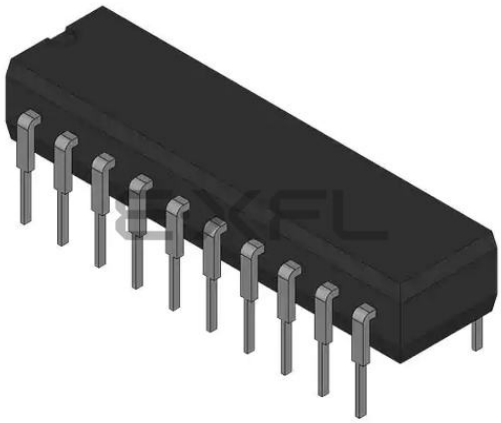


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SIO
Peripherals	POR, Temp Sensor, WDT
Number of I/O	14
Program Memory Size	6KB (6K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	224 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-DIP
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mchc705jj7cpe

MC68HC705JJ7 MC68HRC705SJ7
MC68HC705SJ7 MC68HC705JP7
MC68HRC705JJ7 MC68HC705SP7

Advance Information Data Sheet

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://www.freescale.com/

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
August, 2001	4.0	General reformat to bring document up to current publication standards	All
		References to MC68HRC705SJ7 and MC68HRC705SP7 removed throughout	All
		Figure 7-9. PB4/AN4/TCMP/CMP1 Pin I/O Circuit — Change label of register $1FF0 from mask option register to COP register	94
		Table 7-2. Port B Pin Functions — PB0–PB4 — Change heading under Comparator 1 from OPT in MOR to OPT in COPR	96
		12.4 PEPROM Programming — Contact information updated	179
		Figure 13-3. EPROM Security in COP and Security Register (COPR) — Figure title change	188
		13.4 EPROM Programming — Contact information updated and corrected reference to COP register from COP to COPR	189
		15.15 SIOP Timing (VDD = 5.0 Vdc) — Value change for clock (SCK) low time	225
		15.16 SIOP Timing (VDD = 3.0 Vdc) — Value change for clock (SCK) low time	226
		Section 15. Electrical Specifications — Added Figure 15-1 through Figure 15-10 and Figure 15-12	213, 214, 219, 223, and 227
September, 2005	4.1	Updated to meet Freescale identity guidelines.	Throughout

Addr.	Register		Bit 7	6	5	4	3	2	1	Bit 0
$0018	Programmable Timer Register High (TMRH) See page 107.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$0019	Programmable Timer Register Low (TMRL) See page 107.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	1	1	1	1	1	1	0	0
$001A	Alternate Counter Register High (ACRH) See page 108.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$001B	Alternate Counter Register Low (ACRL) See page 108.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	1	1	1	1	1	1	0	0
$001C	EPROM Programming Register (EPROG) See page 119.	Read:	0	0	0	0	0	ELAT	MPGM	EPGM
		Write:		R	R	R	R			
		Reset:	0	0	0	0	0	0	0	0
$001D	Analog Counter Register (ACR) See page 77.	Read:	CHG	ATD2	ATD1	ICEN	CPIE	CP2EN	CP1EN	ISEN
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$001E	Analog Status Register (ASR) See page 77.	Read:	CPF2	CPF1	0	0	COE1	VOFF	CMP2	CMP1
		Write:			CPFR2	CPFR1				R
		Reset:	0	0	0	0	0	0	0	0
$001F	Reserved		R	R	R	R	R	R	R	R
↓										
$1FEF	Reserved		R	R	R	R	R	R	R	R
$1FF0	COP and Security Register (COPR) See pages 27, 92, 104, and 122.	Read:		OPT						
		Write:	EPMSEC							COPC
		Reset:	Unaffected by reset							

= Unimplemented R = Reserved U = Unaffected

1. Features related to port C are only available on the 28-pin MC68HC705JP7 devices.

Figure 2-3. Register Summary (Sheet 3 of 3)

4.3 Interrupt Processing

To begin servicing an interrupt, the CPU does these actions:

- Stores the CPU registers on the stack in the order shown in Figure 4-1
- Sets the I bit in the condition code register to prevent further interrupts
- Loads the program counter with the contents of the appropriate interrupt vector locations as shown in Table 4-1

The return-from-interrupt (RTI) instruction causes the CPU to recover its register contents from the stack as shown in Figure 4-1. The sequence of events caused by an interrupt is shown in the flowchart in Figure 4-2.

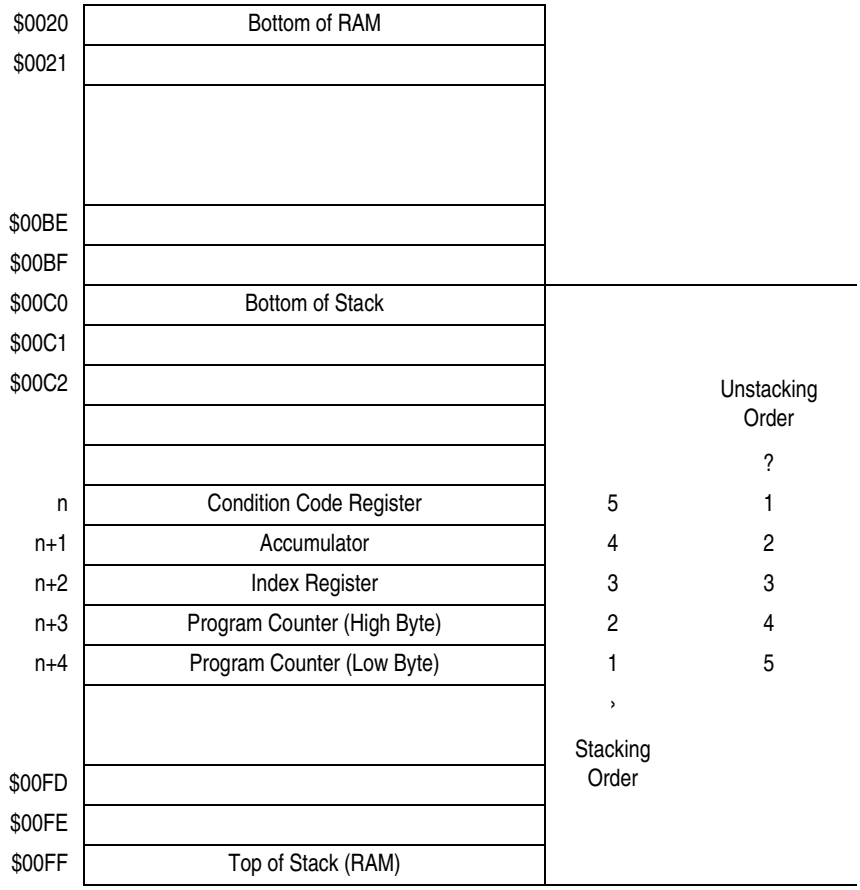


Figure 4-1. Interrupt Stacking Order

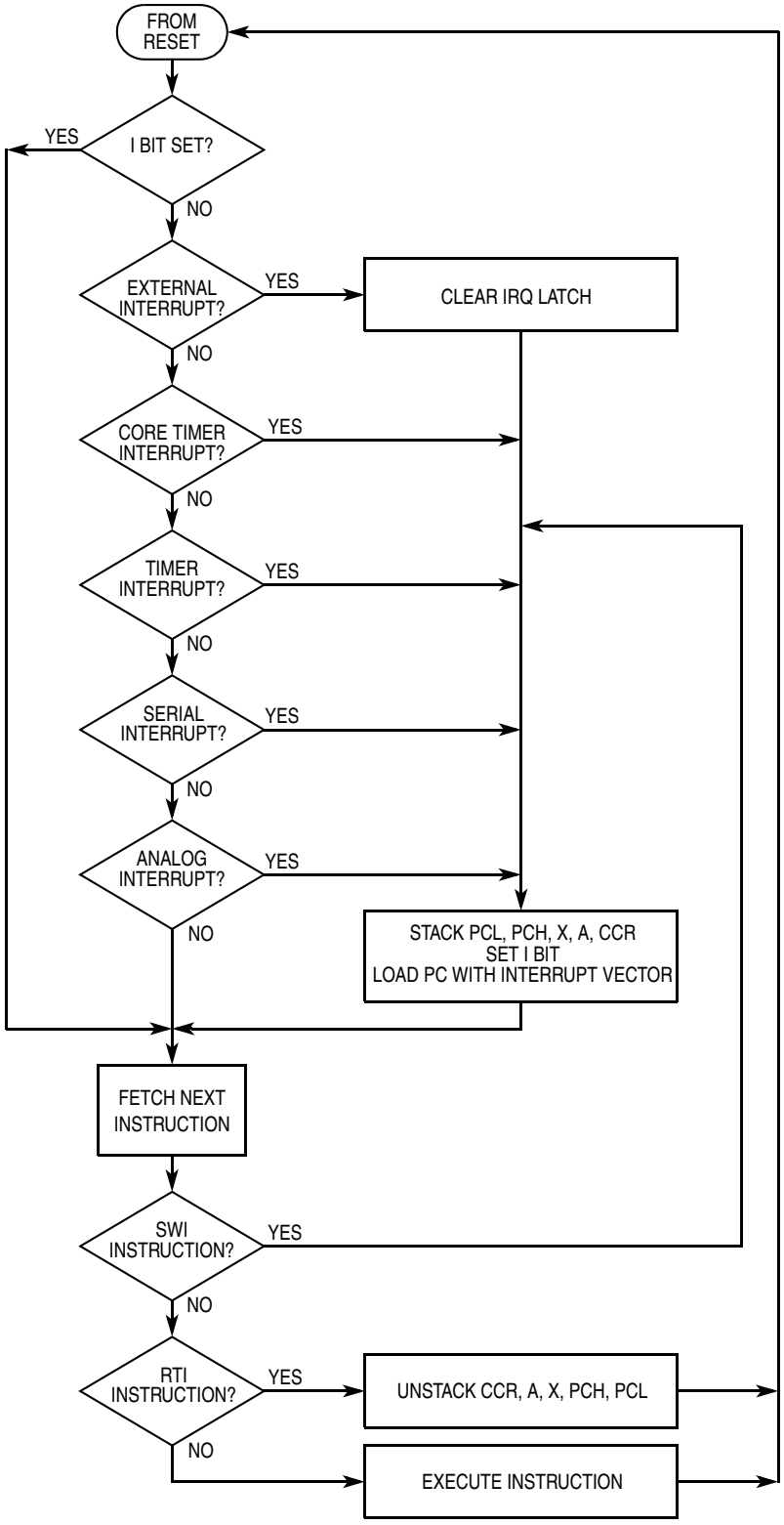


Figure 4-2. Interrupt Flowchart

Therefore, the lowest power is consumed when OM1 is cleared. The state with both OM1 and OM2 set is provided so that the EPO can be started and allowed to stabilize while the LPO still clocks the MCU. The reset state is for OM1 to be cleared and OM2 to be set, which selects the LPO and disables the EPO.

IRQF — External Interrupt Request Flag

The IRQ flag is a clearable, read-only bit that is set when an external interrupt request is pending. Writing to the IRQF bit has no effect. Reset clears the IRQF bit.

1 = Interrupt request pending
0 = No interrupt request pending

The following conditions set the IRQ flag:

- An external interrupt signal on the $\overline{IRQ}/V_{PP}$ pin
- An external interrupt signal on pin PA0, PA1, PA2, or PA3
  when the PA0–PA3 pins are enabled by the PIRQ bit in the MOR to serve as external interrupt sources.

The following conditions clear the IRQ flag:

- When the CPU fetches the interrupt vector
- When a logic 1 is written to the IRQR bit

IRQR — Interrupt Request Reset Bit

This write-only bit clears the IRQF flag bit and prevents redundant execution of interrupt routines. Writing a logic 1 to IRQR clears the IRQF. Writing a logic 0 to IRQR has no effect. IRQR always reads as a logic 0. Reset has no effect on IRQR.

1 = Clear IRQF flag bit
0 = No effect

4.6 Core Timer Interrupts

The core timer can generate the following interrupts:

- Timer overflow interrupt
- Real-time interrupt

Setting the I bit in the condition code register disables core timer interrupts. The controls and flags for these interrupts are in the core timer status and control register (CTSCR) located at $0008.

4.6.1 Core Timer Overflow Interrupt

An overflow interrupt request occurs if the core timer overflow flag (TOF) becomes set while the core timer overflow interrupt enable bit (TOFE) is also set. The TOF flag bit can be reset by writing a logic 1 to the CTOFR bit in the CTSCR or by a reset of the device.

4.6.2 Real-Time Interrupt

A real-time interrupt request occurs if the real-time interrupt flag (RTIF) in the CTSCR becomes set while the real-time interrupt enable bit (RTIE) is also set. The RTIF flag bit can be reset by writing a logical 1 to the RTIFR bit in the CTSCR or by a reset of the device.

7.2.2 Data Direction Register A

The contents of the port A data direction register (DDRA) determine whether each port A pin is an input or an output. Writing a logic 1 to a DDRA bit enables the output buffer for the associated port A pin. A DDRA bit set to a logic 1 also disables the pulldown device for that pin. Writing a logic 0 to a DDRA bit disables the output buffer for the associated port A pin. The upper two bits always read as logic 0s. A reset initializes all DDRA bits to logic 0s, configuring all port A pins as inputs and disabling the voltage comparators from driving PA4 or PA5.

Address: $0004

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 7-2. Data Direction Register A (DDRA)

DDRA5–DDRA0 — Port A Data Direction Bits

These read/write bits control port A data direction. Reset clears the DDRA5–DDRA0 bits.

1 = Corresponding port A pin configured as output and pulldown device disabled

0 = Corresponding port A pin configured as input

7.2.3 Pulldown Register A

All port A pins can have software programmable pulldown devices enabled or disabled globally by SWPDI bit in the MOR. These pulldown devices are controlled by the write-only pulldown register A (PDRA) shown in Figure 7-3. Clearing the PDIA5–PDIA0 bits in the PDRA turns on the pulldown devices if the port A pin is an input. Reading the PDRA returns undefined results since it is a write-only register; therefore, do not change the value in PDRA with read/modify/write instructions. On the MC68HC705JP7 the PDRA contains two pulldown control bits (PDICH and PDICL) for port C. Reset clears the PDIA5–PDIA0, PDICH, and PDICL bits, which turns on all the port A and port C pulldown devices.

Address: $0010

	Bit 7	6	5	4	3	2	1	Bit 0
Read:								
Write:	PDICH	PDICL	PDIA5	PDIA4	PDIA3	PDIA2	PDIA1	PDIA0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 7-3. Pulldown Register A (PDRA)

PDICH — Upper Port C Pulldown Inhibit Bits (MC68HC705JP7)

Writing to this write-only bit controls the port C pulldown devices on the upper four bits (PC4–PC7). Reading these pulldown register A bits returns undefined data. Reset clears bit PDICH.

1 = Upper four port C pins pulldown devices turned off

0 = Upper four port C pins pulldown devices turned on if pin has been programmed by the DDRC to be an input

7.3.4 Port B Logic

All port B pins have the general I/O port logic similar to port A; but they also share this function with inputs or outputs from other modules, which are also attached to the pin itself or override the general I/O function. PB0, PB1, PB2, and PB3 simply share their inputs with another module. PB4, PB5, PB6, and PB7 will have their operation altered by outputs or controls from other modules.

7.3.5 PB0, PBI, PB2, and PB3 Logic

The typical I/O logic shown in Figure 7-8 is used for PB0, PB1, PB2, and PB3 pins of port B. When these port B pins are programmed as an output, reading the port bit actually reads the value of the data latch and not the voltage on the pin itself. When these port B pins are programmed as an input, reading the port bit reads the voltage level on the pin. The data latch can always be written, regardless of the state of its DDRB bit. The operations of the PB0–PB3 pins are summarized in Table 7-2.

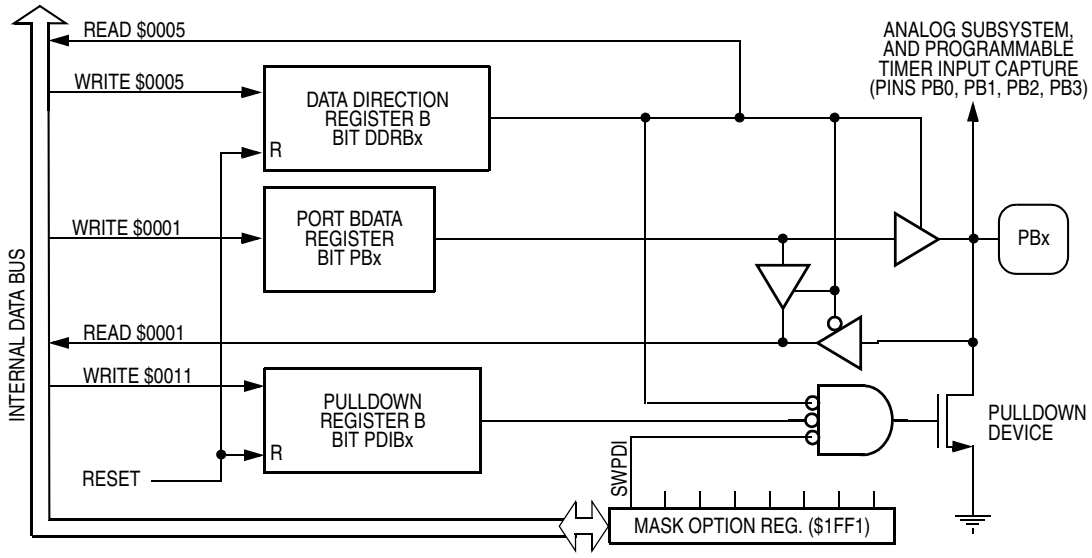
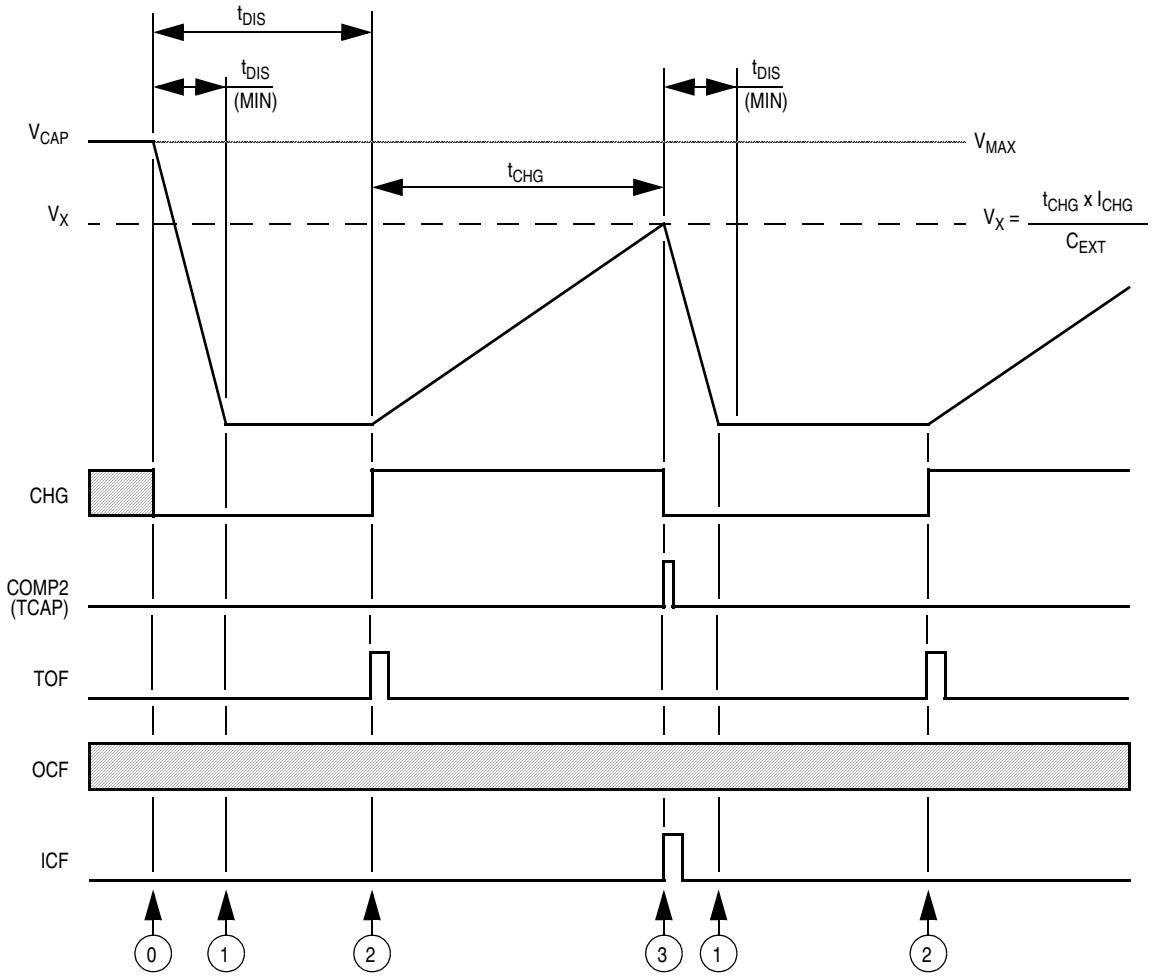


Figure 7-8. PB0–PB3 Pin I/O Circuit

The PB0–PB3 pins share their inputs with another module. When using the other attached module, these conditions must be observed:

1. If the DDRB configures the pin as an output, then the port data register can provide an output which may conflict with any external input source to the other module. The pulldown device will be disabled in this case.
2. If the DDRB configures the pin as an input, then reading the port data register will return the state of the input in terms of the digital threshold for that pin (analog inputs will default to logic states).
3. If DDRB configures the pin as an input and the pulldown device is activated for a pin, it will also load the input to the other module.
4. If interaction between the port logic and the other module is not desired, the pin should be configured as an input by clearing the appropriate DDRB bit. The input pulldown device is disabled by clearing the appropriate PDRB bit (or by disabling programmable pulldowns with the SWPDI bit in the MOR).



Point	Action	Software/Hardware Action	Dependent Variable(s)
0	Begin initial discharge and select mode 2 by clearing CHG and ATD1 and setting ATD2 in the ACR. Also set ICEN bit in ACR and IEDG bit in TCR.	Software write	Software
1	V_{CAP} falls to V_{SS}.	Wait out minimum t_{DIS} time.	V_{MAX}, I_{DIS}, C_{EXT}
2	Stop discharge and begin charge when the next TOF sets the CHG control bit in ACR.	Timer TOF sets the CHG control bit in the ACR.	Free-running timer counter overflow, f_{OSC}
3	V_{CAP} rises to V_X and comparator 2 output trips, setting CPF2 and CMP2, which causes an ICF from the timer and clears the CHG control bit in ACR. Must clear CPF2 to trap next CPF2 flag.	Wait out t_{CHG} time. Timer ICF clears the CHG control bit in the ACR.	V_X, I_{CHG}, C_{EXT}

Figure 8-10. A/D Conversion — TOF/ICF Control (Mode 2)

periodically by a program sequence. Writing a logic 0 to COPC bit in the COPR register clears the COP watchdog and prevents a COP reset.

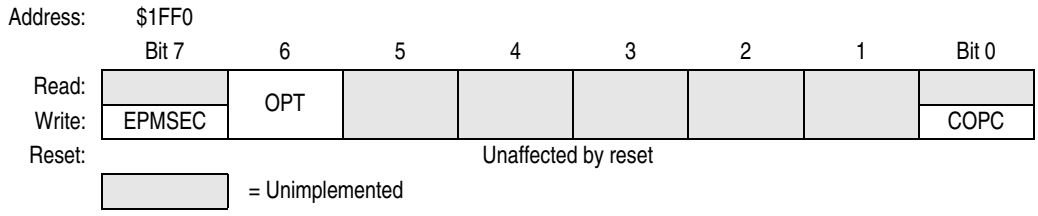


Figure 10-4. COP and Security Register (COPR)

EPMSEC — EPROM Security((1)) Bit

The EPMSEC bit is a write-only security bit to protect the contents of the user EPROM code stored in locations $0700–$1FFF.

OPT — Optional Features Bit

The OPT bit enables two additional features: direct drive by comparator outputs to port A and voltage offset capability to sample capacitor in analog subsystem.

1 = Optional features enabled
0 = Optional features disabled

COPC — COP Clear Bit

This write-only bit resets the COP watchdog. The COP watchdog is active in the run, wait, and halt modes of operation if the COP is enabled by setting the COPEN bit in the MOR. The STOP instruction disables the COP watchdog by clearing the counter and turning off its clock source.

In applications that depend on the COP watchdog, the STOP instruction can be disabled by setting the SWAIT bit in the MOR. In applications that have wait cycles longer than the COP timeout period, the COP watchdog can be disabled by clearing the COPEN bit. Table 10-2 summarizes recommended conditions for enabling and disabling the COP watchdog.

NOTE

If the voltage on the $\overline{IRQ}/V_{PP}$ pin exceeds $1.5 \times V_{DD}$, the COP watchdog turns off and remains off until the $\overline{IRQ}/V_{PP}$ pin voltage falls below $1.5 \times V_{DD}$.

Table 10-2. COP Watchdog Recommendations

Voltage on $\overline{IRQ}/V_{PP}$ Pin	SWAIT (in MOR)(1)	Wait/Halt Time	Recommended COP Watchdog Condition
Less than $1.5 \times V_{DD}$	1	Less than COP timeout period	Enabled(2)
Less than $1.5 \times V_{DD}$	1	Greater than COP timeout period	Disabled
Less than $1.5 \times V_{DD}$	0	X(3)	Disabled
More than $1.5 \times V_{DD}$	X	X(3)	Disabled

1. The SWAIT bit in the MOR converts STOP instructions to HALT instructions.
2. Reset the COP watchdog immediately before executing the WAIT/HALT instruction.
3. Don't care

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the EPROM/OTPROM difficult for unauthorized users.

IEDG — Input Capture Edge Select

The state of this read/write bit determines whether a positive or negative transition triggers a transfer of the contents of the timer register to the input capture register. This transfer can occur due to transitions on the TCAP pin or the CPF2 flag bit of voltage comparator 2. Resets have no effect on the IEDG bit.

1 = Positive edge (low-to-high transition) triggers input capture
0 = Negative edge (high-to-low transition) triggers input capture

NOTE

The IEDG bit must be set when either mode 2 or 3 of the analog subsystem is being used for A/D conversions. Otherwise, the input capture will not occur on the rising edge of the comparator 2 flag.

OLVL — Output Compare Output Level Select

The state of this read/write bit determines whether a logic 1 or a logic 0 is transferred to the TCMP pin when a successful output compare occurs. Reset clears the OLVL bit.

1 = Signal to TCMP pin goes high on output compare.
0 = Signal to TCMP pin goes low on output compare.

11.7 Timer Status Register

The timer status register (TSR) shown in Figure 11-11 contains flags for these events:

- An active signal on the TCAP pin or the CPF2 flag bit of voltage comparator 2 in the analog subsystem, transferring the contents of the timer registers to the input capture registers
- A match between the 16-bit counter and the output compare registers, transferring the OLVL bit to the PB4/AN4/TCMP pin if that pin is set as an output
- An overflow of the timer registers from $FFFF to $0000

Writing to any of the bits in the TSR has no effect. Reset does not change the state of any of the flag bits in the TSR.

Address: $0013

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	ICF	OCF	TOF	0	0	0	0	0
Write:								
Reset:	U	U	U	0	0	0	0	0

= Unimplemented U = Unaffected

Figure 11-11. Timer Status Register (TSR)

ICF — Input Capture Flag

The ICF bit is automatically set when an edge of the selected polarity occurs on the TCAP pin. Clear the ICF bit by reading the timer status register with the ICF set, and then reading the low byte (ICRL, $0015) of the input capture registers. Resets have no effect on ICF.

OCF — Output Compare Flag

The OCF bit is automatically set when the value of the timer registers matches the contents of the output compare registers. Clear the OCF bit by reading the timer status register with the OCF set and then accessing the low byte (OCRL, $0017) of the output compare registers. Resets have no effect on OCF.

PEPGM — PEPROM Program Control Bit

This read/write bit controls the switches that apply the programming voltage from the $\overline{IRQ}/V_{PP}$ pin to the selected PEPROM bit cell. When the PEPGM bit is set, the selected bit cell will be programmed to a logic 1, regardless of the state of the PEDATA bit. Reset clears the PEPGM bit.

1 = Programming voltage applied to array bit
0 = Programming voltage not applied to array bit

PEPRZF — PEPROM Row Zero Flag

This read-only bit is set when the PEPROM bit select register selects the first row (row zero) of the PEPROM array. Selecting any other row clears PEPRZF. Monitoring PEPRZF can reduce the code needed to access one byte of eight PEPROM locations. Reset clears the PEPROM bit select register, thereby setting the PEPRZF bit by default.

1 = Row zero selected
0 = Row zero not selected

Table 12-1. PEPROM Bit Selection

PEBSR	PEPROM Bit Selected	
$00	Row 0	Column 0
$01	Row 1	Column 0
|	|	|
V	V	V
$07	Row 7	Column 0
$08	Row 0	Column 1
$09	Row 1	Column 1
|	|	|
V	V	V
$37	Row 7	Column 6
$38	Row 0	Column 7
$39	Row 1	Column 7
|	|	|
V	V	V
$3E	Row 6	Column 7
$3F	Row 7	Column 7

12.3 PEPROM Programming

Factory-provided software for programming the PEPROM is available on the World Wide Web at:
http://www.freescale.com

NOTE

While the PEPGM bit is set and the V_{PP} voltage level is applied to the $\overline{IRQ}/V_{PP}$ pin, do not access bits that are to be left unprogrammed (erased).

To program the PEPROM bits properly, the V_{DD} voltage must be greater than 4.5 Vdc.

The PEPROM can also be programmed by user software with the V_{PP} voltage level applied to the $\overline{IRQ}/V_{PP}$ pin. This sequence shows how to program each PEPROM bit:

1. Select a PEPROM bit by writing to the PEBSR.
2. Set the PEPGM bit in the PESCR.
3. Wait for the programming time, t_{EPGM}.
4. Clear the PEPGM bit.
5. Move to next PEPROM bit to be programmed in step 1.

12.4 PEPROM Reading

This sequence shows how to read the PEPROM:

1. Select a bit by writing to the PEBSR.
2. Read the PEDATA bit in the PESCR.
3. Store the PEDATA bit in RAM or in a register.
4. Select another bit by changing the PEBSR.
5. Continue reading and storing the PEDATA bits until the required personality EPROM data is retrieved and stored.

Reading the PEPROM is easiest when each PEPROM column contains one byte. Selecting a row 0 bit selects the first bit, and incrementing the PEPROM bit select register (PEBSR) selects the next bit in row 1 from the same column. Incrementing PEBSR seven more times selects the remaining bits of the column and ends up selecting the bit in row 0 of the next column, thereby setting the row 0 flag, PEPRZF.

NOTE

A PEPROM byte that has been read can be transferred to the personality EPROM bit select register (PEBSR) as a temporary storage location such that subsequent reads of the PEBSR quickly yield that PEPROM byte.

12.5 PEPROM Erasing

MCUs with windowed packages permit PEPROM erasing with ultraviolet light. Erase the PEPROM by exposing it to 15 Ws/cm^2 of ultraviolet light with a wavelength of 2537 angstroms. Position the ultraviolet light source 1 inch from the window. Do not use a shortwave filter. The erased state of a PEPROM bit is a logic 0.

DELAY — Stop Startup Delay Bit

This EPROM bit selects the number of bus cycles that must elapse before bus activity begins following a restart from the stop mode.

1 = Startup delay is 4064 bus cycles.
0 = Startup delay is 16 bus cycles.

CAUTION

The 16-cycle delay option will work properly in devices with the internal low-power oscillator or with a steady external clock source. Check crystal/ceramic resonator specifications carefully before using the 16-cycle delay option with a crystal or ceramic resonator.

OSCRES — Oscillator Resistor Bit

This EPROM bit configures the internal shunt resistor.

1 = Oscillator configured with 2 M¾ shunt resistor
0 = Oscillator configured without a shunt resistor

NOTE

The optional oscillator resistor is NOT recommended for devices that use an external RC oscillator. For such devices, this bit should be left erased as a 0.

SWAIT — STOP Conversion to WAIT Bit

This EPROM bit disables the STOP instruction and prevents inadvertently turning off the COP watchdog with a STOP instruction. When the SWAIT bit is set, a STOP instruction puts the MCU in halt mode. Halt mode is a wait-like low-power state. The internal oscillator and timer clock continue to run, but the CPU clock stops. When the SWAIT bit is clear, a STOP instruction stops the internal oscillator, the internal clock, the CPU clock, the timer clock, and the COP watchdog timer.

1 = STOP instruction converted to WAIT instruction
0 = STOP instruction not converted to WAIT instruction

LVREN — Low-Voltage Reset Enable Bit

This EPROM bit enables the low-voltage reset (LVR) function.

1 = LVR function enabled
0 = LVR function disabled

PIRQ — Port A IRQ Enable Bit

This EPROM bit enables the PA3–PA0 pins to function as external interrupt sources.

1 = PA3–PA0 enabled as external interrupt sources
0 = PA3–PA0 not enabled as external interrupt sources

LEVEL — External Interrupt Sensitivity Bit

This EPROM bit makes the external interrupt inputs level-triggered as well as edge-triggered

1 = $\overline{IRQ}/V_{PP}$ pin negative-edge triggered and low-level triggered;
PA3–PA0 pins positive-edge triggered and high-level triggered
0 = $\overline{IRQ}/V_{PP}$ pin negative-edge triggered only; PA3–PA0 pins positive-edge triggered only

COPEN — COP Watchdog Enable Bit

This EPROM bit enables the COP watchdog.

1 = COP watchdog enabled
0 = COP watchdog disabled

Chapter 15
Electrical Specifications

15.1 Introduction

This section contains the electrical and timing specifications.

15.2 Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

The MCU contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table below. Keep V_{In} and V_{Out} within the range $V_{SS} \le (V_{In}$ or $V_{Out}) \le V_{DD}$. Connect unused inputs to the appropriate voltage level, either V_{SS} or V_{DD}.

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +7.0	V
Bootloader/self-check mode ($\overline{IRQ}/V_{PP}$ pin only)	V_{In}	V_{SS} –0.3 to 17	V
Current drain per pin excluding V_{DD} and V_{SS}	I	25	mA
Operating junction temperature	T_J	+150	°C
Storage temperature range	T_{stg}	–65 to +150	°C

NOTE

This device is not guaranteed to operate properly at the maximum ratings. Refer to 15.7 DC Electrical Characteristics (5.0 Vdc) and 15.8 DC Electrical Characteristics (3.0 Vdc) for guaranteed operating conditions.

15.3 Operating Temperature Range

Characteristic	Symbol	Value	Unit
Operating temperature range Extended	T_A	T_L to T_H –40 to +85	°C

15.4 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance Plastic DIP SOIC	θ_{JA}	60	°C/W

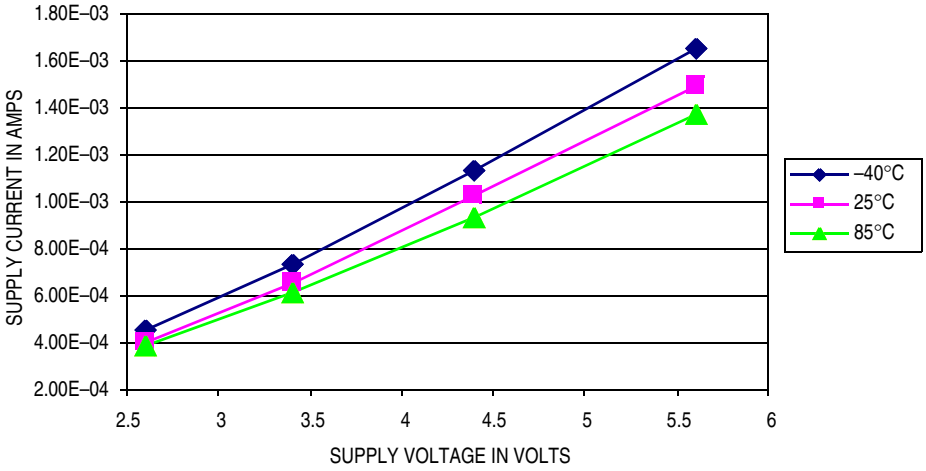


Figure 15-4. Typical Wait I_{DD} with External Oscillator

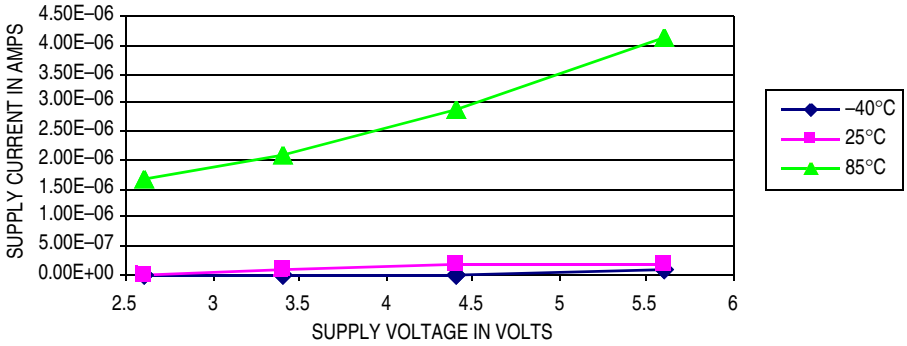


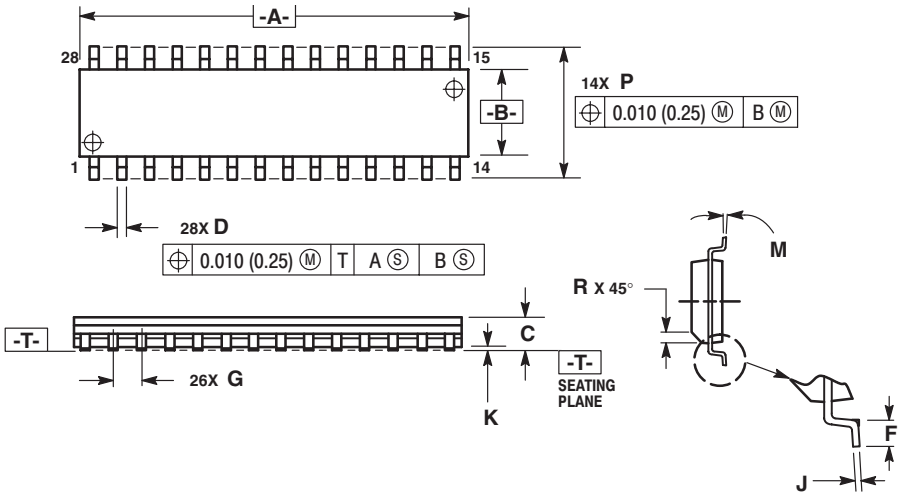
Figure 15-5. Typical Stop I_{DD} with Analog and LVR Disabled

15.8 DC Electrical Characteristics (3.0 Vdc)

Characteristic[1], [2]	Symbol	Min	Typ[3]	Max	Unit
Output voltage I_{Load} = 10.0 µA I_{Load} = –10.0 µA	V_{OL} V_{OH}	— V_{DD} –0.1	— —	0.1 —	V
Output high voltage (I_{Load} = –0.2 mA) PB0–PB7 (I_{Load} = –2.0 mA) PA0–PA5, PB4, PC0–PC7[4]	V_{OH}	V_{DD} –0.8 V_{DD} –0.8	— —	— —	V
Output low voltage (I_{Load} = 1.6 mA) PB0–PB7, $\overline{RESET}$ (I_{Load} = 5 mA) PA0–PA5, PB4, PC0–PC7[4]	V_{OL}	— —	— —	0.3 0.3	V
High source current Total for all (6) PA0–PA5 pins and PB4 Total for all (8) PC0–PC7[4] pins	I_{OH}	— —	— —	20 30	mA
High sink current Total for all (6) PA0–PA5 pins and PB4 Total for all (8) PC0–PC7[4] pins	I_{OL}	— —	— —	40 60	mA
Input high voltage PA0–PA5, PB0–PB7, PC0–PC7[4], $\overline{RESET}$, OSC1, $\overline{IRQ}$/V_{PP}	V_{IH}	0.7 x V_{DD}	—	V_{DD}	V
Input low voltage PA0–PA5, PB0–PB7, PC0–PC7[4], $\overline{RESET}$, OSC1, $\overline{IRQ}$/V_{PP}	V_{IL}	V_{SS}	—	0.2 x V_{DD}	V
Input current OSC1, $\overline{IRQ}$/V_{PP}	I_{In}	–1	—	1	µA
Input current $\overline{RESET}$ (pullup, source) $\overline{RESET}$ (pulldown, sink)	I_{In}	5 –3	— —	— —	µA mA
I/O ports hi-Z leakage current (pulldowns off) PA0–PA6, PB0–PB7, PC0–PC7[4]	I_{OZ}	–2	—	2	µA
Input pulldown current PA0–PA5, PB0–PB7, PC0–PC7[4] (V_{In} ; V_{IH} = 0.7 x V_{DD}) PA0–PA5, PB0–PB7, PC0–PC7[4] (V_{In} ; V_{IL} = 0.3 x V_{DD})	I_{IL}	10 4	25 20	75 40	µA

1. +2.7 ≤ V_{DD} ≤ +3.3 V, V_{SS} = 0 V, $T_L \le T_A \le T_H$, unless otherwise noted
2. All values shown reflect average measurements.
3. Typical values at midpoint of voltage range, 25°C only.
4. PC0–PC7 parameters only apply to MC68HC705JP7.

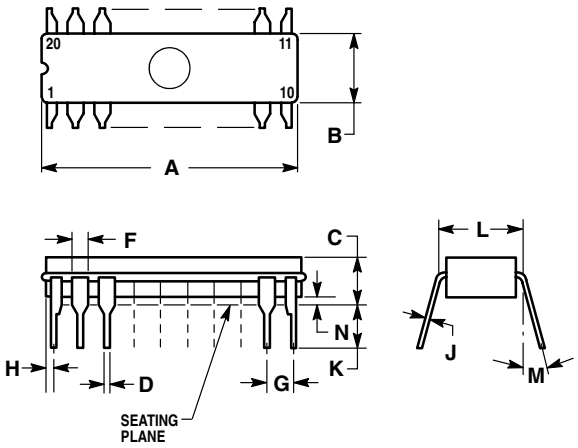
16.5 28-Pin Small Outline Integrated Circuit (Case 751F)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

16.6 20-Pin Windowed Ceramic Integrated Circuit (Case 732)



NOTES:
1. LEADS WITHIN 0.010 DIAMETER, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS A AND B INCLUDE MENISCUS.

	INCHES	
DIM	MIN	MAX
A	0.940	0.990
B	0.260	0.295
C	0.150	0.200
D	0.015	0.022
F	0.055	0.065
G	0.100 BSC	
H	0.020	0.050
J	0.008	0.012
K	0.125	0.160
L	0.300 BSC	
M	0°	15°
N	0.010	0.040