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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SIO
Peripherals	POR, Temp Sensor, WDT
Number of I/O	22
Program Memory Size	6KB (6K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	224 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mchc705jp7cdwe

- Power-saving stop and wait mode instructions (MOR selectable STOP conversion to halt and option for fast 16-cycle restart
and power-on reset)
- On-chip temperature measurement diode
- MOR selectable reset module to reset central processor unit (CPU) in low-voltage conditions
- Illegal address reset
- Internal steering diode and pullup device on $\overline{\text{RESET}}$ pin to V_{DD}

1.3 Device Options

These device options are available:

- On-chip oscillator type: crystal/ceramic resonator connections or resistor-capacitor (RC) connections
- Nominal frequency of internal low-power oscillator: 100 or 500 kHz

NOTE

A line over a signal name indicates an active low signal. For example, RESET is active high and $\overline{\text{RESET}}$ is active low.

Any reference to voltage, current, or frequency specified in the following sections will refer to the nominal values. The exact values and their tolerance or limits are specified in Chapter 15 Electrical Specifications.

Combinations of the various device options are specified by part number. Refer to Table 1-1 and to Chapter 17 Ordering Information for specific ordering information.

Table 1-1. Device Options by Part Number

Part Number	Pin Count	Oscillator Type	Internal LPO Nominal Frequency (kHz)
MC68HC705JJ7 MC68HC705JP7	20 28	Crystal/resonator Crystal/resonator	100 100
MC68HC705SJ7 MC68HC705SP7	20 28	Crystal/resonator Crystal/resonator	500 500
MC68HRC705JJ7 MC68HRC705JP7	20 28	Resistor-capacitor Resistor-capacitor	100 100

Chapter 2
Memory

2.1 Introduction

This section describes the organization of the memory on the MC68HC705JJ7/MC68HC705JP7.

2.2 Memory Map

The central processor unit (CPU) can address 8 kilobytes of memory space as shown in Figure 2-1. The memory map includes:

- The erasable programmable read-only memory (EPROM) portion of memory holds the program instructions, fixed data, user-defined vectors, and interrupt service routines.
- The random-access memory (RAM) portion of memory holds variable data.
- Input/output (I/O) registers are memory mapped so that the CPU can access their locations in the same way that it accesses all other memory locations.

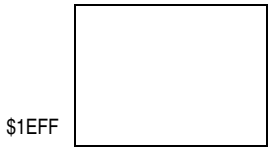


Figure 2-1. Memory Map

2.3 Input/Output Registers

Figure 2-2 and Figure 2-3 summarize:

- The first 32 addresses of the memory space, $0000–$001F, containing the I/O registers section
- One I/O register located outside the 32-byte I/O section, which is the computer operating properly register (COPR) mapped at $1FF0

Chapter 4
Interrupts

4.1 Introduction

An interrupt temporarily stops normal program execution to process a particular event. An interrupt does not stop the execution of the instruction in progress, but takes effect when the current instruction completes its execution. Interrupt processing automatically saves the central processor unit (CPU) registers on the stack and loads the program counter with a user-defined vector address.

4.2 Interrupt Vectors

Table 4-1 summarizes the reset and interrupt sources and vector assignments.

NOTE

If more than one interrupt request is pending, the CPU fetches the vector of the higher priority interrupt first. A higher priority interrupt does not actually interrupt a lower priority interrupt service routine unless the lower priority interrupt service routine clears the I bit.

Table 4-1. Reset/Interrupt Vector Addresses

Function	Source	MOR Control Bit	Global Hardware Mask	Local Software Mask	Priority (1 = Highest)	Vector Address
Reset	Power-on logic $\overline{\text{RESET}}$ pin Low-voltage reset Illegal address reset	—	—	—	1	$1FFE–$1FFF
	COP watchdog	COPEN(1)				
Software interrupt (SWI)	User code	—	—	—	Same priority as instruction	$1FFC–$1FFD
External interrupt (IRQ)	$\overline{\text{IRQ}}$/V_{PP} pin	—	I bit	IRQE bit	2	$1FFA–$1FFB
	PA3 pin PA2 pin PA1 pin PA0 pin	PIRQ(2)				
Core timer interrupts	TOF bit RTIF bit	—	I bit	TOFE bit RTIE bit	3	$1FF8–$1FF9
Programmable timer interrupts	ICF bit OCF bit TOF bit	—	I bit	ICIE bit OCIE bit TOIE bit	4	$1FF6–$1FF7
Serial interrupt	SPIF bit	—	I bit	SPIE bit	5	$1FF4–$1FF5
Analog interrupt	CPF1 bit CPF2 bit	—	I bit	CPIE bit	6	$1FF2–$1FF3

1. COPEN enables the COP watchdog timer.
2. PIRQ enables port A external interrupts on PA0–PA3.

7.2.2 Data Direction Register A

The contents of the port A data direction register (DDRA) determine whether each port A pin is an input or an output. Writing a logic 1 to a DDRA bit enables the output buffer for the associated port A pin. A DDRA bit set to a logic 1 also disables the pulldown device for that pin. Writing a logic 0 to a DDRA bit disables the output buffer for the associated port A pin. The upper two bits always read as logic 0s. A reset initializes all DDRA bits to logic 0s, configuring all port A pins as inputs and disabling the voltage comparators from driving PA4 or PA5.

Address: $0004

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 7-2. Data Direction Register A (DDRA)

DDRA5–DDRA0 — Port A Data Direction Bits

These read/write bits control port A data direction. Reset clears the DDRA5–DDRA0 bits.

1 = Corresponding port A pin configured as output and pulldown device disabled

0 = Corresponding port A pin configured as input

7.2.3 Pulldown Register A

All port A pins can have software programmable pulldown devices enabled or disabled globally by SWPDI bit in the MOR. These pulldown devices are controlled by the write-only pulldown register A (PDRA) shown in Figure 7-3. Clearing the PDIA5–PDIA0 bits in the PDRA turns on the pulldown devices if the port A pin is an input. Reading the PDRA returns undefined results since it is a write-only register; therefore, do not change the value in PDRA with read/modify/write instructions. On the MC68HC705JP7 the PDRA contains two pulldown control bits (PDICH and PDICL) for port C. Reset clears the PDIA5–PDIA0, PDICH, and PDICL bits, which turns on all the port A and port C pulldown devices.

Address: $0010

	Bit 7	6	5	4	3	2	1	Bit 0
Read:								
Write:	PDICH	PDICL	PDIA5	PDIA4	PDIA3	PDIA2	PDIA1	PDIA0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 7-3. Pulldown Register A (PDRA)

PDICH — Upper Port C Pulldown Inhibit Bits (MC68HC705JP7)

Writing to this write-only bit controls the port C pulldown devices on the upper four bits (PC4–PC7). Reading these pulldown register A bits returns undefined data. Reset clears bit PDICH.

1 = Upper four port C pins pulldown devices turned off

0 = Upper four port C pins pulldown devices turned on if pin has been programmed by the DDRC to be an input

7.3.9 PB7/SCK Logic

The PB7/SCK pin can be used as a simple I/O port pin or be controlled by the SIOP serial interface as shown in Figure 7-12. The operations of the PB7/SCK pin are summarized in Table 7-3.

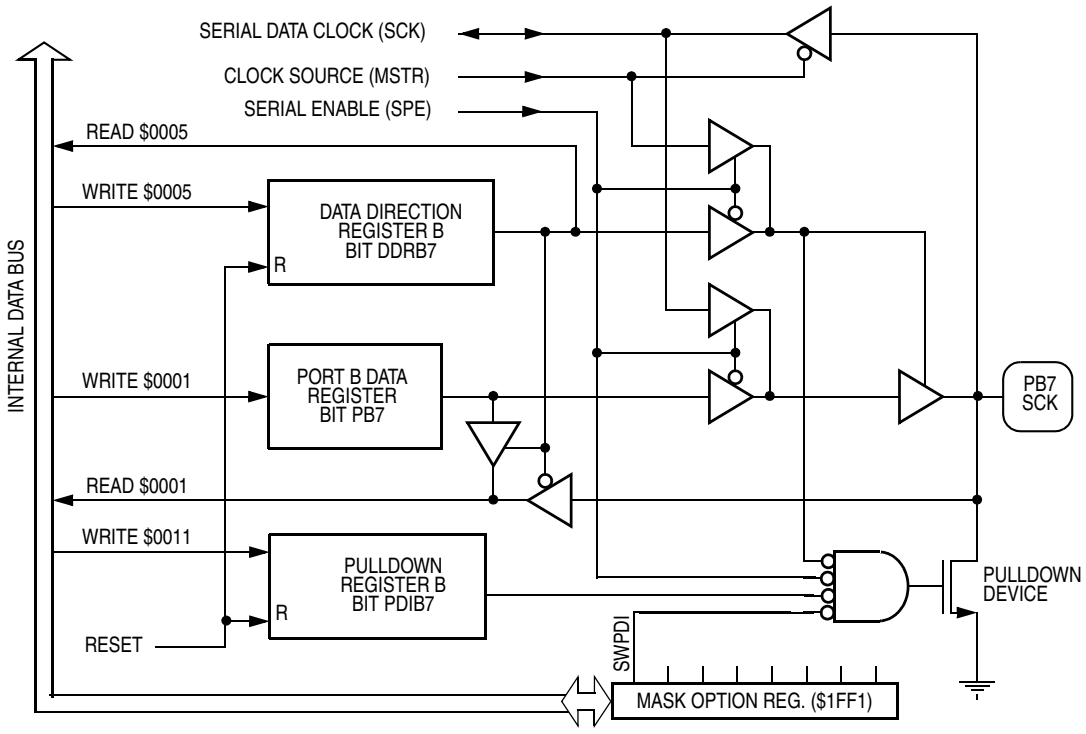
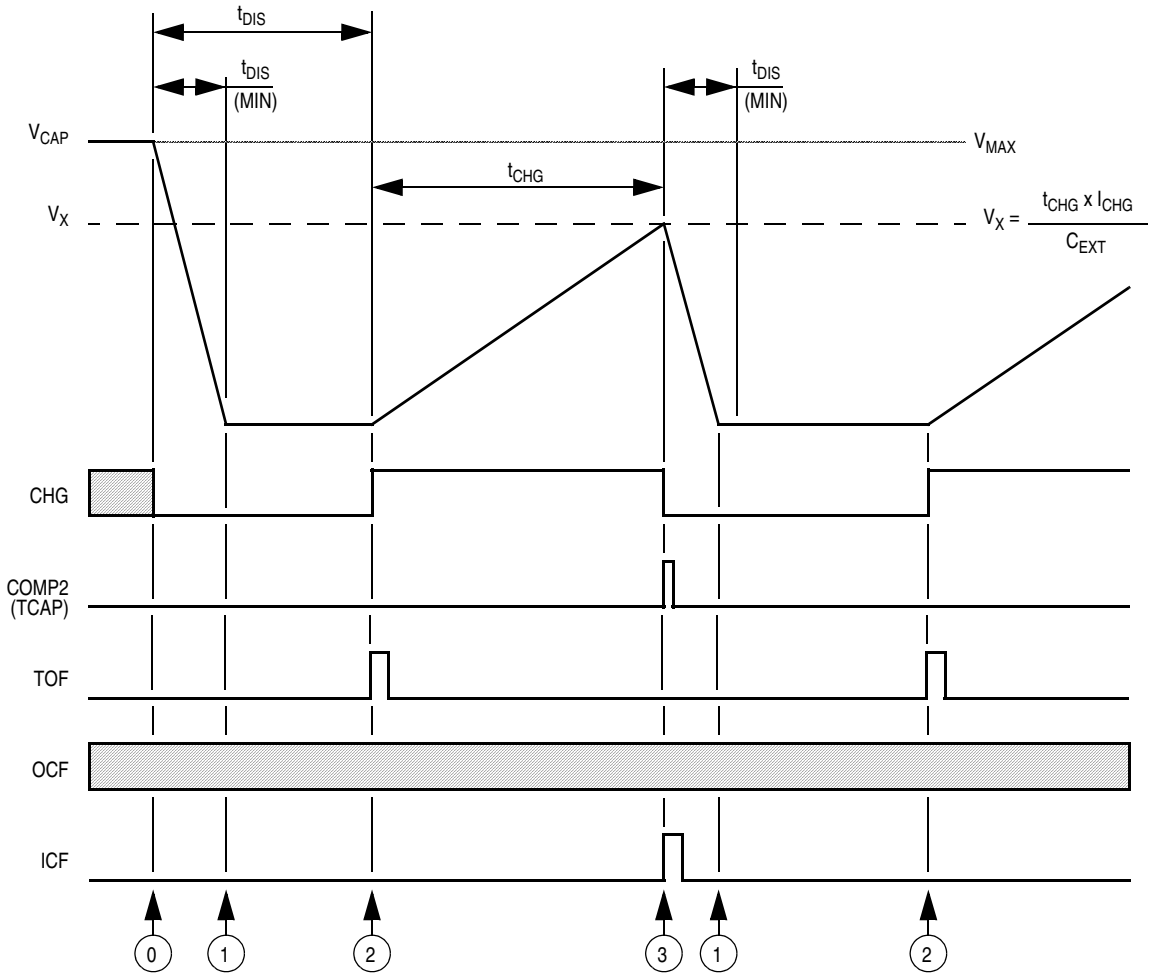


Figure 7-12. PB7/SCK Pin I/O Circuit

When using the PB7/SCK pin, these interactions must be noted:

1. If the SIOP function is required, then the SPE bit in the SCR must be set. This causes the PB7/SCK pin buffer to be controlled by the MSTR control bit in the SCR. The pulldown device is disabled in these cases.
   a. If the MSTR bit is set, then the PB7/SCK pin buffer will be enabled and driven by the serial data clock (SCK) from the SIOP.
   b. If the MSTR bit is clear, then the PB7/SCK pin buffer will be disabled, allowing the PB7/SCK pin to drive the serial data clock (SCK) into the SIOP.
2. If the SIOP function is in control of the PB7/SCK pin, the DDRB7 and PB7 data register bits are still accessible to the CPU and can be altered or read without affecting the SIOP functionality. However, if the DDRB7 bit is cleared, reading the PB7 data register will return the current state of the PB7/SCK pin.
3. If the SIOP function is terminated by clearing the SPE bit in the SCR, then the last conditions stored in the DDRB7, PDIB7, and PB7 register bits will then control the PB7/SCK pin.
4. If the PB7/SCK pin is to be a digital input, then both the SPE bit in the SCR and the DDRB7 bit must be cleared. Depending on the external application, the pulldown device may also be disabled by setting the PDIB7 pulldown inhibit bit.



Point	Action	Software/Hardware Action	Dependent Variable(s)
0	Begin initial discharge and select mode 2 by clearing CHG and ATD1 and setting ATD2 in the ACR. Also set ICEN bit in ACR and IEDG bit in TCR.	Software write	Software
1	V_{CAP} falls to V_{SS}.	Wait out minimum t_{DIS} time.	V_{MAX}, I_{DIS}, C_{EXT}
2	Stop discharge and begin charge when the next TOF sets the CHG control bit in ACR.	Timer TOF sets the CHG control bit in the ACR.	Free-running timer counter overflow, f_{OSC}
3	V_{CAP} rises to V_X and comparator 2 output trips, setting CPF2 and CMP2, which causes an ICF from the timer and clears the CHG control bit in ACR. Must clear CPF2 to trap next CPF2 flag.	Wait out t_{CHG} time. Timer ICF clears the CHG control bit in the ACR.	V_X, I_{CHG}, C_{EXT}

Figure 8-10. A/D Conversion — TOF/ICF Control (Mode 2)

8.6 Voltage Measurement Methods

The methods for obtaining a voltage measurement can use software techniques to express these voltages as absolute or ratiometric readings.

In most applications the external capacitor, the clock source, the reference voltage, and the charging current may vary between devices and with changes in supply voltage or ambient temperature. All of these variations must be considered when determining the desired resolution of the measurement. The maximum and minimum extremes for the full scale count will be:

$$N_{FSMIN} = C_{EXTMIN} \times V_{FSMIN} \times f_{OSCMIN} / (P \times I_{CHGMAX})$$

$$N_{FSMAX} = C_{EXTMAX} \times V_{FSMAX} \times f_{OSCMAX} / (P \times I_{CHGMIN})$$

The minimum count should be the desired resolution, and the counting mechanism must be capable of counting to the maximum. The final scaling of the count will be by a math routine which calculates:

$$V_X = V_{REF} \times (N_X - N_{OFF}) / (N_{REF} - N_{OFF})$$

Where:

V_{REF} = Known reference voltage

V_X = Unknown voltage between V_{SS} and V_{REF}

N_X = Conversion count for unknown voltage

N_{REF} = Conversion count for known reference voltage (V_{REF})

N_{OFF} = Conversion count for minimum reference voltage (V_{SS})

When V_{REF} is a stable voltage source such as a zener or other reference source, then the unknown voltage will be determined as an absolute reading. If V_{REF} is the supply source to the device (V_{DD}), then the unknown voltage will be determined as a ratio of V_{DD}, or a ratiometric reading.

If the unknown voltage applied to the comparator is greater than its common-mode range (V_{DD} –1.5 volts), then the external capacitor will try to charge to the same level. This will cause both comparator inputs to be above the common-mode range and the output of the comparator will be indeterminate. In this case the comparator output flags may also be set even if the actual voltage on the positive input (+) is less than the voltage on the negative input (–). All A/D conversion methods should have a maximum time check to determine if this case is occurring.

Once the maximum timeout detection has been made, the state of the comparator outputs can be tested to determine the situation. However, such tests should be carefully designed when using modes 1, 2, or 3 as these modes cause the immediate automatic discharge of the external ramping capacitor before any software check can be made of the output state of comparator 2.

NOTE

All A/D conversion methods should include a test for a maximum elapsed time to detect error cases where the inputs may be outside of the design specification.

8.6.1 Absolute Voltage Readings

The absolute value of a voltage measurement can be calculated in software by first taking a reference reading from a fixed source and then comparing subsequent unknown voltages to that reading as a percentage of the reference voltage multiplied times the known reference value.

The accuracy of absolute readings will depend on the error sources taken into account using the features of the analog subsystem and appropriate software as described in Table 8-6. As can be seen from this table, most of the errors can be reduced by frequent comparisons to a known voltage, use of the inverted comparator inputs, and averaging of multiple samples.

8.6.1.1 Internal Absolute Reference

If a stable source of V_{DD} is provided, the reference measurement point can be internally selected. In this case, the reference reading can be taken by setting the V_{REF} bit and clearing the MUX1:4 bits in the AMUX register. This connects the channel selection bus to the V_{DD} pin. To stay within the V_{MAX} range, the DHOLD bit should be used to select the 1/2 divided input.

8.6.1.2 External Absolute Reference

If a stable external source is provided, the reference measurement point can be any one of the channel selected pins from PB1–PB4. In this case the reference reading can be taken by setting the MUX bit in the AMUX which connects channel selection bus to the pin connected to the external reference source. If the external reference is greater than V_{DD} –1.5 volts, then the DHOLD bit should be used to select the 1/2 divided input.

Table 8-6. Absolute Voltage Reading Errors

Error Source	Accuracy Improvements Possible	
	In Hardware	In Software
Change in reference voltage	Provide closer tolerance reference	Calibration and storage of reference source over temperature and supply voltage
Change in magnitude of ramp current source	Not adjustable	Compare unknown with recent measurement from reference
Non-linearity of ramp current source vs. voltage	Not adjustable	Calibration and storage of voltages at 1/4, 1/2, 3/4, and FS
Frequency shift in internal low-power oscillator	Use external oscillator with crystal	Compare unknown with recent measurement from reference
Sampling capacitor leakage	Use faster conversion times	Compare unknown with recent measurement from reference
Internal voltage divider ratio	Not adjustable	Compare unknown with recent measurement from reference OR avoid use of divided input
Input offset voltage of comparator 2	Not adjustable	Sum two readings on reference or unknown using INV and $\overline{INV}$ control bit and divide by 2 (average of both)
Noise internal to MCU	Close decoupling at V_{DD} and V_{SS} pins and reduce supply source impedance	Average multiple readings on both the reference and the unknown voltage

8.11 Port B Interaction with Analog Inputs

The analog subsystem is connected directly to the port B I/O pins without any intervening gates. It is, therefore, possible to measure the voltages on port B pins set as inputs or to have the analog voltage measurements corrupted by port B pins set as outputs.

8.12 Port B Pins as Inputs

All the port B pins will power up as inputs or return to inputs after a reset of the device since the bits in the port B data direction register will be reset.

If any port B pins are to be used for analog voltage measurements, they should be left as inputs. In this case, not only can the voltage on the pin be measured, but the logic state of the port B pins can be read from location $0002.

8.13 Port B Pulldowns

All the port B pins have internal software programmable pulldown devices available dependent on the state of the SWPDI bit in the mask option register (MOR).

If the pulldowns are enabled, they will create an approximate 100 µA load to any analog source connected to the pin. In some cases, the analog source may be able to supply this current without causing any error due to the analog source output impedance. Since this may not always be true, it is therefore best to disable port B pulldowns on those pins used for analog input sources.

8.14 Noise Sensitivity

In addition to the normal effects of electrical noise on the analog input signal there can also be other noise-related effects caused by the digital-to-analog interface. Since there is only one V_{SS} return for both the digital and the analog subsystems on the device, currents in the digital section may affect the analog ground reference within the device. This can add voltage offsets to measured inputs or cause channel-to-channel crosstalk.

To reduce the impact of these effects, there should be no switching of heavy I/O currents to or from the device while there is a critical analog conversion or voltage comparison in process. Limiting switched I/O currents to 2–4 mA during these times is recommended.

A noise reduction benefit can be gained with 0.1-µF bypass capacitors from each analog input (PB4:1) to the V_{SS} pin. Also, try to keep all the digital power supply or load currents from passing through any conductors which are the return paths for an analog signal.

Chapter 10
Core Timer

10.1 Introduction

This section describes the operation of the core timer and the computer operating properly (COP) watchdog as shown by the block diagram in Figure 10-1.

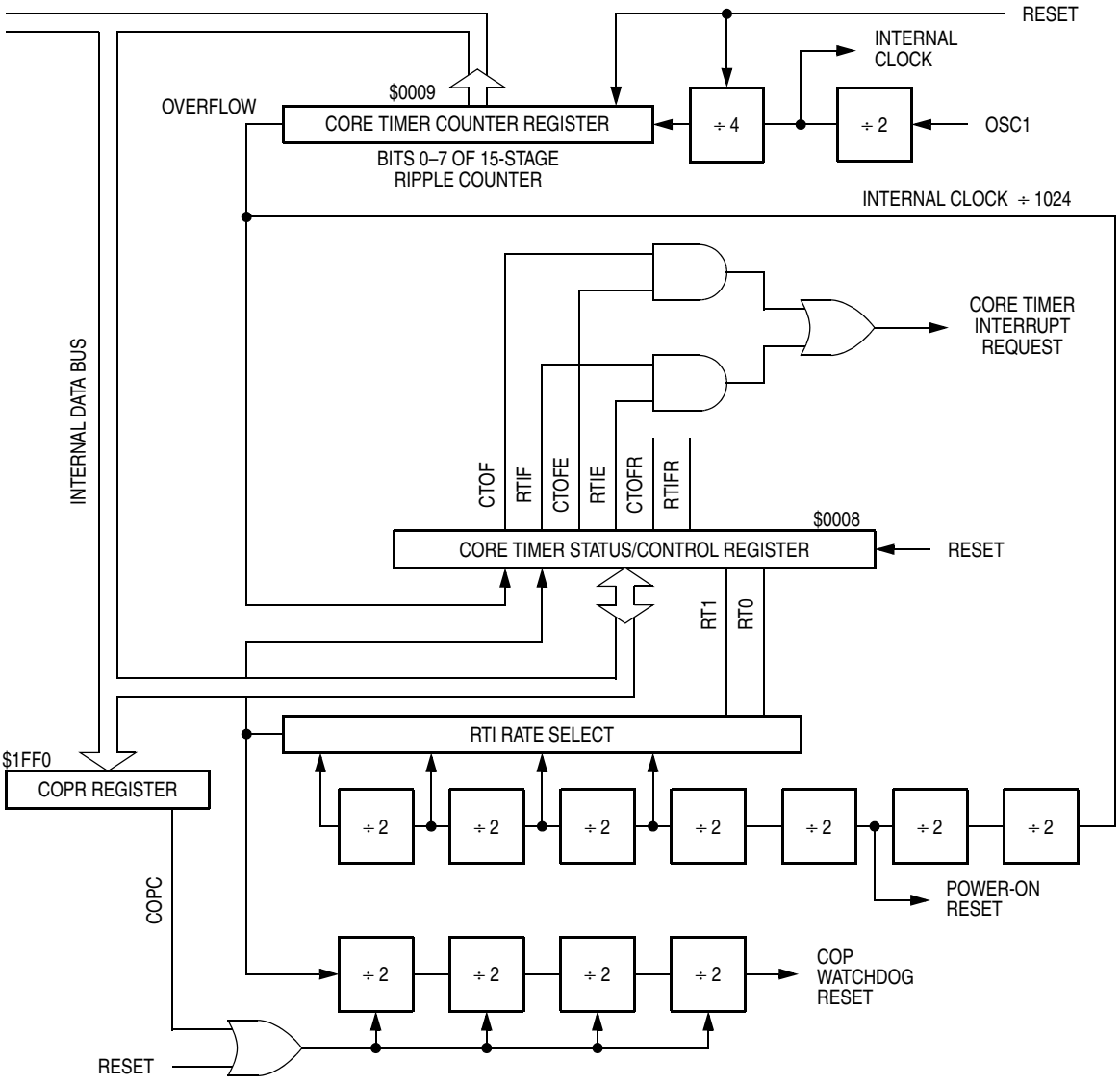


Figure 10-1. Core Timer Block Diagram

Table 11-1. Output Compare Initialization Example

9B		SEI		DISABLE INTERRUPTS
...		...		.....
...		...		.....
B7	16	STA	OCRH	INHIBIT OUTPUT COMPARE
B6	13	LDA	TSR	ARM OCF FLAG FOR CLEARING
BF	17	STX	OCRL	READY FOR NEXT COMPARE, OCF CLEARED
...		...		.....
...		...		.....
9A		CLI		ENABLE INTERRUPTS

11.6 Timer Control Register

The timer control register (TCR) shown in Figure 11-10, performs the following functions:

- Enables input capture interrupts
- Enables output compare interrupts
- Enables timer overflow interrupts
- Controls the active edge polarity of the TCAP signal
- Controls the active level of the TCMP output

Reset clears all the bits in the TCR with the exception of the IEDG bit which is unaffected.

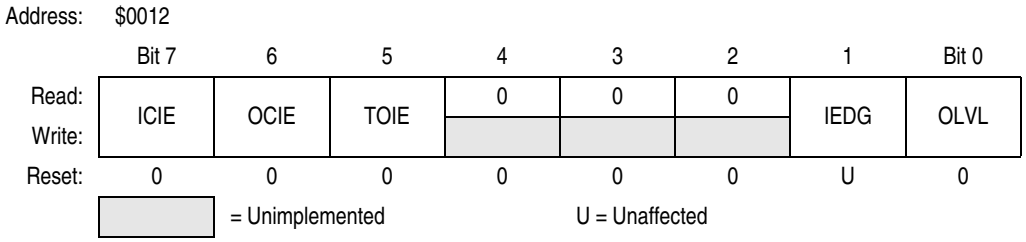


Figure 11-10. Timer Control Register (TCR)

ICIE — Input Capture Interrupt Enable Bit

This read/write bit enables interrupts caused by an active signal on the TCAP pin or from CPF2 flag bit of the analog subsystem voltage comparator 2. Reset clears the ICIE bit.

1 = Input capture interrupts enabled
0 = Input capture interrupts disabled

OCIE — Output Compare Interrupt Enable Bit

This read/write bit enables interrupts caused by an active match of the output compare function. Reset clears the OCIE bit.

1 = Output compare interrupts enabled
0 = Output compare interrupts disabled

TOIE — Timer Overflow Interrupt Enable

This read/write bit enables interrupts caused by a timer overflow. Reset clears the TOIE bit.

1 = Timer overflow interrupts enabled
0 = Timer overflow interrupts disabled

12.2 PEPROM Registers

Two I/O registers control programming and reading of the PEPROM:

- The PEPROM bit select register (PEBSR)
- The PEPROM status and control register (PESCR)

12.2.1 PEPROM Bit Select Register

The PEPROM bit select register (PEBSR) selects one of 64 bits in the PEPROM array. Reset clears all the bits in the PEPROM bit select register.

Address: $000E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PEB7	PEB6	PEB5	PEB4	PEB3	PEB2	PEB1	PEB0
Reset:	0	0	0	0	0	0	0	0

Figure 12-2. PEPROM Bit Select Register (PEBSR)

PEB7 and PEB6 — Not connected to the PEPROM array

These read/write bits are available as storage locations. Reset clears PEB7 and PEB6.

PEB5–PEB0 — PEPROM Bit Selects

These read/write bits select one of 64 bits in the PEPROM as shown in Table 12-1. Bits PEB2–0 select the PEPROM row, and bits PEB5–PEB3 select the PEPROM column. Reset clears PEB5–PEB0, selecting the PEPROM bit in row zero, column zero.

12.2.2 PEPROM Status and Control Register

The PEPROM status and control register (PESCR) controls the PEPROM programming voltage. This register also transfers the PEPROM bits to the internal data bus and contains a flag bit when row zero is selected.

Address: $000F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PEDATA	0	PEPGM	0	0	0	0	PEPRZF
Write:					R	R	R	
Reset:	U	0	0	0	0	0	0	1

= Unimplemented R = Reserved U = Unaffected

Figure 12-3. PEPROM Status and Control Register (PESCR)

PEDATA — PEPROM Data Bit

This read-only bit is the output state of the PEPROM sense amplifier and shows the state of the currently selected bit. The state of the PEDATA bit does not affect the programming of the bit selected by the PEBSR. Reset does not affect the PEDATA bit.

1 = PEPROM data is a logic 1.
0 = PEPROM data is a logic 0.

14.4 Instruction Set Summary

Table 14-6. Instruction Set Summary (Sheet 1 of 6)

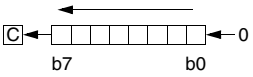
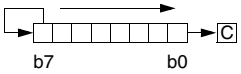
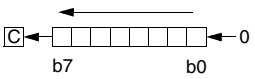
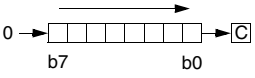
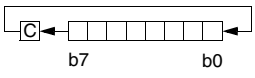
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
ADC #*opr* ADC *opr* ADC *opr* ADC *opr*,X ADC *opr*,X ADC ,X	Add with Carry	A ← (A) + (M) + (C)	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A9 B9 C9 D9 E9 F9	ii dd hh ll ee ff ff	2 3 4 5 4 3
ADD #*opr* ADD *opr* ADD *opr* ADD *opr*,X ADD *opr*,X ADD ,X	Add without Carry	A ← (A) + (M)	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	AB BB CB DB EB FB	ii dd hh ll ee ff ff	2 3 4 5 4 3
AND #*opr* AND *opr* AN*D opr* AND *opr*,X AND *opr*,X AND ,X	Logical AND	A ← (A) ∧ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A4 B4 C4 D4 E4 F4	ii dd hh ll ee ff ff	2 3 4 5 4 3
ASL *opr* ASLA ASLX ASL *opr*,X ASL ,X	Arithmetic Shift Left (Same as LSL)		—	—	↕	↕	↕	DIR INH INH IX1 IX	38 48 58 68 78	dd ff 	5 3 3 6 5
ASR *opr* ASRA ASRX ASR *opr*,X ASR ,X	Arithmetic Shift Right		—	—	↕	↕	↕	DIR INH INH IX1 IX	37 47 57 67 77	dd ff 	5 3 3 6 5
BCC *rel*	Branch if Carry Bit Clear	PC ← (PC) + 2 + *rel* ? C = 0	—	—	—	—	—	REL	24	rr	3
BCLR *n opr*	Clear Bit n	Mn ← 0	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5
BCS *rel*	Branch if Carry Bit Set (Same as BLO)	PC ← (PC) + 2 + *rel* ? C = 1	—	—	—	—	—	REL	25	rr	3
BEQ *rel*	Branch if Equal	PC ← (PC) + 2 + *rel* ? Z = 1	—	—	—	—	—	REL	27	rr	3
BHCC *rel*	Branch if Half-Carry Bit Clear	PC ← (PC) + 2 + *rel* ? H = 0	—	—	—	—	—	REL	28	rr	3
BHCS *rel*	Branch if Half-Carry Bit Set	PC ← (PC) + 2 + *rel* ? H = 1	—	—	—	—	—	REL	29	rr	3
BHI *rel*	Branch if Higher	PC ← (PC) + 2 + *rel* ? C ∨ Z = 0	—	—	—	—	—	REL	22	rr	3

Table 14-6. Instruction Set Summary (Sheet 2 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
BHS *rel*	Branch if Higher or Same	PC ← (PC) + 2 + *rel* ? C = 0	—	—	—	—	—	REL	24	rr	3
BIH *rel*	Branch if $\overline{\text{IRQ}}$ Pin High	PC ← (PC) + 2 + *rel* ? $\overline{\text{IRQ}}$ = 1	—	—	—	—	—	REL	2F	rr	3
BIL *rel*	Branch if $\overline{\text{IRQ}}$ Pin Low	PC ← (PC) + 2 + *rel* ? $\overline{\text{IRQ}}$ = 0	—	—	—	—	—	REL	2E	rr	3
BIT #*opr* BIT *opr* BIT *opr* BIT *opr*,X BIT *opr*,X BIT ,X	Bit Test Accumulator with Memory Byte	(A) ∧ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A5 B5 C5 D5 E5 F5	ii dd hh ll ee ff ff p	2 3 4 5 4 3
BLO *rel*	Branch if Lower (Same as BCS)	PC ← (PC) + 2 + *rel* ? C = 1	—	—	—	—	—	REL	25	rr	3
BLS *rel*	Branch if Lower or Same	PC ← (PC) + 2 + *rel* ? C ∨ Z = 1	—	—	—	—	—	REL	23	rr	3
BMC *rel*	Branch if Interrupt Mask Clear	PC ← (PC) + 2 + *rel* ? I = 0	—	—	—	—	—	REL	2C	rr	3
BMI *rel*	Branch if Minus	PC ← (PC) + 2 + *rel* ? N = 1	—	—	—	—	—	REL	2B	rr	3
BMS *rel*	Branch if Interrupt Mask Set	PC ← (PC) + 2 + *rel* ? I = 1	—	—	—	—	—	REL	2D	rr	3
BNE *rel*	Branch if Not Equal	PC ← (PC) + 2 + *rel* ? Z = 0	—	—	—	—	—	REL	26	rr	3
BPL *rel*	Branch if Plus	PC ← (PC) + 2 + *rel* ? N = 0	—	—	—	—	—	REL	2A	rr	3
BRA *rel*	Branch Always	PC ← (PC) + 2 + *rel* ? 1 = 1	—	—	—	—	—	REL	20	rr	3
BRCLR *n opr rel*	Branch if bit n clear	PC ← (PC) + 2 + *rel* ? Mn = 0	—	—	—	—	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	01 03 05 07 09 0B 0D 0F	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BRSET *n opr rel*	Branch if Bit n Set	PC ← (PC) + 2 + *rel* ? Mn = 1	—	—	—	—	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	00 02 04 06 08 0A 0C 0E	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BRN *rel*	Branch Never	PC ← (PC) + 2 + *rel* ? 1 = 0	—	—	—	—	—	REL	21	rr	3
BSET *n opr*	Set Bit n	Mn ← 1	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	10 12 14 16 18 1A 1C 1E	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5

Table 14-6. Instruction Set Summary (Sheet 4 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
JSR *opr* JSR *opr* JSR *opr*,X JSR *opr*,X JSR ,X	Jump to Subroutine	PC ← (PC) + n (n = 1, 2, or 3) Push (PCL); SP ← (SP) – 1 Push (PCH); SP ← (SP) – 1 PC ← Conditional Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BD CD DD ED FD	dd hh ll ee ff ff	5 6 7 6 5
LDA #*opr* LDA *opr* LDA *opr* LDA *opr*,X LDA *opr*,X LDA ,X	Load Accumulator with Memory Byte	A ← (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A6 B6 C6 D6 E6 F6	ii dd hh ll ee ff ff	2 3 4 5 4 3
LDX #*opr* LDX *opr* LDX *opr* LDX *opr*,X LDX *opr*,X LDX ,X	Load Index Register with Memory Byte	X ← (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	AE BE CE DE EE FE	ii dd hh ll ee ff ff	2 3 4 5 4 3
LSL *opr* LSLA LSLX LSL *opr*,X LSL ,X	Logical Shift Left (Same as ASL)		—	—	↕	↕	·	DIR INH INH IX1 IX	38 48 58 68 78	dd ff	5 3 3 6 5
LSR *opr* LSRA LSRX LSR *opr*,X LSR ,X	Logical Shift Right		—	—	0	↕	↕	DIR INH INH IX1 IX	34 44 54 64 74	dd ff	5 3 3 6 5
MUL	Unsigned Multiply	X : A ← (X) × (A)	0	—	—	—	0	INH	42		11
NEG *opr* NEGA NEGX NEG *opr*,X NEG ,X	Negate Byte (Two's Complement)	M ← –(M) = $00 – (M) A ← –(A) = $00 – (A) X ← –(X) = $00 – (X) M ← –(M) = $00 – (M) M ← –(M) = $00 – (M)	—	—	↕	↕	↕	DIR INH INH IX1 IX	30 40 50 60 70	ii ff	5 3 3 6 5
NOP	No Operation		—	—	—	—	—	INH	9D		2
ORA #*opr* ORA *opr* ORA *opr* ORA *opr*,X ORA *opr*,X ORA ,X	Logical OR Accumulator with Memory	A ← (A) ∨ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	AA BA CA DA EA FA	ii dd hh ll ee ff ff	2 3 4 5 4 3
ROL *opr* ROLA ROLX ROL *opr*,X ROL ,X	Rotate Byte Left through Carry Bit		—	—	↕	↕	↕	DIR INH INH IX1 IX	39 49 59 69 79	dd ff	5 3 3 6 5

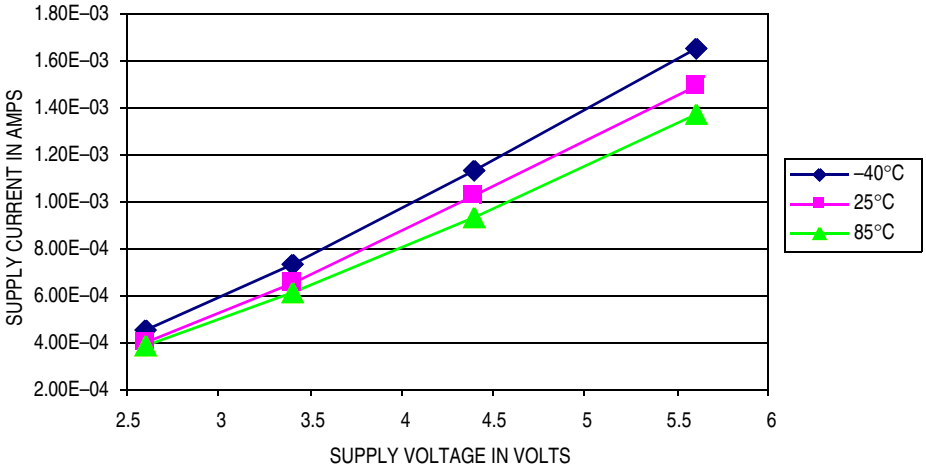


Figure 15-4. Typical Wait I_{DD} with External Oscillator

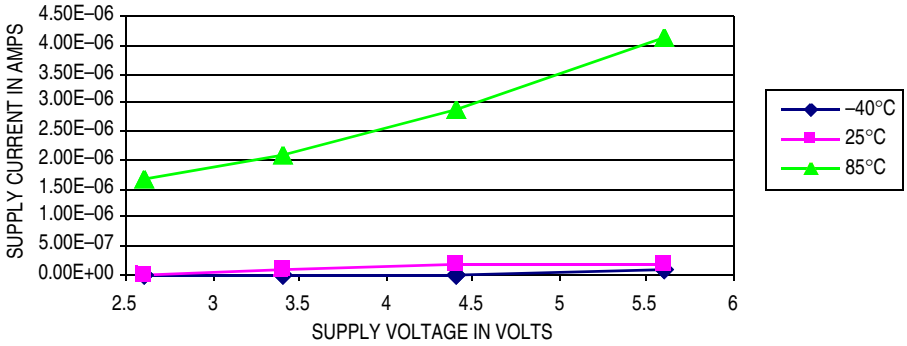


Figure 15-5. Typical Stop I_{DD} with Analog and LVR Disabled

15.13 PEPROM and EPROM Programming Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
PEPROM programming voltage ($\overline{IRQ}/V_{PP}$)	V_{PP}	16.0	16.5	17.0	V
PEPROM programming voltage ($\overline{IRQ}/V_{PP}$)	I_{PP}	—	3.0	5.0	mA
PEPROM programming time per bit	t_{EPGM}	4.0	—	—	ms
EPROM/MOR programming voltage ($\overline{IRQ}/V_{PP}$)	V_{PP}	16.0	16.5	17.0	V
EPROM/MOR programming current ($\overline{IRQ}/V_{PP}$)	I_{PP}	—	3.0	5.0	mA
EPROM programming time per byte	t_{EPGM}	4.0	—	—	ms
MOR programming time	t_{MPGM}	10.0	—	—	ms

1. $+4.5 \le V_{DD} \le +5.5$ V, $V_{SS} = 0$ V, $T_L \le T_A \le T_H$, unless otherwise noted

NOTE

To program the EPROM/OTPROM, MOR, or EPMSEC bits, the voltage on V_{DD} must be greater than 4.5 volts.