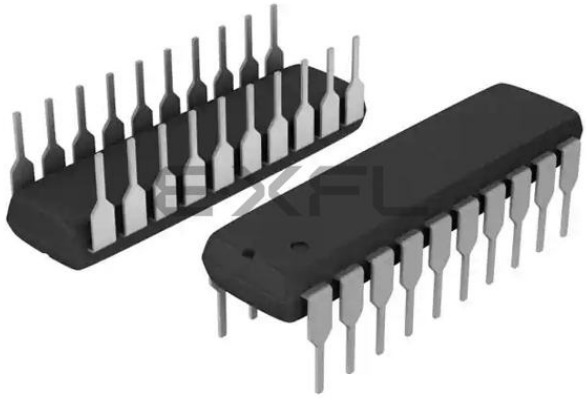

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Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SIO
Peripherals	POR, Temp Sensor, WDT
Number of I/O	14
Program Memory Size	6KB (6K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	224 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-DIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mchrc705jj7cpe

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General Description

Chapter 2
Memory

Chapter 3
Central Processor Unit (CPU)

1.8 $\overline{IRQ}/V_{PP}$ Pin

The $\overline{IRQ}/V_{PP}$ input pin drives the asynchronous IRQ interrupt function of the CPU. The IRQ interrupt function uses the LEVEL bit in the MOR to provide either negative edge-sensitive triggering or both negative edge-sensitive and low level-sensitive triggering. If the LEVEL bit is set to enable level-sensitive triggering, the $\overline{IRQ}/V_{PP}$ pin requires an external resistor to V_{DD} for “wired-OR” operation. If the $\overline{IRQ}/V_{PP}$ pin is not used, it must be tied to the V_{DD} supply. The $\overline{IRQ}/V_{PP}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity.

The voltage on this pin may affect operation if the voltage on the $\overline{IRQ}/V_{PP}$ pin is above V_{DD} when the device is released from a reset condition. The $\overline{IRQ}/V_{PP}$ pin should only be taken above V_{DD} to program an EPROM memory location or personality EPROM bit. For more information, refer to 15.13 PEPROM and EPROM Programming Characteristics.

NOTE

Each of the PA0–PA3 I/O pins may be connected as an OR function with the IRQ interrupt function by the PIRQ bit in the MOR. This capability allows keyboard scan applications where the transitions or levels on the I/O pins will behave the same as the $\overline{IRQ}/V_{PP}$ pin, except that active transitions and levels are inverted. The edge or level sensitivity selected by the LEVEL bit in the MOR for the $\overline{IRQ}/V_{PP}$ pin also applies to the I/O pins that are ORed to create the IRQ signal. For more information, refer to 4.5 External Interrupts.

1.9 PA0–PA5

These six I/O lines comprise port A, a general-purpose bidirectional I/O port. This port also has four pins which have keyboard interrupt capability. All six of these pins have high current source and sink capability.

All of these pins have software programmable pulldowns which can be disabled by the SWPDI bit in the MOR.

1.10 PB0–PB7

These eight I/O lines comprise port B, a general-purpose bidirectional I/O port. This port is also shared with the 16-bit programmable timer input capture and output compare functions, with the two voltage comparators in the analog subsystem, and with the simple serial interface (SIOP).

The outputs of voltage comparator 1 can directly drive the PB4 pin; and the PB4 pin has high current source and sink capability.

All of these pins have software programmable pulldowns which can be disabled by the SWPDI bit in the MOR.

1.11 PC0–PC7 (MC68HC705JP7)

These eight I/O lines comprise port C, a general-purpose bidirectional I/O port. This port is only available on the 28-pin MC68HC705JP7. All eight of these pins have high current source and sink capability.

All of these pins have software programmable pulldowns which can be disabled by the SWPDI bit in the MOR.

Address	Register Name
$0000	Port A Data Register
$0001	Port B Data Register
$0002	Port C Data Register *
$0003	Analog MUX Register
$0004	Port A Data Direction Register
$0005	Port B Data Direction Register
$0006	Port C Data Direction Register *
$0007	Unused
$0008	Core Timer Status & Control Register
$0009	Core Timer Counter
$000A	Serial Control Register
$000B	Serial Status Register
$000C	Serial Data Register
$000D	IRQ Status & Control Register
$000E	Personality EPROM Bit Select Register
$000F	Personality EPROM Status & Control Register
$0010	Port A and Port C Pulldown Register *
$0011	Port B Pulldown Register
$0012	Timer Control Register
$0013	Timer Status Register
$0014	Input Capture Register (MSB)
$0015	Input Capture Register (LSB)
$0016	Output Compare Register (MSB)
$0017	Output Compare Register (LSB)
$0018	Timer Counter Register (MSB)
$0019	Timer Counter Register (LSB)
$001A	Alternate Counter Register (MSB)
$001B	Alternate Counter Register (LSB)
$001C	EPROM Programming Register
$001D	Analog Control Register
$001E	Analog Status Register
$001F	Reserved

* Features related to port C are only available on the 28-pin MC68HC705JP7 devices.

Figure 2-2. I/O Registers

7.3.4 Port B Logic

All port B pins have the general I/O port logic similar to port A; but they also share this function with inputs or outputs from other modules, which are also attached to the pin itself or override the general I/O function. PB0, PB1, PB2, and PB3 simply share their inputs with another module. PB4, PB5, PB6, and PB7 will have their operation altered by outputs or controls from other modules.

7.3.5 PB0, PBI, PB2, and PB3 Logic

The typical I/O logic shown in Figure 7-8 is used for PB0, PB1, PB2, and PB3 pins of port B. When these port B pins are programmed as an output, reading the port bit actually reads the value of the data latch and not the voltage on the pin itself. When these port B pins are programmed as an input, reading the port bit reads the voltage level on the pin. The data latch can always be written, regardless of the state of its DDRB bit. The operations of the PB0–PB3 pins are summarized in Table 7-2.

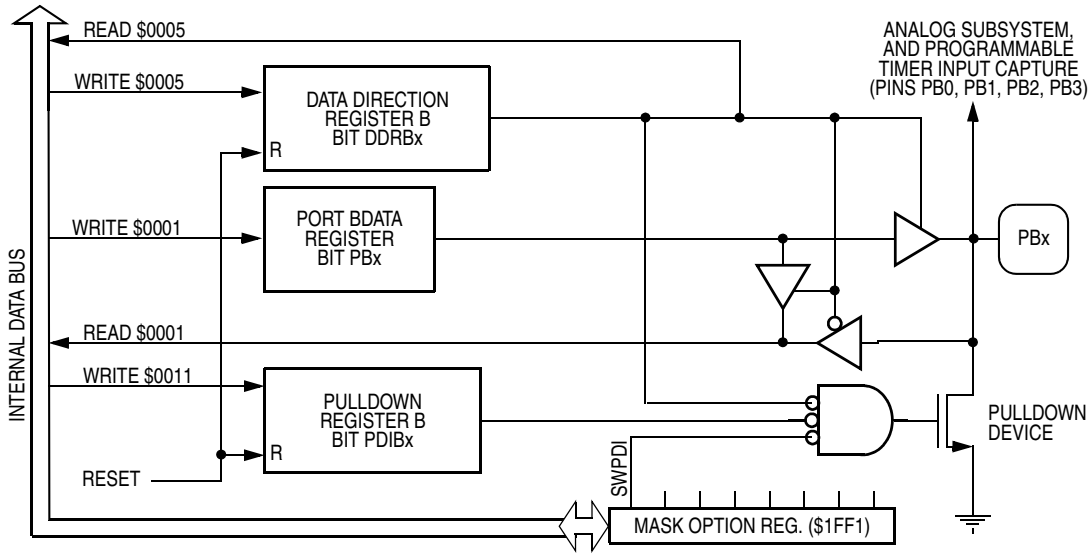


Figure 7-8. PB0–PB3 Pin I/O Circuit

The PB0–PB3 pins share their inputs with another module. When using the other attached module, these conditions must be observed:

1. If the DDRB configures the pin as an output, then the port data register can provide an output which may conflict with any external input source to the other module. The pulldown device will be disabled in this case.
2. If the DDRB configures the pin as an input, then reading the port data register will return the state of the input in terms of the digital threshold for that pin (analog inputs will default to logic states).
3. If DDRB configures the pin as an input and the pulldown device is activated for a pin, it will also load the input to the other module.
4. If interaction between the port logic and the other module is not desired, the pin should be configured as an input by clearing the appropriate DDRB bit. The input pulldown device is disabled by clearing the appropriate PDRB bit (or by disabling programmable pulldowns with the SWPDI bit in the MOR).

Address: $001D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	CHG	ATD2	ATD1	ICEN	CPIE	CP2EN	CP1EN	ISEN
Reset:	0	0	0	0	0	0	0	0

Figure 8-5. Analog Control Register (ACR)

CHG

The CHG enable bit allows direct control of the charge current source and the discharge device and also reflects the state of the discharge device. This bit is cleared by a reset of the device.

1 = If the ISEN bit is also set, the charge current source is sourcing current out of the PB0/AN0 pin. Writing a logic 1 enables the charging current out of the PB0/AN0 pin.

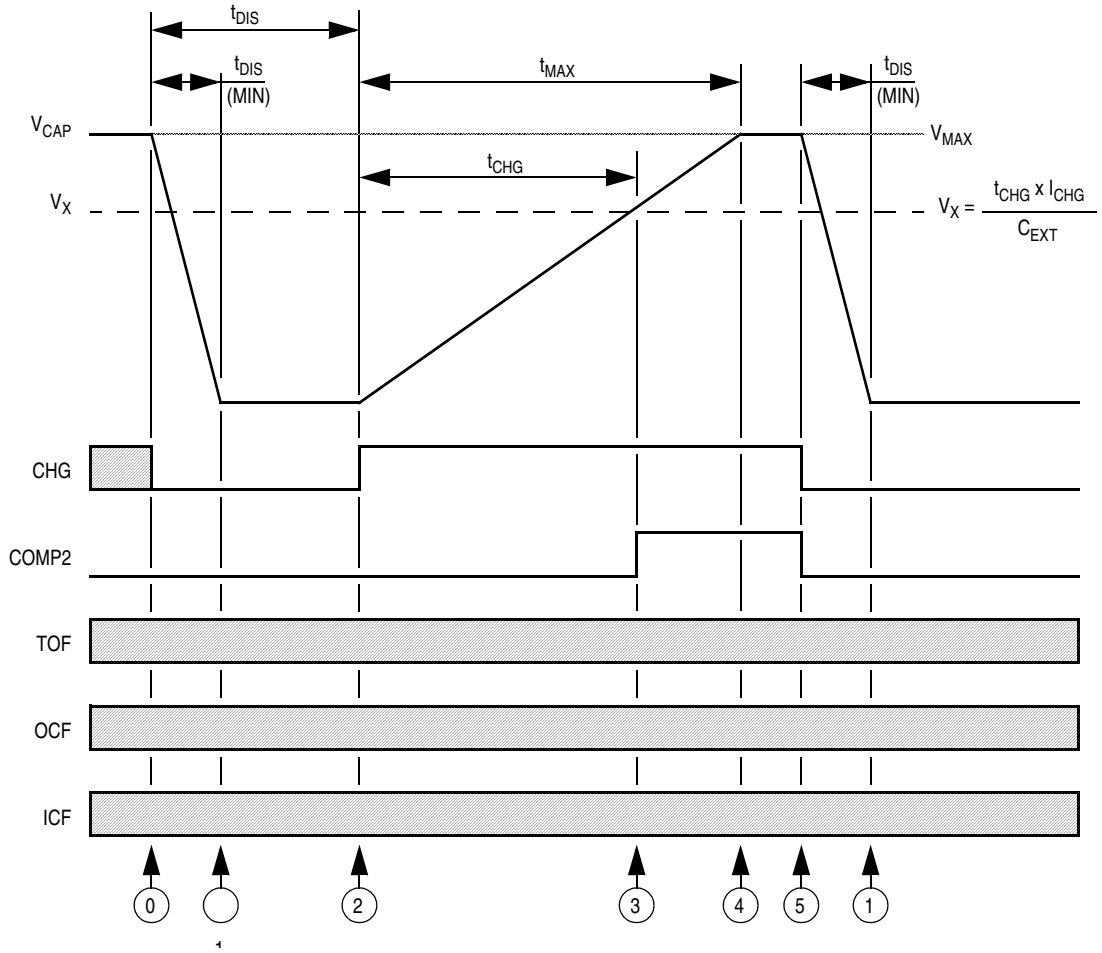
0 = The discharge device is sinking current into the PB0/AN0 pin. Writing a logic 0 disables the charging current and enables the discharging current into the PB0/AN0 pin, if the ISEN bit is also set.

ATD1–ATD2

The ATD1–ATD2 enable bits select one of the four operating modes used for making A/D conversions via the single-slope method.These four modes are given in Table 8-3. These bits have no effect if the ISEN enable bit is cleared. These bits are cleared by a reset of the device and thereby return the analog subsystem to the manual A/D conversion method.

Table 8-3. A/D Conversion Options

A/D Option Mode	Charge Control	A/D Options				Current Flow to/from PB0/AN0
		ISEN	ATD2	ATD1	CHG	
Disabled	Current source and discharge disabled	0	X	X	X	Current control disabled, no source or sink current
		1	0	0	1	Begin sourcing current when the CHG bit is set and continue to source current until the CHG bit is cleared.
		1	1	0	1	The CHG bit remains set until the next time ICF occurs.
3	Automatic charge and discharge (OCF–ICF) synchronized to timer	1	1	1	0	The CHG bit remains cleared until the next time OCF occurs.
		1	1	1	1	The CHG bit remains set until the next time ICF occurs.



Point	Action	Software/Hardware Action	Dependent Variable(s)
0	Begin initial discharge and select mode 0 by clearing the CHG, ATD2, and ATD1 control bits in the ACR.	Software write	Software
1	V_{CAP} falls to V_{SS}.	Wait out minimum t_{DIS} time.	V_{MAX}, I_{DIS}, C_{EXT}
2	Stop discharge and begin charge by setting CHG control bit in ACR.	Software write	Software
3	V_{CAP} rises to V_X and comparator 2 output trips, setting CPF2 and CMP2.	Wait out t_{CHG} time.	V_X, I_{CHG}, C_{EXT}
4	V_{CAP} reaches V_{MAX}.	None	V_{MAX}, I_{CHG}, C_{EXT}
5	Begin next discharge by clearing the CHG control bit in the ACR. Reset CPF2 by writing a 1 to CPFR2.	Software write	Software

Figure 8-8. A/D Conversion — Full Manual Control (Mode 0)

8.6 Voltage Measurement Methods

The methods for obtaining a voltage measurement can use software techniques to express these voltages as absolute or ratiometric readings.

In most applications the external capacitor, the clock source, the reference voltage, and the charging current may vary between devices and with changes in supply voltage or ambient temperature. All of these variations must be considered when determining the desired resolution of the measurement. The maximum and minimum extremes for the full scale count will be:

$$N_{FSMIN} = C_{EXTMIN} \times V_{FSMIN} \times f_{OSCMIN} / (P \times I_{CHGMAX})$$

$$N_{FSMAX} = C_{EXTMAX} \times V_{FSMAX} \times f_{OSCMAX} / (P \times I_{CHGMIN})$$

The minimum count should be the desired resolution, and the counting mechanism must be capable of counting to the maximum. The final scaling of the count will be by a math routine which calculates:

$$V_X = V_{REF} \times (N_X - N_{OFF}) / (N_{REF} - N_{OFF})$$

Where:

V_{REF} = Known reference voltage

V_X = Unknown voltage between V_{SS} and V_{REF}

N_X = Conversion count for unknown voltage

N_{REF} = Conversion count for known reference voltage (V_{REF})

N_{OFF} = Conversion count for minimum reference voltage (V_{SS})

When V_{REF} is a stable voltage source such as a zener or other reference source, then the unknown voltage will be determined as an absolute reading. If V_{REF} is the supply source to the device (V_{DD}), then the unknown voltage will be determined as a ratio of V_{DD}, or a ratiometric reading.

If the unknown voltage applied to the comparator is greater than its common-mode range (V_{DD} –1.5 volts), then the external capacitor will try to charge to the same level. This will cause both comparator inputs to be above the common-mode range and the output of the comparator will be indeterminate. In this case the comparator output flags may also be set even if the actual voltage on the positive input (+) is less than the voltage on the negative input (–). All A/D conversion methods should have a maximum time check to determine if this case is occurring.

Once the maximum timeout detection has been made, the state of the comparator outputs can be tested to determine the situation. However, such tests should be carefully designed when using modes 1, 2, or 3 as these modes cause the immediate automatic discharge of the external ramping capacitor before any software check can be made of the output state of comparator 2.

NOTE

All A/D conversion methods should include a test for a maximum elapsed time to detect error cases where the inputs may be outside of the design specification.

8.7 Voltage Comparator Features

The two internal comparators can be used as simple voltage comparators if set up as described in Table 8-8. Both comparators can be active in the wait mode and can directly restart the part by means of the analog interrupt. Both comparators can also be active in the stop mode, but cannot directly restart the part. However, the comparators can directly drive PB4 which can then be connected externally to activate either a port interrupt on the PA0:3 pins or the $\overline{IRQ}/V_{PP}$ pin.

Table 8-8. Voltage Comparator Setup Conditions

Comparator	Current Source Enable	Discharge Device Disable	Port B Pin as Inputs	Port B Pin Pulldowns Disabled	Prog. Timer Input Capture Source
1	Not affected	Not affected	DDRB2 = 0 DDRB3 = 0	PDIB2 = 1 PDIB3 = 1	Not affected
2	ISEN = 0	ISEN = 0	DDRB0 = 0 DDRB1 = 0	PDIB0 = 1 PDIB1 = 1	ICEN = 0 IEDG = 1

8.7.1 Voltage Comparator 1

Voltage comparator 1 is always connected to two of the port B I/O pins. These pins should be configured as inputs and have their software programmable pulldowns disabled. Also, the negative input of voltage comparator 1 is connected to the PB3/AN3/TCAP and shared with the input capture function of the 16-bit programmable timer. Therefore, the timer input capture interrupt should be disabled so that changes in the voltage on the PB3/AN3/TCAP pin do not cause unwanted input capture interrupts.

The output of comparator 1 can be connected to the port logic driving the PB4/AN4/TCMP/CMP1 pin such that the output of the comparator is ORed with the PB4 data bit and the OLVL bit from the 16-bit timer. This capability requires that the OPT bit is set in the COPR at location $1FF0 as in Figure 8-12, and the COE1 bit is set in the ASR at location $001E.

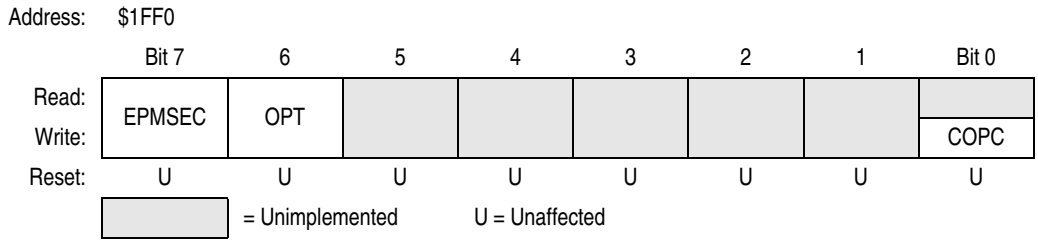


Figure 8-12. COP and Security Register (COPR)

OPT — Optional Features Bit

The OPT bit enables two additional features: direct drive by comparator 1 output to PB4 and voltage offset capability to sample capacitor in analog subsystem.

1 = Optional features enabled
0 = Optional features disabled

8.11 Port B Interaction with Analog Inputs

The analog subsystem is connected directly to the port B I/O pins without any intervening gates. It is, therefore, possible to measure the voltages on port B pins set as inputs or to have the analog voltage measurements corrupted by port B pins set as outputs.

8.12 Port B Pins as Inputs

All the port B pins will power up as inputs or return to inputs after a reset of the device since the bits in the port B data direction register will be reset.

If any port B pins are to be used for analog voltage measurements, they should be left as inputs. In this case, not only can the voltage on the pin be measured, but the logic state of the port B pins can be read from location $0002.

8.13 Port B Pulldowns

All the port B pins have internal software programmable pulldown devices available dependent on the state of the SWPDI bit in the mask option register (MOR).

If the pulldowns are enabled, they will create an approximate 100 µA load to any analog source connected to the pin. In some cases, the analog source may be able to supply this current without causing any error due to the analog source output impedance. Since this may not always be true, it is therefore best to disable port B pulldowns on those pins used for analog input sources.

8.14 Noise Sensitivity

In addition to the normal effects of electrical noise on the analog input signal there can also be other noise-related effects caused by the digital-to-analog interface. Since there is only one V_{SS} return for both the digital and the analog subsystems on the device, currents in the digital section may affect the analog ground reference within the device. This can add voltage offsets to measured inputs or cause channel-to-channel crosstalk.

To reduce the impact of these effects, there should be no switching of heavy I/O currents to or from the device while there is a critical analog conversion or voltage comparison in process. Limiting switched I/O currents to 2–4 mA during these times is recommended.

A noise reduction benefit can be gained with 0.1-µF bypass capacitors from each analog input (PB4:1) to the V_{SS} pin. Also, try to keep all the digital power supply or load currents from passing through any conductors which are the return paths for an analog signal.

9.2.2 Serial Data Input (SDI)

The SDI pin becomes an input as soon as the SIOP subsystem is enabled. New data is presented to the SDI pin on the falling edge of SCK. Valid data must be present at least 100 nanoseconds before the rising edge of SCK and remain valid for 100 nanoseconds after the rising edge of SCK. See Figure 9-3.

9.2.3 Serial Data Output (SDO)

The SDO pin becomes an output as soon as the SIOP subsystem is enabled. The state of the PB5/SDO pin reflects the value of the first bit received on the previous transmission. Prior to enabling the SIOP, the PB5/SDO can be initialized to determine the beginning state. While SIOP is enabled, the port B logic cannot be used as a standard output since that pin is connected to the last stage of the SIOP serial shift register. A control bit (LSBF) is included in the SCR to allow the data to be transmitted in either the MSB first format or the LSB first format.

The first data bit will be shifted out to the SDO pin on the first falling edge of the SCK. The remaining data bits will be shifted out to the SDI pin on subsequent falling edges of SCK. The SDO pin will present valid data at least 100 nanoseconds before the rising edge of the SCK and remain valid for 100 nanoseconds after the rising edge of SCK. See Figure 9-3.

9.3 SIOP Registers

The SIOP is programmed and controlled by the SIOP control register (SCR) located at address $000A, the SIOP status register (SSR) located at address $000B, and the SIOP data register (SDR) located at address $000C.

9.3.1 SIOP Control Register (SCR)

The SIOP control register (SCR) is located at address $000A and contains seven control bits and a write-only reset of the interrupt flag. Figure 9-4 shows the position of each bit in the register and indicates the value of each bit after reset.

Address: $000A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	SPIE	SPE	LSBF	MSTR	0	CPHA	SPR1	SPR0
Write:					SPIR			
Reset:	0	0	0	0	0	0	0	0

Figure 9-4. SIOP Control Register (SCR)

SPIE — Serial Peripheral Interrupt Enable Bit

The SPIE bit enables the SIOP to generate an interrupt whenever the SPIF flag bit in the SSR is set. Clearing the SPIE bit will not affect the state of the SPIF flag bit and will not terminate a serial interrupt once the interrupt sequence has started. Reset clears the SPIE bit.

1 = Serial interrupt enabled
0 = Serial interrupt disabled

NOTE

If the SPIE bit is cleared just after the serial interrupt sequence has started (for instance, the CPU status is being stacked), then the CPU will be unable

to determine the source of the interrupt and will vector to the reset vector as a default.

SPE — Serial Peripheral Enable Bit

The SPE bit switches the port B interface such that SDO/PB5 is the serial data output, SDI/PB6 is the serial data input, and SCK/PB7 is a serial clock input in the slave mode or a serial clock output in the master mode. The port B DDR and data registers can be manipulated as usual, but these actions will not affect the transmitted or received data. The SPE bit is readable and writable at any time, but clearing the SPE bit while a transmission is in progress will 1) abort the transmission, 2) reset the serial bit counter, and 3) convert port B to a general-purpose I/O port. Reset clears the SPE bit.

1 = Serial peripheral enabled (port B I/O disabled)
0 = Serial peripheral disabled (port B I/O enabled)

LSBF — Least Significant Bit First Bit

The LSBF bit controls the format of the transmitted and received data to be transferred LSB or MSB first. Reset clears this bit.

1 = LSB transferred first
0 = MSB transferred first

MSTR — Master Mode Select Bit

The MSTR bit configures the serial I/O port for master mode. A transfer is initiated by writing to the SDR. Also, the SCK pin becomes an output providing a synchronous data clock dependent upon the divider of the oscillator frequency selected by the SPR0:1 bits. When the device is in master mode, the SDO and SDI pins do not change function. These pins behave exactly the same in both the master and slave modes. The MSTR bit is readable and writable at any time regardless of the state of the SPE bit. Clearing the MSTR bit will abort any transfers that may have been in progress. Reset clears the MSTR bit, placing the SIOP subsystem in slave mode.

1 = SIOP set up as master, SCK is an output
0 = SIOP set up as slave, SCK is an input

SPIR — Serial Peripheral Interrupt Reset Bit

The SPIR bit is a write-only control to reset the SPIF flag bit in the SSR. Reading the SPIR bit will return a logic 0.

1 = Reset the SPIF flag bit
0 = No effect

CPHA — Clock Phase Bit

The CPHA bit controls the clock timing and phase in the SIOP. Data is changed on the falling edge of SCK and data is captured (read) on the rising edge of SCK. This bit is cleared by reset.

1 = SCK is idle low
0 = SCK is idle high

SPR0:1 — Serial Peripheral Clock Rate Select Bits

The SPR0 and SPR1 bits select one of four clock rates given in Table 9-1 to be supplied on the PB7/SCK pin when the device is configured with the SIOP as a master (MSTR = 1). The fastest rate is when both SPR0 and SPR1 are set. Both the SPR0 and SPR1 bits are cleared by reset, which places the SIOP clock selection at the slowest rate.

10.2 Core Timer Status and Control Register

The read/write core timer status and control register (CTSCR) contains the interrupt flag bits, interrupt enable bits, interrupt flag bit resets, and the rate selects for the real-time interrupt as shown in Figure 10-2.

Address: $0008

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CTOF	RTIF	CTOFE	RTIE	0	0	RT1	RT0
Write:					CTOFR	RTIFR		
Reset:	0	0	0	0	0	0	1	1

= Unimplemented

Figure 10-2. Core Timer Status and Control Register (CTSCR)

CTOF — Core Timer Overflow Flag

This read-only flag becomes set when the first eight stages of the core timer counter roll over from $FF to $00. The CTOF flag bit generates a timer overflow interrupt request if CTOFE is also set. The CTOF flag bit is cleared by writing a logic 1 to the CTOFR bit. Writing to CTOF has no effect. Reset clears CTOF.

1 = Overflow in core timer has occurred.
0 = No overflow of core timer since CTOF last cleared

RTIF — Real-Time Interrupt Flag

This read-only flag becomes set when the selected real-time interrupt (RTI) output becomes active. RTIF generates a real-time interrupt request if RTIE is also set. The RTIF enable bit is cleared by writing a logic 1 to the RTIFR bit. Writing to RTIF has no effect. Reset clears RTIF.

1 = Overflow in real-time counter has occurred.
0 = No overflow of real-time counter since RTIF last cleared

CTOFE — Core Timer Overflow Interrupt Enable Bit

This read/write bit enables core timer overflow interrupts. Reset clears CTOFE.

1 = Core timer overflow interrupts enabled
0 = Core timer overflow interrupts disabled

RTIE — Real-Time Interrupt Enable Bit

This read/write bit enables real-time interrupts. Reset clears RTIE.

1 = Real-time interrupts enabled
0 = Real-time interrupts disabled

CTOFR — Core Timer Overflow Flag Reset Bit

Writing a logic 1 to this write-only bit clears the CTOF bit. CTOFR always reads as a logic 0. Reset does not affect CTOFR.

1 = Clear CTOF flag bit
0 = No effect on CTOF flag bit

RTIFR — Real-Time Interrupt Flag Reset Bit

Writing a logic 1 to this write-only bit clears the RTIF bit. RTIFR always reads as a logic 0. Reset does not affect RTIFR.

1 = Clear RTIF flag bit
0 = No effect on RTIF flag bit

RT1 and RT0 — Real-Time Interrupt Select Bits 1 and 0

These read/write bits select one of four real-time interrupt rates, as shown in Table 10-1. Because the selected RTI output drives the COP watchdog, changing the real -time interrupt rate also changes the

periodically by a program sequence. Writing a logic 0 to COPC bit in the COPR register clears the COP watchdog and prevents a COP reset.

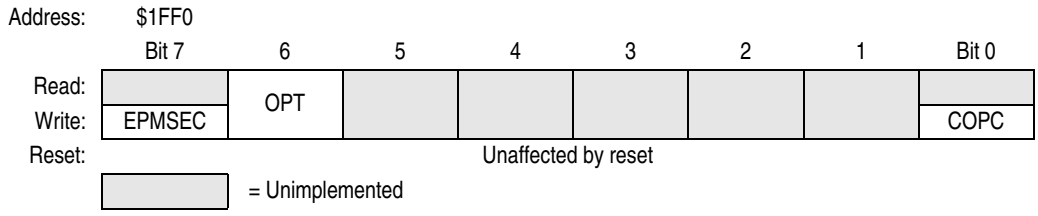


Figure 10-4. COP and Security Register (COPR)

EPMSEC — EPROM Security((1)) Bit

The EPMSEC bit is a write-only security bit to protect the contents of the user EPROM code stored in locations $0700–$1FFF.

OPT — Optional Features Bit

The OPT bit enables two additional features: direct drive by comparator outputs to port A and voltage offset capability to sample capacitor in analog subsystem.

1 = Optional features enabled
0 = Optional features disabled

COPC — COP Clear Bit

This write-only bit resets the COP watchdog. The COP watchdog is active in the run, wait, and halt modes of operation if the COP is enabled by setting the COPEN bit in the MOR. The STOP instruction disables the COP watchdog by clearing the counter and turning off its clock source.

In applications that depend on the COP watchdog, the STOP instruction can be disabled by setting the SWAIT bit in the MOR. In applications that have wait cycles longer than the COP timeout period, the COP watchdog can be disabled by clearing the COPEN bit. Table 10-2 summarizes recommended conditions for enabling and disabling the COP watchdog.

NOTE

If the voltage on the $\overline{IRQ}/V_{PP}$ pin exceeds $1.5 \times V_{DD}$, the COP watchdog turns off and remains off until the $\overline{IRQ}/V_{PP}$ pin voltage falls below $1.5 \times V_{DD}$.

Table 10-2. COP Watchdog Recommendations

Voltage on $\overline{IRQ}/V_{PP}$ Pin	SWAIT (in MOR)(1)	Wait/Halt Time	Recommended COP Watchdog Condition
Less than $1.5 \times V_{DD}$	1	Less than COP timeout period	Enabled(2)
Less than $1.5 \times V_{DD}$	1	Greater than COP timeout period	Disabled
Less than $1.5 \times V_{DD}$	0	X(3)	Disabled
More than $1.5 \times V_{DD}$	X	X(3)	Disabled

1. The SWAIT bit in the MOR converts STOP instructions to HALT instructions.
2. Reset the COP watchdog immediately before executing the WAIT/HALT instruction.
3. Don't care

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the EPROM/OTPROM difficult for unauthorized users.

11.2 Timer Registers

The functional block diagram of the 16-bit free-running timer counter and timer registers is shown in Figure 11-2. The timer registers include a transparent buffer latch on the LSB of the 16-bit timer counter.

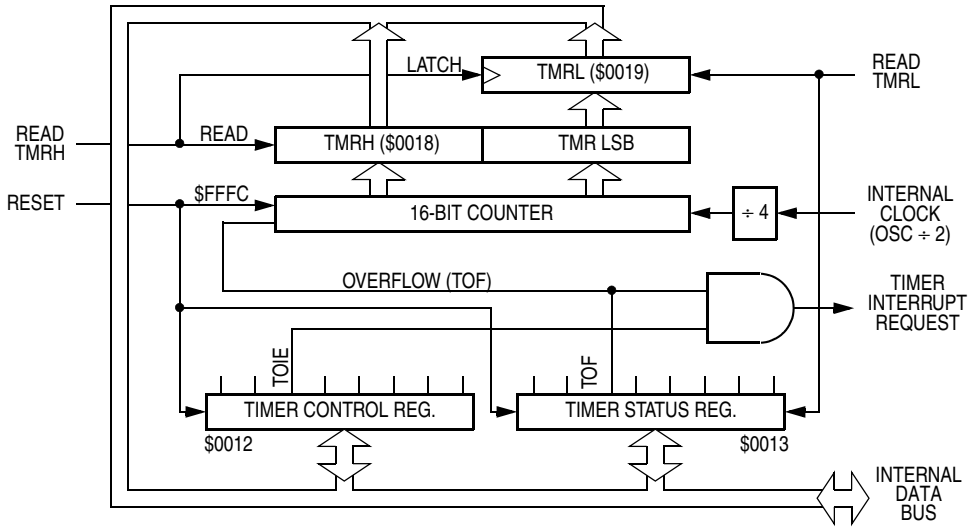


Figure 11-2. Programmable Timer Block Diagram

The timer registers (TMRH and TMRL) shown in Figure 11-3 are read-only locations which contain the current high and low bytes of the 16-bit free-running counter. Writing to the timer registers has no effect. Reset of the device presets the timer counter to $FFFC.

The TMRL latch is a transparent read of the LSB until a read of the TMRH takes place. A read of the TMRH latches the LSB into the TMRL location until the TMRL is again read. The latched value remains fixed even if multiple reads of the TMRH take place before the next read of the TMRL. Therefore, when reading the MSB of the timer at TMRH, the LSB of the timer at TMRL must also be read to complete the read sequence.

During power-on reset (POR), the counter is initialized to $FFFC and begins counting after the oscillator startup delay. Because the counter is 16 bits and preceded by a fixed prescaler, the value in the counter repeats every 262,144 internal bus clock cycles (524,288 oscillator cycles).

Address: $0018

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 15	14	13	12	11	10	9	Bit 8
Write:								
Reset:	1	1	1	1	1	1	1	1

Address: $0018

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	6	5	4	3	2	1	Bit 0
Write:								
Reset:	1	1	1	1	1	1	0	0

= Unimplemented

Figure 11-3. Programmable Timer Registers (TMRH and TMRL)

ELAT — EPROM Bus Latch Bit

This read/write bit configures address and data buses for programming the EPROM array. EPROM data cannot be read when ELAT is set. Clearing the ELAT bit also clears the EPGM bit. Reset clears ELAT.

1 = Address and data buses configured for EPROM programming of the array. The address and data buses are latched in the EPROM array when a subsequent write to the array is made. Data in the EPROM array cannot be read.

0 = Address and data buses configured for normal operation

Whenever the ELAT bit is cleared, the EPGM bit is also cleared. Both the EPGM and the ELAT bit cannot be set using the same write instruction. Any attempt to set both the ELAT and EPGM bit on the same write instruction cycle will result in the ELAT bit being set and the EPGM bit being cleared. To program a byte of EPROM, manipulate the EPROG register as follows:

1. Set the ELAT bit in the EPROG register.
2. Write the desired data to the desired EPROM address.
3. Set the EPGM bit in the EPROG register for the specified programming time, t_{EPGM}.
4. Clear the ELAT and EPGM bits in the EPROG register.

13.2.2 Mask Option Register

The mask option register (MOR) shown in Figure 13-2 is an EPROM byte that controls eight mask options. The MOR is unaffected by reset. The erased state of the MOR is $00. The options that can be programmed by the MOR are:

1. Port software programmable pulldown devices (enable or disable)
2. Startup delay after stop (16 or 4064 cycles)
3. Oscillator shunt resistor (2 MΩ or open)
4. STOP instruction (enable or disable)
5. Low-voltage reset (enable or disable)
6. Port A external interrupt function (enable or disable)
7. IRQ trigger sensitivity (edge-triggered only or both edge- and level-triggered)
8. COP watchdog (enable or disable)

Address: $1FF1

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SWPDI	DELAY	OSCRES	SWAIT	LVREN	PIRQ	LEVEL	COPEN
Reset:	Unaffected by reset							
Erased:	0	0	0	0	0	0	0	0

Figure 13-2. Mask Option Register (MOR)

SWPDI — Software Pulldown Inhibit Bit

This EPROM bit inhibits software control of the port A and port B pulldown devices.

1 = Software pulldown inhibited

0 = Software pulldown enabled

DELAY — Stop Startup Delay Bit

This EPROM bit selects the number of bus cycles that must elapse before bus activity begins following a restart from the stop mode.

1 = Startup delay is 4064 bus cycles.
0 = Startup delay is 16 bus cycles.

CAUTION

The 16-cycle delay option will work properly in devices with the internal low-power oscillator or with a steady external clock source. Check crystal/ceramic resonator specifications carefully before using the 16-cycle delay option with a crystal or ceramic resonator.

OSCRES — Oscillator Resistor Bit

This EPROM bit configures the internal shunt resistor.

1 = Oscillator configured with 2 M¾ shunt resistor
0 = Oscillator configured without a shunt resistor

NOTE

The optional oscillator resistor is NOT recommended for devices that use an external RC oscillator. For such devices, this bit should be left erased as a 0.

SWAIT — STOP Conversion to WAIT Bit

This EPROM bit disables the STOP instruction and prevents inadvertently turning off the COP watchdog with a STOP instruction. When the SWAIT bit is set, a STOP instruction puts the MCU in halt mode. Halt mode is a wait-like low-power state. The internal oscillator and timer clock continue to run, but the CPU clock stops. When the SWAIT bit is clear, a STOP instruction stops the internal oscillator, the internal clock, the CPU clock, the timer clock, and the COP watchdog timer.

1 = STOP instruction converted to WAIT instruction
0 = STOP instruction not converted to WAIT instruction

LVREN — Low-Voltage Reset Enable Bit

This EPROM bit enables the low-voltage reset (LVR) function.

1 = LVR function enabled
0 = LVR function disabled

PIRQ — Port A IRQ Enable Bit

This EPROM bit enables the PA3–PA0 pins to function as external interrupt sources.

1 = PA3–PA0 enabled as external interrupt sources
0 = PA3–PA0 not enabled as external interrupt sources

LEVEL — External Interrupt Sensitivity Bit

This EPROM bit makes the external interrupt inputs level-triggered as well as edge-triggered

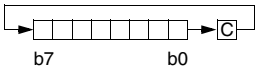
1 = $\overline{IRQ}/V_{PP}$ pin negative-edge triggered and low-level triggered;
PA3–PA0 pins positive-edge triggered and high-level triggered
0 = $\overline{IRQ}/V_{PP}$ pin negative-edge triggered only; PA3–PA0 pins positive-edge triggered only

COPEN — COP Watchdog Enable Bit

This EPROM bit enables the COP watchdog.

1 = COP watchdog enabled
0 = COP watchdog disabled

Table 14-6. Instruction Set Summary (Sheet 5 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
ROR *opr* RORA RORX ROR *opr*,X ROR ,X	Rotate Byte Right through Carry Bit		—	—	↕	↕	↕	DIR INH INH IX1 IX	36 46 56 66 76	dd ff 	5 3 3 6 5
RSP	Reset Stack Pointer	SP ← $00FF	—	—	—	—	—	INH	9C		2
RTI	Return from Interrupt	SP ← (SP) + 1; Pull (CCR) SP ← (SP) + 1; Pull (A) SP ← (SP) + 1; Pull (X) SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	↕	↕	↕	↕	þ	INH	80		6
RTS	Return from Subroutine	SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)						INH			
SBC #*opr* SBC *opr* SBC *opr* SBC *opr*,X SBC *opr*,X SBC ,X	Subtract Memory Byte and Carry Bit from Accumulator	A ← (A) – (M) – (C)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A2 B2 C2 D2 E2 F2	ii dd hh ll ee ff ff 	2 3 4 5 4 3
SEC	Set Carry Bit	C ← 1	—	—	—	—	1	INH	99		2
SEI	Set Interrupt Mask	I ← 1	—	1	—	—	—	INH	9B		2
STA *opr* STA *opr* STA *opr*,X STA *opr*,X STA ,X	Store Accumulator in Memory	M ← (A)	—	—	↕	↕	—	DIR EXT IX2 IX1 IX	B7 C7 D7 E7 F7	dd hh ll ee ff ff 	4 5 6 5 4
STOP	Stop Oscillator and Enable $\overline{\text{IRQ}}$ Pin		—	0	—	—	—	INH	8E		2
STX *opr* STX *opr* STX *opr*,X STX *opr*,X STX ,X	Store Index Register In Memory	M ← (X)	—	—	↕	↕	—	DIR EXT IX2 IX1 IX	BF CF DF EF FF	dd hh ll ee ff ff 	4 5 6 5 4
SUB #*opr* SUB *opr* SUB *opr* SUB *opr*,X SUB *opr*,X SUB ,X	Subtract Memory Byte from Accumulator	A ← (A) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A0 B0 C0 D0 E0 F0	ii dd hh ll ee ff ff 	2 3 4 5 4 3
SWI	Software Interrupt	PC ← (PC) + 1; Push (PCL) SP ← (SP) – 1; Push (PCH) SP ← (SP) – 1; Push (X) SP ← (SP) – 1; Push (A) SP ← (SP) – 1; Push (CCR) SP ← (SP) – 1; I ← 1 PCH ← Interrupt Vector High Byte PCL ← Interrupt Vector Low Byte	—	1	—	—	—	INH	83		10

15.12 Control Timing (3.0 Vdc)

Characteristic[1]	Symbol	Min	Max	Unit
Frequency of oscillation (OSC)				
RC oscillator option	f_{OSC}	—	2.1	MHz
Crystal oscillator option		0.1	2.1	MHz
External clock source		dc	2.1	MHz
Internal low-power oscillator				
Standard product (100 kHz nominal)		60	140	kHz
Mask option (500 kHz nominal, see Note 3))		300	700	kHz
Internal operating frequency, crystal, or external clock ($f_{OSC}/2$)				
RC oscillator option	f_{OP}	—	1.05	MHz
Crystal oscillator option		0.05	1.05	MHz
External clock source		dc	1.05	MHz
Internal low-power oscillator				
Standard product (100 kHz nominal)		30	70	kHz
Mask option (500 kHz nominal[2])		150	350	kHz
Cycle time ($1/f_{OP}$)				
External oscillator or clock source	t_{cyc}	952	—	ns
Internal low-power oscillator				
Standard product (100 kHz nominal)		14.29	33.33	µs
Mask option (500 kHz nominal[2])		2.86	6.67	µs
16-bit timer				
Resolution	t_{RESL}	4.0	—	t_{cyc}
Input capture (TCAP) pulse width	t_{TH}, t_{TL}	284	—	ns
Interrupt pulse width low (edge-triggered)	t_{ILIH}	284	—	ns
Interrupt pulse period	t_{ILIL}	[3]	—	t_{cyc}
OSC1 pulse width (external clock input)	t_{OH}, t_{OL}	110	—	ns
Analog subsystem response				
Voltage comparators				
Switching time (10 mV overdrive, either input)	t_{CPROP}	—	2	µs
Comparator power-up delay (bias circuit already powered up)	t_{CDELAY}	—	2	µs
External current source (PB0/AN0)				
Switching time (I_{DIS} to I_{RAMP})	t_{ISTART}	—	1	µs
Power-up delay (bias circuit already powered up)	t_{IDELAY}	—	2	µs
Bias circuit power-up delay	t_{BDELAY}	—	2	µs

1. $+2.7 \le V_{DD} \le +3.3$ V, $V_{SS} = 0$ V, $T_L \le T_A \le T_H$, unless otherwise noted
2. The 500 kHz nominal mask option is available through special order only. Contact your local Freescale sales representative for detailed ordering information. Not offered with the RC oscillator option.
3. The minimum period, t_{ILIL}, should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{cyc}.

15.14 SIOP Timing (V_{DD} = 5.0 Vdc)

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Frequency of operation Master Slave	 $f_{SIOP(M)}$ $f_{SIOP(S)}$	 0.25 x f_{OP} dc	 0.25 x f_{OP} —	 0.25 x f_{OP} 1050	kHz
Cycle time Master Slave	 $t_{SCK(M)}$ $t_{SCK(M)}$	 4.0 x t_{cyc} —	 4.0 x t_{cyc} —	 4.0 x t_{cyc} 3.8	µs
Clock (SCK) low time (f_{OP} = 4.2 MHz)	t_{SCKL}	952	—	—	ns
SDO data valid time	t_V	—	—	200	ns
SDO hold time	t_{HO}	0	—	—	ns
SDI setup time	t_S	100	—	—	ns
SDI hold time	t_H	100	—	—	ns

1. +4.5 ≤ V_{DD} ≤ +5.5 V, V_{SS} = 0 V, $T_L \le T_A \le T_H$, unless otherwise noted

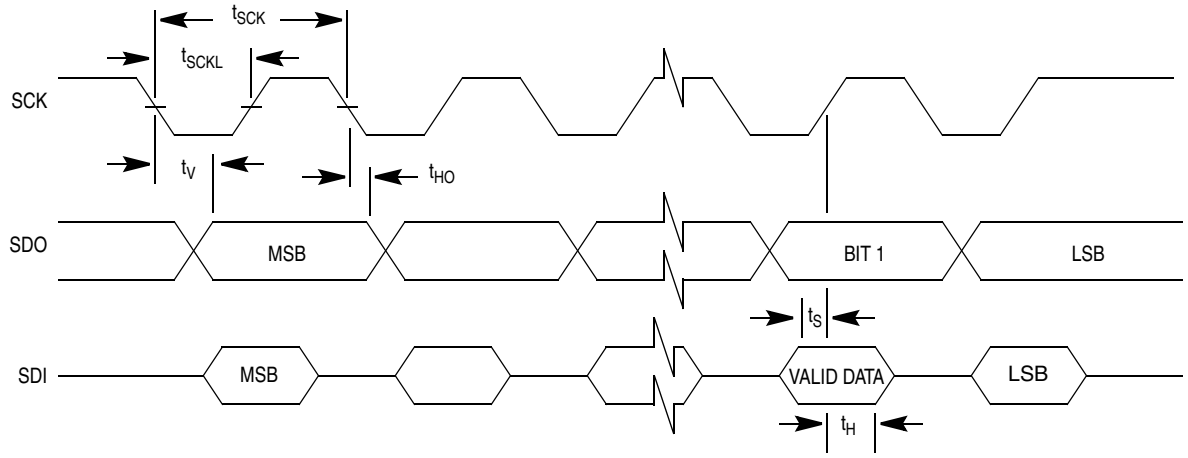


Figure 15-11. SIOP Timing Diagram