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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SIO
Peripherals	POR, Temp Sensor, WDT
Number of I/O	22
Program Memory Size	6KB (6K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	224 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcr705jp7cdwe

MC68HC705JJ7 MC68HRC705SJ7
MC68HC705SJ7 MC68HC705JP7
MC68HRC705JJ7 MC68HC705SP7

Advance Information Data Sheet

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://www.freescale.com/

Chapter 1
General Description

1.1 Introduction

The MC68HC705JJ7 and MC68HC705JP7 are erasable programmable read-only memory (EPROM) versions of the MC68HC05JJ/JP Family of microcontrollers (MCU).

1.2 Features

Features of the two parts include:

- Low-cost, M68HC05 core MCU in 20-pin package (MC68HC705JJ7) or 28-pin package (MC68HC705JP7)
- 6160 bytes of user EPROM, including 16 bytes of user vectors
- 224 bytes of low-power user random-access memory (RAM)
- 64 bits of personality EPROM (serial access)
- 16-bit programmable timer with input capture and output compare
- 15-stage core timer, including 8-bit free-running counter and 4-stage selectable real-time interrupt generator
- Simple serial input/output port (SIOP) with interrupt capability
- Two voltage comparators, one of which can be combined with the 16-bit programmable timer to create a 4-channel, single-slope analog-to-digital (A/D) converter
- Output of voltage comparator can drive port pin PB4 directly under software control
- 14 input/output (I/O) lines (MC68HC705JJ7) or 22 I/O lines (MC68HC705JP7), including high-source/sink current capability on 6 I/O pins (MC68HC705JJ7) or 14 I/O pins (MC68HC705JP7)
- Programmable 8-bit mask option register (MOR) to select mask options found in read-only memory (ROM) based versions
- MOR selectable software programmable pulldowns on all I/O pins and keyboard scan interrupt on four I/O pins
- Software mask and request bit for IRQ interrupt with MOR selectable sensitivity on IRQ interrupt (edge- and level-sensitive or edge-only)
- On-chip oscillator with device option of crystal/ceramic resonator or resistor-capacitor (RC) operation and MOR selectable shunt resistor, 2 MΩ by design
- Internal oscillator for lower-power operation, approximately 100 kHz (500 kHz selected as device option)
- EPROM security bit[1] to aid in locking out access to programmable EPROM array
- MOR selectable computer operating properly (COP) watchdog system

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the EPROM/OTPROM difficult for unauthorized users.

Address	Register Name
$0000	Port A Data Register
$0001	Port B Data Register
$0002	Port C Data Register *
$0003	Analog MUX Register
$0004	Port A Data Direction Register
$0005	Port B Data Direction Register
$0006	Port C Data Direction Register *
$0007	Unused
$0008	Core Timer Status & Control Register
$0009	Core Timer Counter
$000A	Serial Control Register
$000B	Serial Status Register
$000C	Serial Data Register
$000D	IRQ Status & Control Register
$000E	Personality EPROM Bit Select Register
$000F	Personality EPROM Status & Control Register
$0010	Port A and Port C Pulldown Register *
$0011	Port B Pulldown Register
$0012	Timer Control Register
$0013	Timer Status Register
$0014	Input Capture Register (MSB)
$0015	Input Capture Register (LSB)
$0016	Output Compare Register (MSB)
$0017	Output Compare Register (LSB)
$0018	Timer Counter Register (MSB)
$0019	Timer Counter Register (LSB)
$001A	Alternate Counter Register (MSB)
$001B	Alternate Counter Register (LSB)
$001C	EPROM Programming Register
$001D	Analog Control Register
$001E	Analog Status Register
$001F	Reserved

* Features related to port C are only available on the 28-pin MC68HC705JP7 devices.

Figure 2-2. I/O Registers

3.6 Condition Code Register

The condition code register is an 8-bit register whose three most significant bits are permanently fixed at 111 as shown in Figure 3-6. The condition code register contains the interrupt mask and four flags that indicate the results of the instruction just executed. The following paragraphs describe the functions of the condition code register.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	1	1	1	H	I	N	C	Z
Write:								
Reset:	1	1	1	U	1	U	U	U

U = Unaffected

Figure 3-6. Condition Code Register (CCR)

Half-Carry Flag (H)

The CPU sets the half-carry flag when a carry occurs between bits 3 and 4 of the accumulator during an ADD or ADC operation. The half-carry flag is required for binary coded decimal (BCD) arithmetic operations. Reset has no effect on the half-carry flag.

Interrupt Mask (I)

Setting the interrupt mask disables interrupts. If an interrupt request occurs while the interrupt mask is a logic 0, the CPU saves the CPU registers on the stack, sets the interrupt mask, and then fetches the interrupt vector. If an interrupt request occurs while the interrupt mask is set, the interrupt request is latched. The CPU processes the latched interrupt as soon as the interrupt mask is cleared again. A return-from-interrupt (RTI) instruction pulls the CPU registers from the stack, restoring the interrupt mask to its cleared state. After a reset, the interrupt mask is set and can be cleared only by a CLI instruction.

Negative Flag (N)

The CPU sets the negative flag when an arithmetic operation, logical operation, or data manipulation produces a negative result. Reset has no affect on the negative flag.

Zero Flag (Z)

The CPU sets the zero flag when an arithmetic operation, logical operation, or data manipulation produces a result of $00. Reset has no affect on the zero flag.

Carry/Borrow Flag (C)

The CPU sets the carry/borrow flag when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some logical operations and data manipulation instructions also clear or set the carry/borrow flag. Reset has no effect on the carry/borrow flag.

3.7 Arithmetic/Logic Unit (ALU)

The ALU performs the arithmetic and logical operations defined by the instruction set. The binary arithmetic circuits decode instructions and set up the ALU for the selected operation. Most binary arithmetic is based on the addition algorithm, carrying out subtraction as negative addition. Multiplication is not performed as a discrete operation but as a chain of addition and shift operations within the ALU. The multiply instruction (MUL) requires 11 internal clock cycles to complete this chain of operations.

Therefore, the lowest power is consumed when OM1 is cleared. The state with both OM1 and OM2 set is provided so that the EPO can be started and allowed to stabilize while the LPO still clocks the MCU. The reset state is for OM1 to be cleared and OM2 to be set, which selects the LPO and disables the EPO.

IRQF — External Interrupt Request Flag

The IRQ flag is a clearable, read-only bit that is set when an external interrupt request is pending. Writing to the IRQF bit has no effect. Reset clears the IRQF bit.

1 = Interrupt request pending
0 = No interrupt request pending

The following conditions set the IRQ flag:

- An external interrupt signal on the $\overline{IRQ}/V_{PP}$ pin
- An external interrupt signal on pin PA0, PA1, PA2, or PA3
  when the PA0–PA3 pins are enabled by the PIRQ bit in the MOR to serve as external interrupt sources.

The following conditions clear the IRQ flag:

- When the CPU fetches the interrupt vector
- When a logic 1 is written to the IRQR bit

IRQR — Interrupt Request Reset Bit

This write-only bit clears the IRQF flag bit and prevents redundant execution of interrupt routines. Writing a logic 1 to IRQR clears the IRQF. Writing a logic 0 to IRQR has no effect. IRQR always reads as a logic 0. Reset has no effect on IRQR.

1 = Clear IRQF flag bit
0 = No effect

4.6 Core Timer Interrupts

The core timer can generate the following interrupts:

- Timer overflow interrupt
- Real-time interrupt

Setting the I bit in the condition code register disables core timer interrupts. The controls and flags for these interrupts are in the core timer status and control register (CTSCR) located at $0008.

4.6.1 Core Timer Overflow Interrupt

An overflow interrupt request occurs if the core timer overflow flag (TOF) becomes set while the core timer overflow interrupt enable bit (TOFE) is also set. The TOF flag bit can be reset by writing a logic 1 to the CTOFR bit in the CTSCR or by a reset of the device.

4.6.2 Real-Time Interrupt

A real-time interrupt request occurs if the real-time interrupt flag (RTIF) in the CTSCR becomes set while the real-time interrupt enable bit (RTIE) is also set. The RTIF flag bit can be reset by writing a logical 1 to the RTIFR bit in the CTSCR or by a reset of the device.

Chapter 5
Resets

5.1 Introduction

This section describes the five reset sources and how they initialize the microcontroller unit (MCU). A reset immediately stops the operation of the instruction being executed, initializes certain control bits, and loads the program counter with a user-defined reset vector address. These conditions produce a reset:

- Initial power-up of device (power-on reset)
- A logic 0 applied to the $\overline{\text{RESET}}$ pin (external reset)
- Timeout of the computer operating properly (COP) watchdog (COP reset)
- Low voltage applied to the device (LVR reset)
- Fetch of an opcode from an address not in the memory map (illegal address reset)

Figure 5-1 shows a block diagram of the reset sources and their interaction.

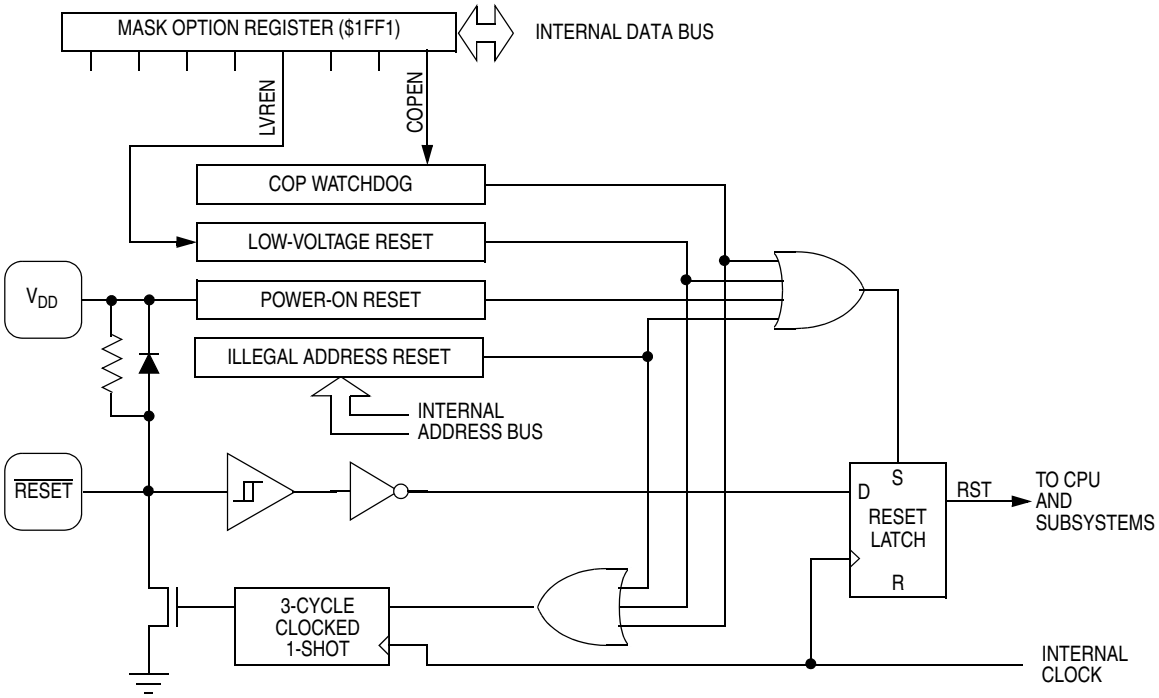

Figure 5-1. Reset Sources

5.4.2 Computer Operating Properly (COP) Reset

A timeout of the COP watchdog generates a COP reset. The COP watchdog is part of a software error detection system and must be cleared periodically to start a new timeout period. To clear the COP watchdog and prevent a COP reset, write a logic 0 to the COPC bit of the COPR register at location $1FF0. The COPC bit, shown in Figure 5-2, is a write-only bit.

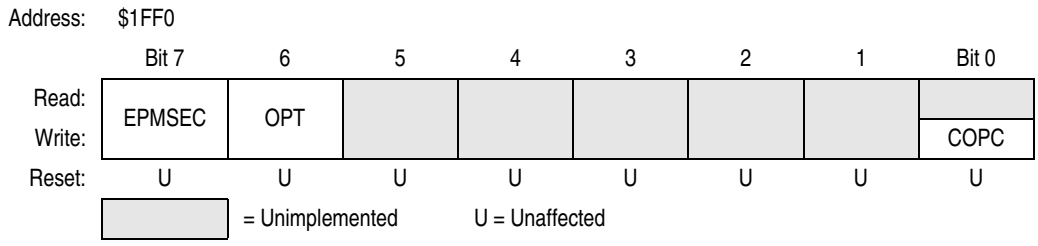

Figure 5-2. COP and Security Register (COPR)

EPMSEC — EPROM Security[1] Bit

The EPMSEC bit is an EPROM, write-only security bit to protect the contents of the user EPROM code stored in locations $0700–$1FFF.

OPT — Optional Features Bit

The OPT bit enables two additional features: direct drive by comparator 1 output to PB4 and voltage offset capability to sample capacitor in analog subsystem.

1 = Optional features enabled
0 = Optional features disabled

NOTE

See 8.7.1 Voltage Comparator 1 and 8.10 Sample and Hold for further descriptions of the OPT bit.

COPC — COP Clear Bit

COPC is a write-only bit. Periodically writing a logic 0 to COPC prevents the COP watchdog from resetting the MCU. Reset clears the COPC bit.

1 = No effect on COP watchdog timer
0 = Reset COP watchdog timer

The COP watchdog reset will assert the pulldown device to pull the $\overline{\text{RESET}}$ pin low for three to four cycles of the internal bus.

The COP watchdog reset function can be enabled or disabled by programming the COPEN bit in the MOR.

5.4.3 Low-Voltage Reset (LVR)

The LVR activates the RST reset signal to reset the device when the voltage on the V_{DD} pin falls below the LVR trip voltage. The LVR will assert the pulldown device to pull the $\overline{\text{RESET}}$ pin low for three to four cycles of the internal bus.

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the EPROM/OTPROM difficult for unauthorized users.

6.3.1 Stop Mode

The STOP instruction puts the MCU in a mode with the lowest power consumption and affects the MCU as follows:

- Turns off the central processor unit (CPU) clock and all internal clocks by stopping both the external pin oscillator and the internal low-power oscillator. The selection of the oscillator by the OM1 and OM2 bits in the ISCR is not affected. The stopped clocks turn off the COP watchdog, the core timer, the programmable timer, the analog subsystem, and the SIOP.
- Removes any pending core timer interrupts by clearing the core timer interrupt flags (CTOF and RTIF) in the core timer status and control register (CTSCR)
- Disables any further core timer interrupts by clearing the core timer interrupt enable bits (CTOFE and RTIE) in the CTSCR
- Removes any pending programmable timer interrupts by clearing the timer interrupt flags (ICF, OCF, and TOF) in the timer status register (TSR)
- Disables any further programmable timer interrupts by clearing the timer interrupt enable bits (ICIE, OCIE, and TOIE) in the timer control register (TCR)
- Enables external interrupts via the $\overline{IRQ}/V_{PP}$ pin by setting the IRQE bit in the IRQ status and control register (ISCR). External interrupts are also enabled via the PA0 through PA3 pins, if the port A interrupts are enabled by the PIRQ bit in the mask option register (MOR).
- Enables interrupts in general by clearing the I bit in the condition code register

The STOP instruction does not affect any other bits, registers, or I/O lines.

The following conditions bring the MCU out of stop mode:

- An external interrupt signal on the $\overline{IRQ}/V_{PP}$ pin — A high-to-low transition on the $\overline{IRQ}/V_{PP}$ pin loads the program counter with the contents of locations $1FFA and $1FFB.
- An external interrupt signal on a port A external interrupt pin — If selected by the PIRQ bit in the MOR, a low-to-high transition on a PA3–PA0 pin loads the program counter with the contents of locations $1FFA and $1FFB.
- External reset — A logic 0 on the $\overline{RESET}$ pin resets the MCU and loads the program counter with the contents of locations $1FFE and $1FFF.

When the MCU exits stop mode, processing resumes after a stabilization delay of 16 or 4064 internal bus cycles, depending on the state of the DELAY bit in the MOR.

NOTE

Execution of the STOP instruction without setting the SWAIT bit in the MOR will cause the oscillators to stop, and, therefore, disable the COP watchdog timer. If the COP watchdog timer is to be used, stop mode should be changed to halt mode as described in 6.3.3 Halt Mode.

6.3.4 Data-Retention Mode

In the data-retention mode, the MCU retains random-access memory (RAM) contents and CPU register contents at V_{DD} voltages as low as 2.0 Vdc. The data retention feature allows the MCU to remain in a low-power consumption state during which it retains data, but the CPU cannot execute instructions. Current consumption in this mode is not tested.

To put the MCU in the data retention mode:

1. Drive the $\overline{\text{RESET}}$ pin to a logic 0.
2. Lower the V_{DD} voltage. The $\overline{\text{RESET}}$ pin must remain low continuously during data retention mode.

To take the MCU out of the data retention mode:

1. Return V_{DD} to normal operating voltage.
2. Return the $\overline{\text{RESET}}$ pin to a logic 1.

7.3.7 PB5/SDO Logic

The PB5/SDO pin can be used as a simple I/O port pin or be controlled by the SIOP serial interface as shown in Figure 7-10. The operations of the PB5 pin are summarized in Table 7-3.

When using the PB5/SDO pin, these interactions must be noted:

1. If the SIOP function is required, then the SPE bit in the SCR must be set. This causes the PB5/SDO pin buffer to be enabled and to be driven by the serial data output (SDO) from the SIOP. The pulldown device will be disabled in this case.
2. If the SIOP function is in control of the PB5/SDO pin, the DDRB5 and PB5 data register bits are still accessible to the CPU and can be altered or read without affecting the SIOP functionality. However, if the DDRB5 bit is cleared, reading the PB5 data register will return the current state of the PB5/SDO pin.

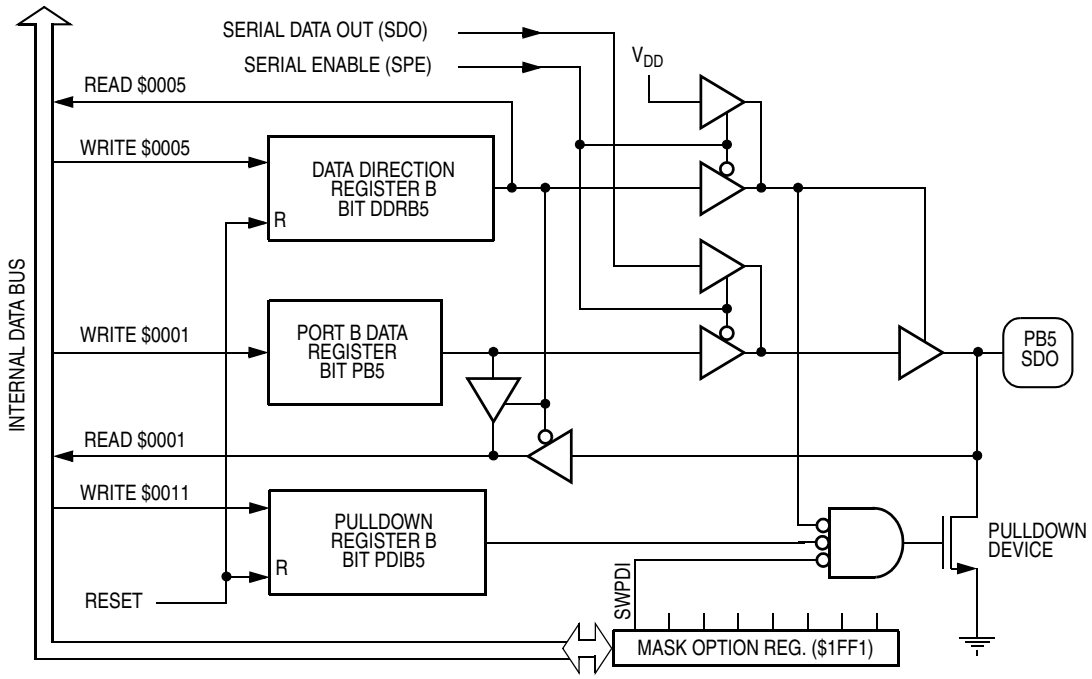

Figure 7-10. PB5/SDO Pin I/O Circuit

3. If the SIOP function is terminated by clearing the SPE bit in the SCR, then the last conditions stored in the DDRB5, PDIB5, and PB5 register bits will then control the PB5/SDO pin.
4. If the PB5/SDO pin is to be a digital input, then both the SPE bit in the SCR and the DDRB5 bit must be cleared. Depending on the external application, the pulldown device may also be disabled by setting the PDIB5 pulldown inhibit bit.
5. If the PB5/SDO pin is to be a digital output, then the SPE bit in the SCR must be cleared and the PDIB5 bit must be set. The pulldown device will be disabled in this case.

7.3.9 PB7/SCK Logic

The PB7/SCK pin can be used as a simple I/O port pin or be controlled by the SIOP serial interface as shown in Figure 7-12. The operations of the PB7/SCK pin are summarized in Table 7-3.

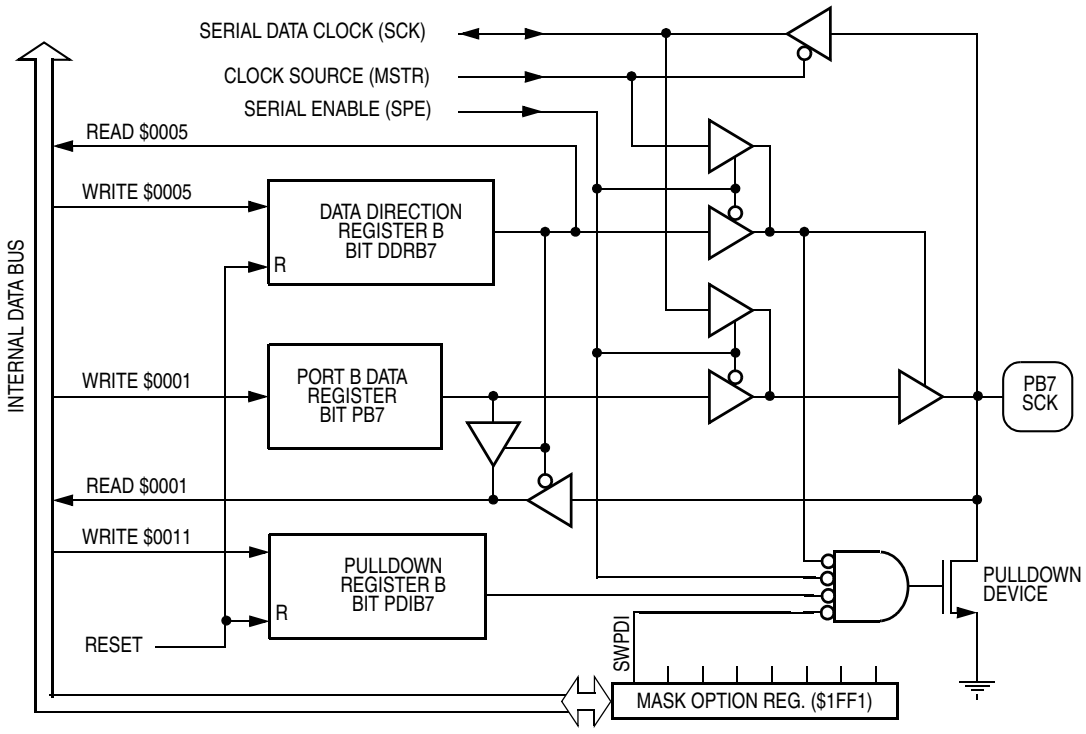

Figure 7-12. PB7/SCK Pin I/O Circuit

When using the PB7/SCK pin, these interactions must be noted:

1. If the SIOP function is required, then the SPE bit in the SCR must be set. This causes the PB7/SCK pin buffer to be controlled by the MSTR control bit in the SCR. The pulldown device is disabled in these cases.
   a. If the MSTR bit is set, then the PB7/SCK pin buffer will be enabled and driven by the serial data clock (SCK) from the SIOP.
   b. If the MSTR bit is clear, then the PB7/SCK pin buffer will be disabled, allowing the PB7/SCK pin to drive the serial data clock (SCK) into the SIOP.
2. If the SIOP function is in control of the PB7/SCK pin, the DDRB7 and PB7 data register bits are still accessible to the CPU and can be altered or read without affecting the SIOP functionality. However, if the DDRB7 bit is cleared, reading the PB7 data register will return the current state of the PB7/SCK pin.
3. If the SIOP function is terminated by clearing the SPE bit in the SCR, then the last conditions stored in the DDRB7, PDIB7, and PB7 register bits will then control the PB7/SCK pin.
4. If the PB7/SCK pin is to be a digital input, then both the SPE bit in the SCR and the DDRB7 bit must be cleared. Depending on the external application, the pulldown device may also be disabled by setting the PDIB7 pulldown inhibit bit.

7.4.3 Port C Pulldown Devices

All port C pins can have software programmable pulldown devices enabled or disabled globally by the SWPDI bit in the MOR. These pulldown devices are individually controlled by the write-only pulldown register A (PDRA) shown in Figure 7-3. PDICH controls the upper four pins (PC7–PC4) and PDICL controls the lower four pins (PC3–PC0). Clearing the PDICH or PDICL bits in the PDRA turns on the pulldown devices if the port C pin is an input. Reading the PDRA returns undefined results since it is a write-only register. Reset clears the PDICH and PDICL bits, which turns on all the port C pulldown devices.

7.4.4 Port C Logic

Figure 7-15 shows the I/O logic of port C.

When a port C pin is programmed as an output, reading the port bit actually reads the value of the data latch and not the voltage on the pin itself. When a port C pin is programmed as an input, reading the port bit reads the voltage level on the pin. The data latch can always be written, regardless of the state of its DDR bit. Table 7-4 summarizes the operations of the port C pins.

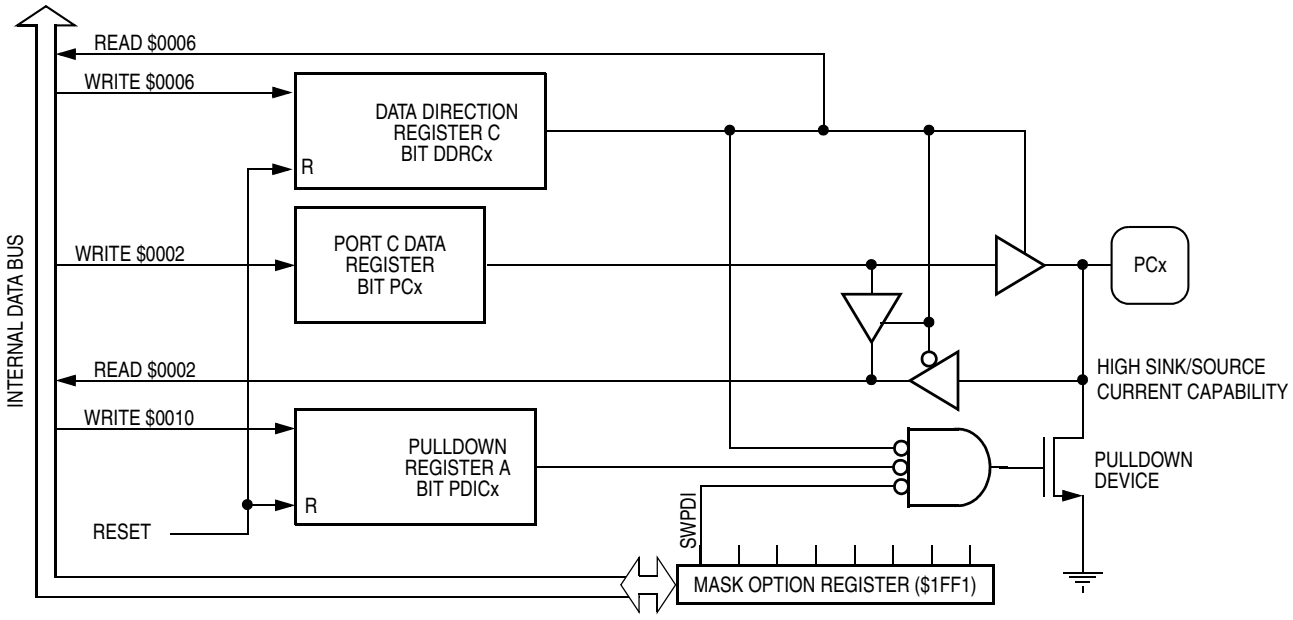

Figure 7-15. Port C I/O Circuit

8.6.1 Absolute Voltage Readings

The absolute value of a voltage measurement can be calculated in software by first taking a reference reading from a fixed source and then comparing subsequent unknown voltages to that reading as a percentage of the reference voltage multiplied times the known reference value.

The accuracy of absolute readings will depend on the error sources taken into account using the features of the analog subsystem and appropriate software as described in Table 8-6. As can be seen from this table, most of the errors can be reduced by frequent comparisons to a known voltage, use of the inverted comparator inputs, and averaging of multiple samples.

8.6.1.1 Internal Absolute Reference

If a stable source of V_{DD} is provided, the reference measurement point can be internally selected. In this case, the reference reading can be taken by setting the V_{REF} bit and clearing the MUX1:4 bits in the AMUX register. This connects the channel selection bus to the V_{DD} pin. To stay within the V_{MAX} range, the DHOLD bit should be used to select the 1/2 divided input.

8.6.1.2 External Absolute Reference

If a stable external source is provided, the reference measurement point can be any one of the channel selected pins from PB1–PB4. In this case the reference reading can be taken by setting the MUX bit in the AMUX which connects channel selection bus to the pin connected to the external reference source. If the external reference is greater than V_{DD} –1.5 volts, then the DHOLD bit should be used to select the 1/2 divided input.

Table 8-6. Absolute Voltage Reading Errors

Error Source	Accuracy Improvements Possible	
	In Hardware	In Software
Change in reference voltage	Provide closer tolerance reference	Calibration and storage of reference source over temperature and supply voltage
Change in magnitude of ramp current source	Not adjustable	Compare unknown with recent measurement from reference
Non-linearity of ramp current source vs. voltage	Not adjustable	Calibration and storage of voltages at 1/4, 1/2, 3/4, and FS
Frequency shift in internal low-power oscillator	Use external oscillator with crystal	Compare unknown with recent measurement from reference
Sampling capacitor leakage	Use faster conversion times	Compare unknown with recent measurement from reference
Internal voltage divider ratio	Not adjustable	Compare unknown with recent measurement from reference OR avoid use of divided input
Input offset voltage of comparator 2	Not adjustable	Sum two readings on reference or unknown using INV and $\overline{INV}$ control bit and divide by 2 (average of both)
Noise internal to MCU	Close decoupling at V_{DD} and V_{SS} pins and reduce supply source impedance	Average multiple readings on both the reference and the unknown voltage

8.7.2 Voltage Comparator 2

Voltage comparator 2 can be used as a simple comparator if its charge current source and discharge device are disabled by clearing the ISEN bit in the ACR. If the ISEN bit is set, the internal ramp discharge device connected to PB0/AN0 may become active and try to pull down any voltage source that may be connected to that pin. Also, since voltage comparator 2 is always connected to two of the port B I/O pins, these pins should be configured as inputs and have their software programmable pulldowns disabled.

8.8 Current Source Features

The internal current source connected to the PB0/AN0 pin supplies about 100 µA of current when the discharge device is disabled and the current source is active. Therefore, this current source can be used in an application if the ISEN enable bit is set to power up the current source and by setting the A/D conversion method to manual mode 0 (ATD1 and ATD2 cleared) and the charge current enabled (CHG set).

8.9 Internal Temperature Sensing Diode Features

An internal diode is forward biased to V_{SS} and will have its voltage change, V_D, for each degree centigrade rise in the temperature of the device. This temperature sensing diode is powered up from a current source only during the time that the diode is selected. When on, this current source typically adds about 30 µA to the I_{DD} current.

The temperature sensing diode can be selected by setting both the HOLD and DHOLD bits in the AMUX register (see 8.2 Analog Multiplex Register).

8.10 Sample and Hold

When using the internal sample capacitor to capture a voltage for later conversion, the HOLD or DHOLD bit must be cleared first before changing any channel selection. If both the HOLD (or DHOLD) bit and the channel selection are changed on the same write cycle, the sample may be corrupted during the switching transitions.

NOTE

The sample capacitor can be affected by excessive noise created with respect to the device's V_{SS} pin such that it may appear to leak down or charge up depending on the voltage level stored on the sample capacitor. It is recommended to avoid switching large currents through the port pins while a voltage is to remain stored on the sample capacitor.

The additional option of adding an offset voltage to the bottom of the sample capacitor allows unknown voltages near V_{SS} to be sampled and then shifted up past the comparator offset and the device offset caused by a single V_{SS} return pin. This offset also provides a means to measure the internal V_{SS} level regardless of the comparator offset to determine N_{OFF} as described in 8.6 Voltage Measurement Methods. In either case the OPT bit must be set in the COPR located at $1FF0 as in Figure 8-12 and the VOFF bit must be set in the ASR. It is not necessary to switch the VOFF bit during conversions, since the offset is controlled by the HOLD and DHOLD bits when the VOFF is active. Refer to 8.2 Analog Multiplex Register for more details on the design and decoding of the sample and hold circuit.

The SIOP subsystem shares its input/output pins with port B. When the SIOP is enabled (SPE bit set in the SCR), the port B data direction and data registers are bypassed by the SIOP. The port B data direction and data registers will remain accessible and can be altered by the application software, but these actions will not affect the SIOP transmitted or received data.

9.2 SIOP Signal Format

The SIOP subsystem can be software configured for master or slave operation. No external mode selection inputs are available (for instance, no slave select pin).

9.2.1 Serial Clock (SCK)

The state of the SCK output remains a fixed logic level during idle periods between data transfers. The edges of SCK indicate the beginning of each output data transfer and latch any incoming data received. The first bit of transmitted data is output from the SDO pin on the first falling edge of SCK. The first bit of received data is accepted at the SDI pin on the first rising edge of SCK after the first falling edge. The transfer is terminated upon the eighth rising edge of SCK.

The idle state of the SCK is determined by the state of the CPHA bit in the SCR. When the CPHA is clear, SCK will remain idle at a logic 1 as shown in Figure 9-2. When the CPHA is set, SCK will remain idle at a logic 0 as shown in Figure 9-3. In both cases, the SDO changes data on the falling edge of the SCK, and the SDI latches data in on the rising edge of SCK.

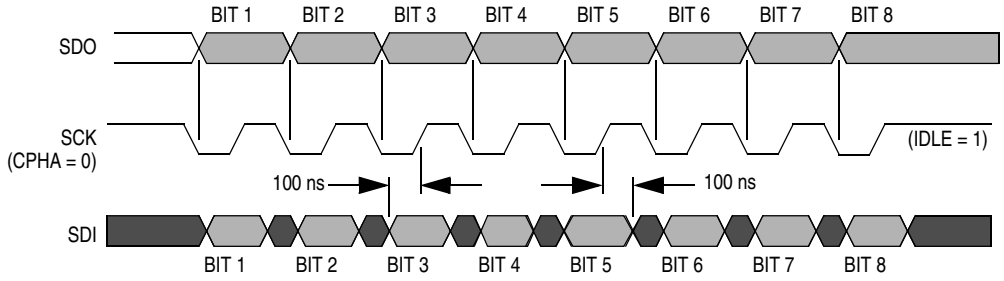

Figure 9-2. SIOP Timing Diagram (CPHA = 0)

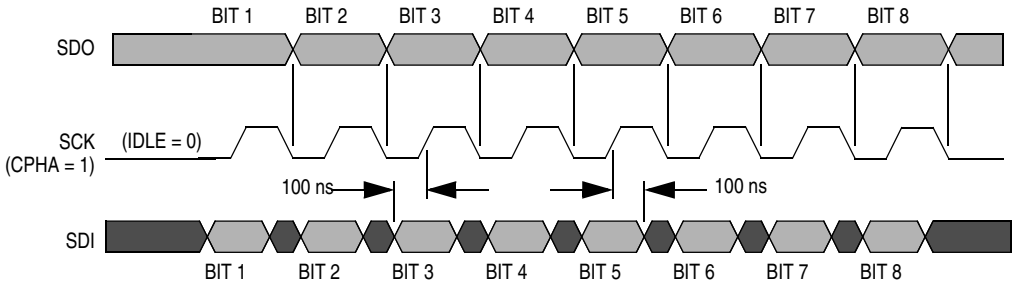

Figure 9-3. SIOP Timing Diagram (CPHA = 1)

The only difference in the master and slave modes of operation is the sourcing of the SCK. In master mode, SCK is driven from an internal source within the MCU. In slave mode, SCK is driven from a source external to the MCU. The SCK frequency is based on one of four divisions of the oscillator clock that is selected by the SPR0 and SPR1 bits in the SCR.

9.2.2 Serial Data Input (SDI)

The SDI pin becomes an input as soon as the SIOP subsystem is enabled. New data is presented to the SDI pin on the falling edge of SCK. Valid data must be present at least 100 nanoseconds before the rising edge of SCK and remain valid for 100 nanoseconds after the rising edge of SCK. See Figure 9-3.

9.2.3 Serial Data Output (SDO)

The SDO pin becomes an output as soon as the SIOP subsystem is enabled. The state of the PB5/SDO pin reflects the value of the first bit received on the previous transmission. Prior to enabling the SIOP, the PB5/SDO can be initialized to determine the beginning state. While SIOP is enabled, the port B logic cannot be used as a standard output since that pin is connected to the last stage of the SIOP serial shift register. A control bit (LSBF) is included in the SCR to allow the data to be transmitted in either the MSB first format or the LSB first format.

The first data bit will be shifted out to the SDO pin on the first falling edge of the SCK. The remaining data bits will be shifted out to the SDI pin on subsequent falling edges of SCK. The SDO pin will present valid data at least 100 nanoseconds before the rising edge of the SCK and remain valid for 100 nanoseconds after the rising edge of SCK. See Figure 9-3.

9.3 SIOP Registers

The SIOP is programmed and controlled by the SIOP control register (SCR) located at address $000A, the SIOP status register (SSR) located at address $000B, and the SIOP data register (SDR) located at address $000C.

9.3.1 SIOP Control Register (SCR)

The SIOP control register (SCR) is located at address $000A and contains seven control bits and a write-only reset of the interrupt flag. Figure 9-4 shows the position of each bit in the register and indicates the value of each bit after reset.

Address: $000A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	SPIE	SPE	LSBF	MSTR	0	CPHA	SPR1	SPR0
Write:					SPIR			
Reset:	0	0	0	0	0	0	0	0

Figure 9-4. SIOP Control Register (SCR)

SPIE — Serial Peripheral Interrupt Enable Bit

The SPIE bit enables the SIOP to generate an interrupt whenever the SPIF flag bit in the SSR is set. Clearing the SPIE bit will not affect the state of the SPIF flag bit and will not terminate a serial interrupt once the interrupt sequence has started. Reset clears the SPIE bit.

1 = Serial interrupt enabled
0 = Serial interrupt disabled

NOTE

If the SPIE bit is cleared just after the serial interrupt sequence has started (for instance, the CPU status is being stacked), then the CPU will be unable

Table 9-1. SIOP Clock Rate Selection

SPR1	SPR0	SIOP Clock Rate Oscillator Frequency Divided by:
0	0	64
0	1	32
1	0	16
1	1	8

9.3.2 SIOP Status Register

The SIOP status register (SSR) is located at address $000B and contains two read-only bits. Figure 9-5 shows the position of each bit in the register and indicates the value of each bit after reset.

Address: $000B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	SPIF	DCOL	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 9-5. SIOP Status Register (SSR)

SPIF — Serial Port Interrupt Flag

The SPIF is a read-only status bit that is set on the last rising edge of SCK and indicates that a data transfer has been completed. It has no effect on any future data transfers and can be ignored. The SPIF bit can be cleared by reading the SSR followed by a read or write of the SDR or by writing a logic 1 to the SPIR bit in the SCR. If the SPIF is cleared before the last rising edge of SCK it will be set again on the last rising edge of SCK. Reset clears the SPIF bit.

1 = Serial transfer complete, serial interrupt if the SPIE bit in SCR is set
0 = Serial transfer in progress or serial interface idle

DCOL — Data Collision Bit

The DCOL is a read-only status bit which indicates that an illegal access of the SDR has occurred. The DCOL bit will be set when reading or writing the SDR after the first falling edge of SCK and before SPIF is set. Reading or writing the SDR during this time will result in invalid data being transmitted or received. The DCOL bit is cleared by reading the SSR (when the SPIF bit is set) followed by a read or write of the SDR. If the last part of the clearing sequence is
done after another transfer has started, the DCOL bit will be set again. Reset clears the DCOL bit.

1 = Illegal access of the SDR occurred
0 = No illegal access of the SDR detected

Chapter 17
Ordering Information

17.1 Introduction

This section contains instructions for ordering the various erasable programmable read-only memory (EPROM) versions of the MC68HC05JJ/JP Family of microcontrollers.

17.2 MC68HC705JJ7 Order Numbers

MC order numbers for the available 20-pin package types are shown here.

Package Type	EPO Oscillator Type[1]	LPO Frequency (kHz)	Operating Temperature Range	Order Number
Plastic DIP[2]	XTAL	100	–40 to 85°C	MC68HC705JJ7CP
SOIC[3]	XTAL	100	–40 to 85°C	MC68HC705JJ7CDW
CERDIP[4], [5]	XTAL	100	–40 to 85°C	MC68HC705JJ7S
Plastic DIP	RC	100	–40 to 85°C	MC68HRC705JJ7CP
SOIC	RC	100	–40 to 85°C	MC68HRC705JJ7CDW
CERDIP[5]	RC	100	–40 to 85°C	MC68HRC705JJ7S
Plastic DIP	XTAL	500	–40 to 85°C	MC68HC705SJ7CP
SOIC	XTAL	500	–40 to 85°C	MC68HC705SJ7CDW
CERDIP[5]	XTAL	500	–40 to 85°C	MC68HC705SJ7S

1. Crystal/ceramic resonator or RC oscillator
2. Plastic dual in-line package (P, case outline 738)
3. Small outline integrated circuit package (DW, case outline 751D)
4. Windowed ceramic dual in-line package (S, case outline 732)
5. CERDIP parts are only guaranteed at room temperature and are for evoluation purposes only.