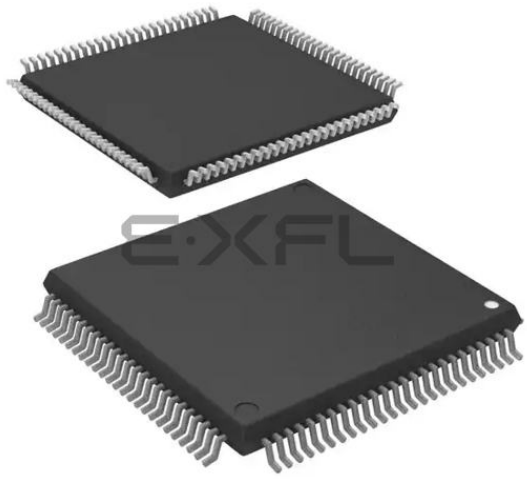
Renesas Electronics America Inc - UPD70F3025AGC-33-8EU-A Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	33MHz
Connectivity	CSI, EBI/EMI, UART/USART
Peripherals	PWM
Number of I/O	67
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3025agc-33-8eu-a

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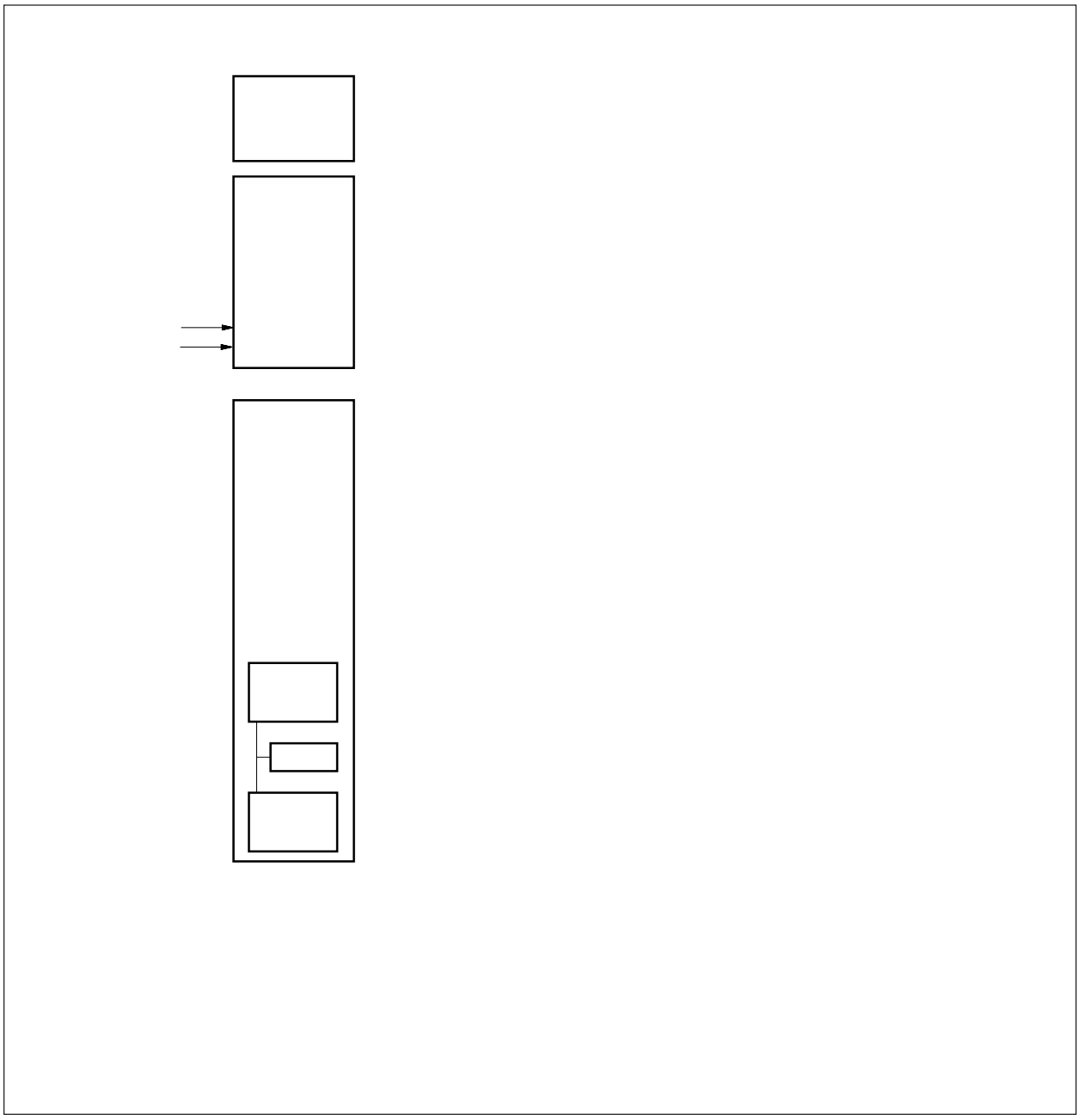
INTERNAL BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN PRODUCTS

Item	μPD703003A	μPD703004A	μPD703025A	μPD703003A(A)	μPD703025A(A)	μPD70F3003A	μPD70F3025A	μPD70F3003A(A)
Internal ROM	Mask ROM					Flash memory		
	128 KB	96 KB	256 KB	128 KB	256 KB	128 KB	256 KB	128 KB
Internal RAM	4 KB		8 KB	4 KB	8 KB	4 KB	8 KB	4 KB
Flash memory programming mode	None					Provided		
V_{PP} pin	None					Provided		
Quality grade	Standard			Special		Standard		Special
Electrical specifications	Current consumption, etc. differs. (Refer to each product data sheets).							
Others	Noise immunity and noise radiation differ because circuit scale and mask layout differ.							

Caution There are differences in noise immunity and noise radiation between the flash memory version and mask ROM version. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluation for commercial samples (not engineering samples) of the mask ROM version.

(2/2)

Pin Name	I/O	Function	Alternate Function
P60 to P63	I/O	Port 6 4-bit I/O port. Input/output can be specified in 1-bit units.	A16 to A19
P70 to P77	Input	Port 7 8-bit input port.	ANI0 to ANI7
P90	I/O	Port 9	$\overline{\text{LBEN}}$
P91		7-bit I/O port.	$\overline{\text{UBEN}}$
P92		Input/output can be specified in 1-bit units.	R/$\overline{\text{W}}$
P93			$\overline{\text{DSTB}}$
P94			ASTB
P95			$\overline{\text{HLDAK}}$
P96			$\overline{\text{HLDRQ}}$
P110	I/O	Port 11	TO140
P111		8-bit I/O port.	TO141
P112		Input/output can be specified in 1-bit units.	TCLR14
P113			TI14
P114			INTP140
P115			INTP141
P116			INTP142
P117			INTP143

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	fc = 1 MHz			15	pF
I/O capacitance	C_{IO}	Pins other than tested pin: 0 V			15	pF
Output capacitance	C_O				15	pF

Operating Conditions

Operation Mode	Internal System Clock Frequency ( )	Operating Temperature (T_A)	Supply Voltage (V_{DD})
Direct mode, PLL mode	2 to 33 MHz[Note 1]	Ð40 to +85°C	5.0 V ±10%
	5 to 33 MHz[Note 2]	Ð40 to +85°C	5.0 V ±10%

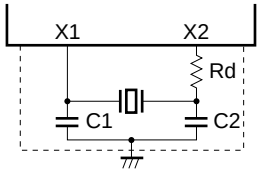
Notes 1. When A/D converter not used.
2. When A/D converter used.

Recommended Oscillator

Caution For the resonator selection and oscillator constant of the μPD70F3003A(A), customers are requested to apply to the resonator manufacturer for evaluation.

(1) Ceramic resonator connection (T_A = Ð40 to +85°C)

(a) μPD70F3003A



Manufacturer	Part Number	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	R_d (W)	MIN. (V)	MAX. (V)	
Kyocera Corporation	PBRC4.00HR	4.0	On-chip	On-chip	Ñ	4.5	5.5	0.10
	PBRC5.00HR	5.0	On-chip	On-chip	Ñ	4.5	5.5	0.08
	PBRC6.00HR	6.0	On-chip	On-chip	Ñ	4.5	5.5	0.08
	PBRC6.60HR	6.6	On-chip	On-chip	Ñ	4.5	5.5	0.08
TDK	FCR4.0MC5	4.0	On-chip	On-chip	Ñ	4.5	5.5	0.14
	FCR5.0MC5	5.0	On-chip	On-chip	Ñ	4.5	5.5	0.14
	FCR6.0MC5	6.0	On-chip	On-chip	Ñ	4.5	5.5	0.11
Murata Mfg. Co., Ltd	CSTS0400MG06	4.0	On-chip	On-chip	Ñ	4.5	5.5	0.12
	CSTCR4M00G05	4.0	On-chip	On-chip	Ñ	4.5	5.5	0.14
	CSTS0600MG06	6.0	On-chip	On-chip	Ñ	4.5	5.5	0.14
	CSTCR6M00G55-R0	6.0	On-chip	On-chip	Ñ	4.5	5.5	0.18

Cautions 1. Connect the oscillator as closely to the X1 and X2 pins as possible.
2. Do not wire any other signal lines in the area indicated by the broken lines.
3. Thoroughly evaluate the matching between the μPD70F3003A and the resonator.

DC Characteristics (T_A = −40 to +85°C, V_{DD} = 5.0 V ±10%, V_{SS} = 0 V)

(1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	Except X1 and Note	2.2		V_{DD} + 0.3	V
		Note	0.8V_{DD}		V_{DD} + 0.3	V
Input voltage, low	V_{IL}	Except X1 and Note	−0.5		+0.8	V
		Note	−0.5		0.2V_{DD}	V
Clock input voltage, high	V_{XH}	X1	0.8V_{DD}		V_{DD} + 0.5	V
Clock input voltage, low	V_{XL}	X1	−0.5		0.6	V
Schmitt trigger input threshold voltage	V_T^+	Note, rising		3.0		V
	V_T^-	Note, falling		2.0		V
Schmitt trigger input hysteresis width	$V_T^+ - V_T^-$	Note	0.5			V
Output voltage, high	V_{OH}	I_{OH} = −2.5 mA	0.7V_{DD}			V
		I_{OH} = −100 μA	V_{DD} − 0.4			V
Output voltage, low	V_{OL}	I_{OC} = 2.5 mA			0.45	V
Input leakage current, high	I_{LIH}	V_I = V_{DD}			10	μA
Input leakage current, low	I_{LIL}	V_I = 0 V			−10	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD}			10	μA
Output leakage current, low	I_{LOL}	V_O = 0 V			−10	μA
Software pull-up resistor	R	P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/$\overline{SCK3}$	15	40	90	kΩ

Note P02 to P07, P12 to P17, P23, P24, P26, P27, P32 to P37, P112 to P117, $\overline{RESET}$, NMI, MODE, and their alternate-function pins.

Remark TYP. values are reference values for when T_A = 25°C and V_{DD} = 5.0 V.

Data Retention Characteristics (T_A = Ð40 to +85°C, $V_{DD} = V_{DDDR}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Data hold voltage	V_{DDDR}	STOP mode		1.5		5.5	V
Data hold current	I_{DDDR}	μPD70F3003A, 70F3003A(A)	CESEL = 0, Note 1		$0.4V_{DDDR}$	50	μA
			CESEL = 0, Note 2		$0.4V_{DDDR}$	200	μA
			CESEL = 1, Note 1		$6V_{DDDR}$	200	μA
			CESEL = 1, Note 2		$6V_{DDDR}$	500	μA
		μPD70F3025A	CESEL = 0, Note 1		$0.4V_{DDDR}$	50	μA
			CESEL = 0, Note 2		$0.4V_{DDDR}$	200	μA
			CESEL = 1, Note 1		$12V_{DDDR}$	300	μA
			CESEL = 1, Note 2		$12V_{DDDR}$	500	μA
Supply voltage rise time	t_{RVD}			200			μs
Supply voltage fall time	t_{FVD}			200			μs
Supply voltage hold time (vs. STOP mode setting)	t_{HVD}			0			ms
STOP mode release signal input time	t_{DREL}			0			ns
Data hold input voltage, high	V_{IHDR}	Note 3		$0.9V_{DDDR}$		V_{DDDR}	V
Data hold input voltage, low	V_{ILDR}	Note 3		0		$0.1V_{DDDR}$	V

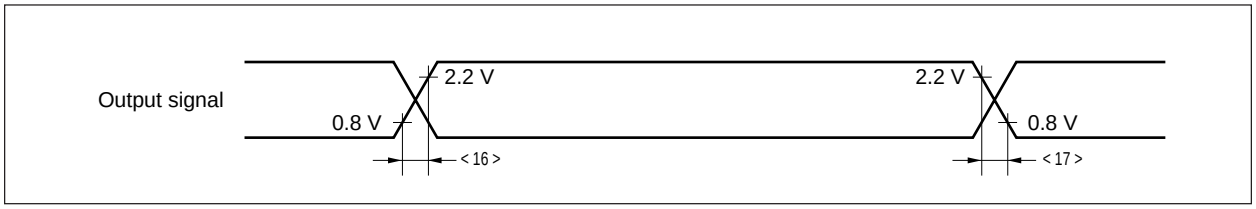
Notes 1. Ð40°C T_A +50°C

2. 50°C < T_A 85°C
3. P02 to P07, P12 to P17, P23, P24, P26, P27, P32 to P37, P112 to P117, $\overline{\text{RESET}}$, NMI, MODE, X1, and their alternate-function pins.

Remark TYP. values are reference values for when T_A = 25°C (except for the conditions in Note 2) and V_{DD} = 5.0 V.

(3) Output wave (other than CLKOUT)

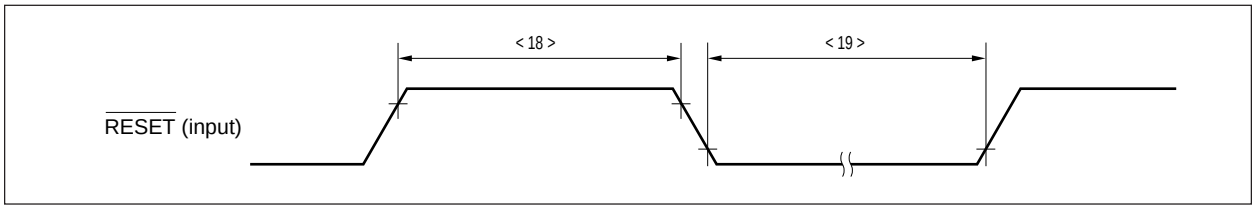
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Output rise time	<16>	t_{OR}			10	ns
Output fall time	<17>	t_{OF}			10	ns



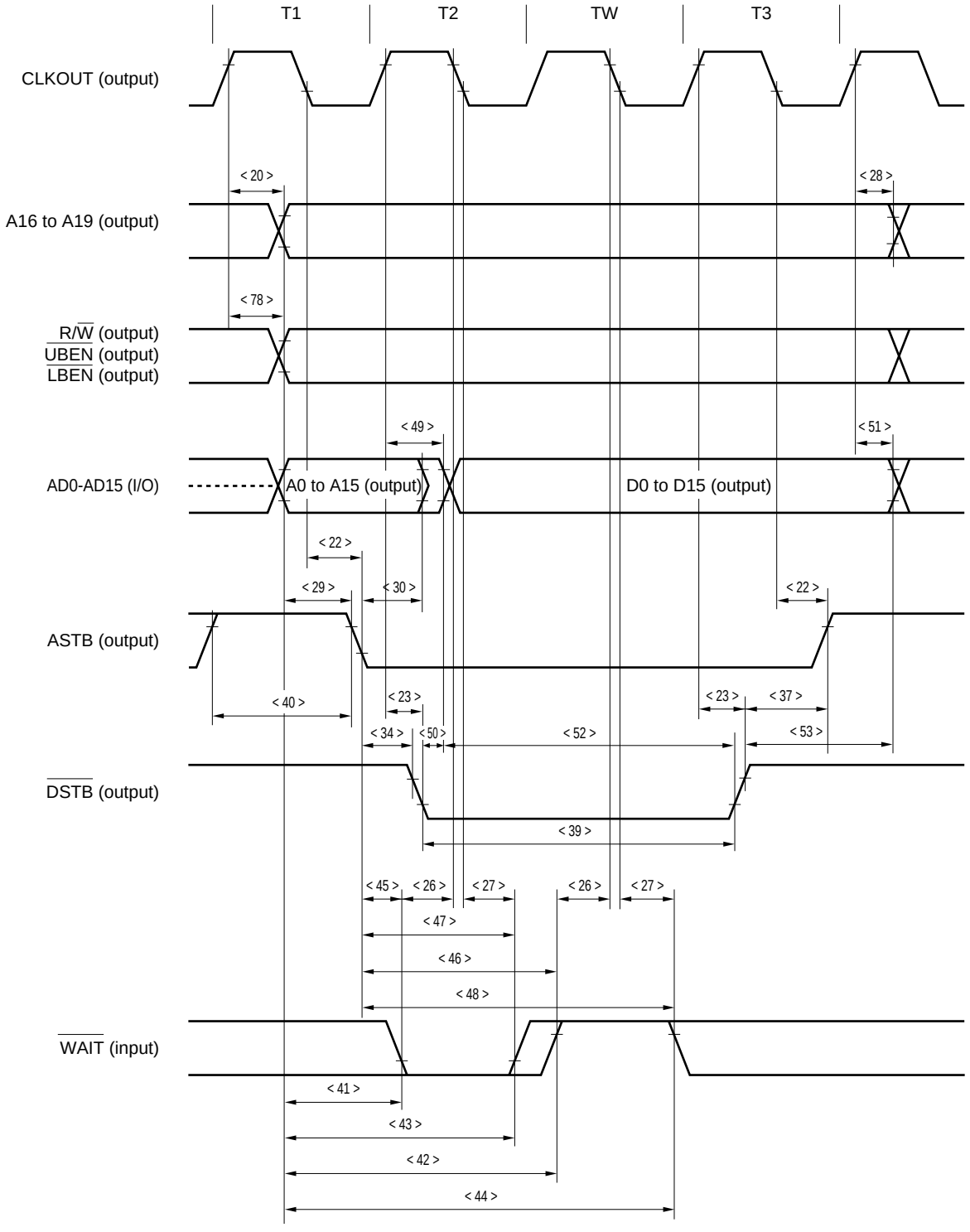
(4) Reset timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ width, high	<18>	t_{WRSH}		500		ns
$\overline{\text{RESET}}$ width, low	<19>	t_{WRSL}	On power application, or on releasing STOP mode	500 + T_{OST}		ns
			Except on power application, or except on releasing STOP mode	500		ns

Remark T_{OST}: Oscillation stabilization time

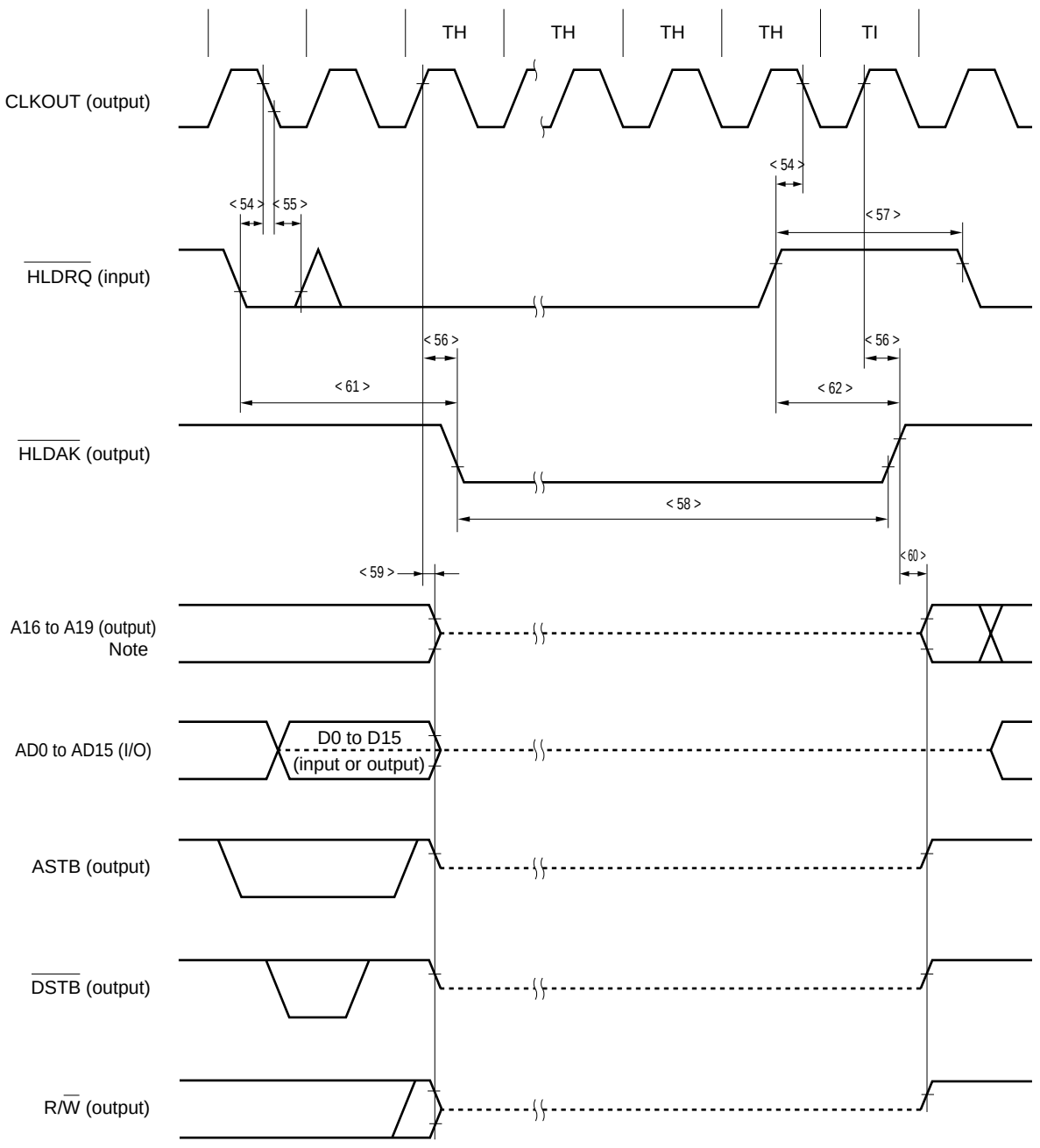


(6) Write timing (2/2): 1 wait



Remark Broken line indicates high-impedance.

(7) Bus hold timing (2/2)



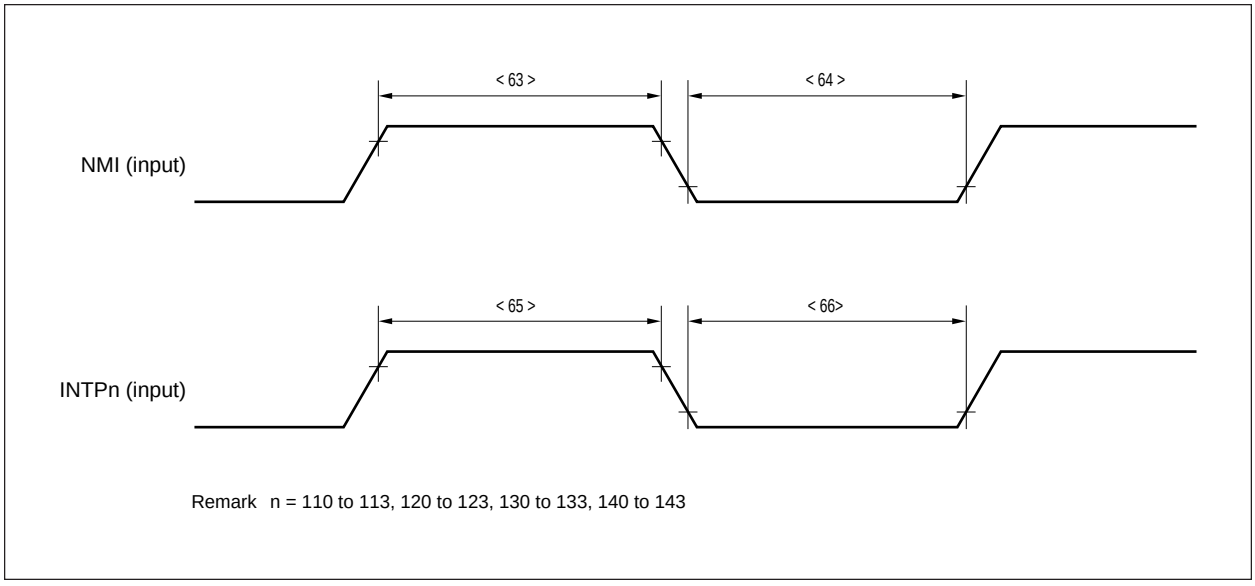
Note UBEN (output), LBEN (output)

Remark Broken line indicates high-impedance.

(8) Interrupt timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
NMI width, high	<63>	t_{WNIH}		500		ns
NMI width, low	<64>	t_{WNIL}		500		ns
INTPn width, high	<65>	t_{WITH}	n = 110 to 113, 120 to 123, 130 to 133, 140 to 143	3 T + 10		ns
INTPn width, low	<66>	t_{WITL}	n = 110 to 113, 120 to 123, 130 to 133, 140 to 143	3 T + 10		ns

Remark T = t_{CYK}



Remark n = 110 to 113, 120 to 123, 130 to 133, 140 to 143

(9) CSI timing (1/2)

(a) Master mode

(i) CSI0 to CSI2 timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<67>	t_{CYSK1}	Output	120		ns
$\overline{SCKn}$ high-level width	<68>	t_{WSKH1}	Output	0.5 t_{CYSK1} Ð 20		ns
$\overline{SCKn}$ low-level width	<69>	t_{WSKL1}	Output	0.5 t_{CYSK1} Ð 20		ns
SIn setup time (to $\overline{SCKn}$)	<70>	t_{SSISK1}		30		ns
SIn hold time (from $\overline{SCKn}$)	<71>	t_{HSKSI1}		0		ns
SOn output delay time (from $\overline{SCKn}$)	<72>	t_{DSKSO1}			18	ns
SOn output hold time (from $\overline{SCKn}$)	<73>	t_{HSKSO1}		0.5 t_{CYSK1} Ð 5		ns

Remark n = 0 to 2

(ii) CSI3 timing

Parameter	Symbol		Conditions		MIN.	MAX.	Unit
$\overline{SCK3}$ cycle	<67>	t_{CYSK3}	Output	R_L = 1.5 k	500		ns
$\overline{SCK3}$ high-level width	<68>	t_{WSKH3}	Output	C_L = 50 pF	0.5 t_{CYSK3} Ð 70		ns
$\overline{SCK3}$ low-level width	<69>	t_{WSKL3}	Output		0.5 t_{CYSK3} Ð 70		ns
SI3 setup time (to $\overline{SCK3}$)	<70>	t_{SSISK3}			100		ns
SI3 hold time (from $\overline{SCK3}$)	<71>	t_{HSKSI3}			50		ns
SO3 output delay time (from $\overline{SCK3}$)	<72>	t_{DSKSO3}	R_L = 1.5 K C_L = 50 pF			150	ns
SO3 output hold time (from $\overline{SCK3}$)	<73>	t_{HSKSO3}			0.5 t_{CYSK3} Ð 5		ns

Remark R_L and C_L are the load resistance and load capacitance respectively of the $\overline{SCK3}$ and SO3 output lines.

(b) Slave mode

(i) CSI0 to CSI2 timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<67>	t_{CYSK2}	Input	120		ns
$\overline{SCKn}$ high-level width	<68>	t_{WSKH2}	Input	30		ns
$\overline{SCKn}$ low-level width	<69>	t_{WSKL2}	Input	30		ns
SIn setup time (to $\overline{SCKn}$)	<70>	t_{SSISK2}		10		ns
SIn hold time (from $\overline{SCKn}$)	<71>	t_{HSKSI2}		10		ns
SOn output delay time (from $\overline{SCKn}$)	<72>	t_{DSKSO2}			30	ns
SOn output hold time (from $\overline{SCKn}$)	<73>	t_{HSKSO2}		t_{WSKH2}		ns

Remark n = 0 to 2

D/A Converter Characteristics (T_A = Ð40 to +85°C, $V_{DD} = AV_{DD}$ = 5 V ±10%, $V_{SS} = AV_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	Ñ		8	8	8	bit
Overall error	Ñ	Load conditions: 2 M , 30 pF $AV_{REF2} = V_{DD}$ AV_{REF3} = 0			0.8	%
	Ñ	Load conditions: 2 M , 30 pF AV_{REF2} = 0.75 V_{DD} AV_{REF3} = 0.25 V_{DD}			1.0	%
	Ñ	Load conditions: 4 M , 30 pF $AV_{REF2} = V_{DD}$ AV_{REF3} = 0			0.6	%
	Ñ	Load conditions: 4 M , 30 pF AV_{REF2} = 0.75 V_{DD} AV_{REF3} = 0.25 V_{DD}			0.8	%
Settling time	Ñ	Load conditions: 2 M , 30 pF			10	μs
Output resistance	RO			8		k
AV_{REF2} input voltage	AV_{REF2}		0.75V_{DD}		V_{DD}	V
AV_{REF3} input voltage	AV_{REF3}		0		0.25V_{DD}	V
Resistance between AV_{REF2} and AV_{REF3}	R_{AIREF}	DACS0, DACS1 = 55H	2	4		k

3.2 Flash Memory Programming Mode

Basic Characteristics (T_A = 10 to 40°C (when rewriting), T_A = Đ40 to +85°C (when not rewriting), $V_{DD} = AV_{DD}$ = 5 V ±10%, $V_{SS} = AV_{SS}$ = 0 V))

(1) μPD70F3003A (all ranks), 70F3025A (except K, E, P, X rank)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency			10		33	MHz
V_{PP} supply voltage	V_{PP1}	During flash memory programming	9.7	10.3	10.6	V
	V_{PPL}	V_{PP} low-level detection	Đ0.5		$0.2V_{DD}$	V
	V_{PPM}	V_{PP}, V_{DD} level detection	$0.8V_{DD}$		$1.2V_{DD}$	V
	V_{PPH}	V_{PP} high-voltage level detection	9.7	10.3	10.6	V
V_{DD} supply current	I_{DO}	$V_{PP} = V_{PP1}$			3.0 × + 25	mA
V_{PP} supply current	I_{PP}	V_{PP} = 10.3 V			200	mA
Step erase time	t_{ER}	Note 1		0.2		s
Overall erase time per area	t_{ERA}	When the step erase time = 0.2 s, Note 2			40	s/area
Write-back time	t_{WB}	Note 3		5		ms
Number of write-backs per write-back command	C_{WB}	When the write-back time = 5 ms, Note 4			50	Count/write-back command
Number of erase/write-backs	C_{ERWB}				16	Count
Step writing time	t_{WT}	Note 5		50		μs
Overall writing time per word	t_{WTW}	When the step writing time = 50 μs (1 word = 4 bytes), Note 6	50		500	μs/word
Number of rewrites per area	C_{ERWR}	1 erase + 1 write after erase = 1 rewrite, Note 7	20			Count/area

Notes 1. The recommended setting value of the step erase time is 0.2 s.

2. The prewrite time prior to erasure and the erase verify time (write-back time) are not included.
3. The recommended setting value of the step erase time is 5 ms.
4. Write-back is executed once by the issuance of the write-back command. Therefore, the retry count must be the maximum value minus the number of commands issued.
5. The recommended setting value of the step writing time is 50 μs.
6. 100 μs is added to the actual writing time per word. The internal verify time during and after the writing is not included.
7. When writing initially to shipped products, it is counted as one rewrite for both Òerase to writeÓ and Òwrite onlyÓ.

Example (P: Write, E: Erase)

Shipped product —— P E P E P: 3 rewrites

Shipped product E P E P E P: 3 rewrites

Cautions 1. V_{PP} pull-down resistance value (RV_{PP}) is recommended to be in the range 5 k to 15 k .

2. Set the transfer rate between programmer and device as follows.
   CSI0: 0.2 to 1 MHz
   UART0: 4,800 to 76,800 bps

Remarks 1. When the PG-FP3 is used, a time parameter required for writing/erasing by downloading parameter files is automatically set. Do not change the settings unless otherwise specified.

2. Area 0 = 00000H to 1FFFFH, area 1 = 20000H to 3FFFFH (area 1 is provided in the μPD70F3025A only)
3. The rank is indicated by the 5th character from the left in the lot number.
4. The I rank applies to engineering samples (ES) only. The operation of an ES is not guaranteed.
5. : Internal system clock frequency

(2) μPD70F3025A (X rank)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency		Note 1	10		33	MHz
V_{PP} supply voltage	V_{PP1}	During flash memory programming	9.7	10.3	10.6	V
	V_{PPL}	V_{PP} low-level detection	Ð0.5		$0.2V_{DD}$	V
	V_{PPM}	V_{PP}, V_{DD} level detection	$0.8V_{DD}$		$1.2V_{DD}$	V
	V_{PPH}	V_{PP} high-voltage level detection	9.7	10.3	10.6	V
V_{DD} supply current	I_{DD}	$V_{PP}= V_{PP1}$			3.0 × + 25	mA
V_{PP} supply current	I_{PP}	V_{PP}= 10.3 V			200	mA
Step erase time	t_{ER}	Note 1		2		s
Overall erase time per area	t_{ERA}	When the step erase time = 2 s, Note 2			40	s/area
Step writing time	t_{WT}	Note 3		200		μs
Overall writing time per word	t_{WTW}	When the step writing time = 200 μs (1 word = 4 bytes), Note 4	200		2000	μs/word
Number of rewrites per area	C_{ERWR}	1 erase + 1 write after erase = 1 rewrite, Note 5	20			Count/area

Notes 1. The recommended setting value of the step erase time is 2 s.
2. The prewrite time prior to erasure and the erase verify time (write-back time) are not included.
3. The recommended setting value of the step writing time is 200 μs.
4. 100 μs is added to the actual writing time per word. The internal verify time during and after the writing is not included.
5. When writing initially to shipped products, it is counted as one rewrite for both Òerase to writeÓ and Òwrite onlyÓ.

Example (P: Write, E: Erase)

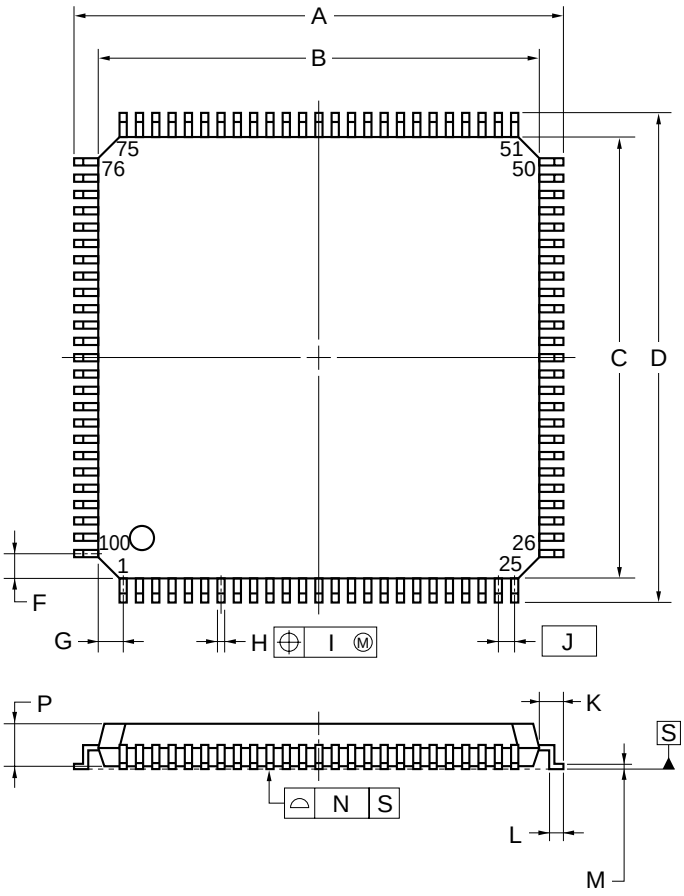
Shipped product —— P E P E P: 3 rewrites
Shipped product E P E P E P: 3 rewrites

Cautions 1. V_{PP} pull-down resistance value (RV_{PP}) is recommended to be in the range 5 k to 15 k .
2. Set the transfer rate between programmer and device as follows.
CSI0: 0.2 to 1 MHz
UART0: 4,800 to 76,800 bps

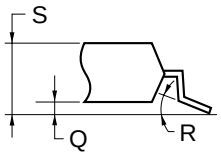
Remarks 1. When the PG-FP3 is used, a time parameter required for writing/erasing by downloading parameter files is automatically set. Do not change the settings unless otherwise specified.
2. Area 0 = 00000H to 1FFFFH, area 1 = 20000H to 3FFFFH
3. The rank is indicated by the 5th character from the left in the lot number.
4. The K, E, P, and X rank products do not support handshake mode. The I rank applies to engineering samples (ES) only. The operation of an ES is not guaranteed.
5. : Internal system clock frequency

★ 4. PACKAGE DRAWING

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



detail of lead end



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

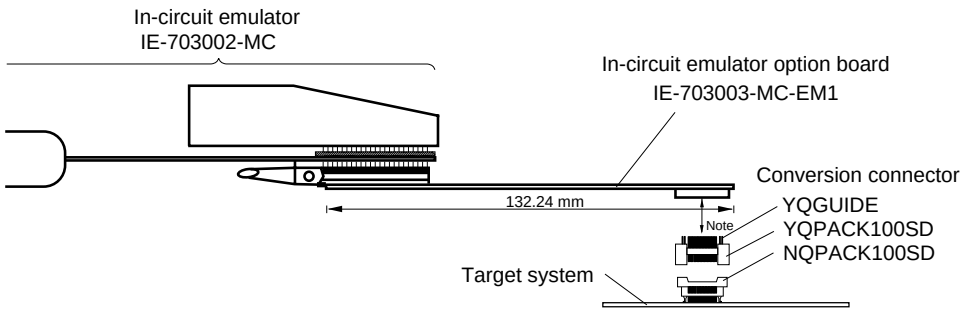
ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	$0.22^{+0.05}_{S0.04}$
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	$0.17^{+0.03}_{S0.07}$
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	$3°^{+7°}_{S3°}$
S	1.60 MAX.

S100GC-50-8EU, 8EA-2

★ APPENDIX NOTES ON TARGET SYSTEM DESIGN

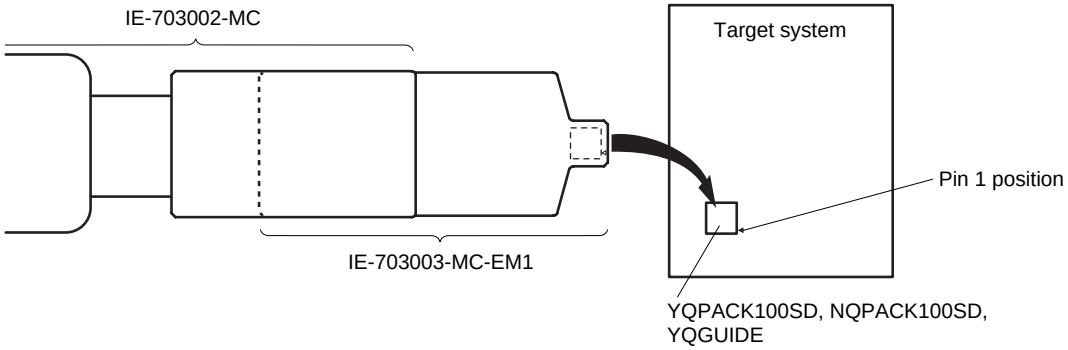
The following shows a diagram of the connection conditions between the in-circuit emulator option board and conversion connector. Design your system making allowances for conditions such as the form of parts mounted on the target system as shown below.

Side view

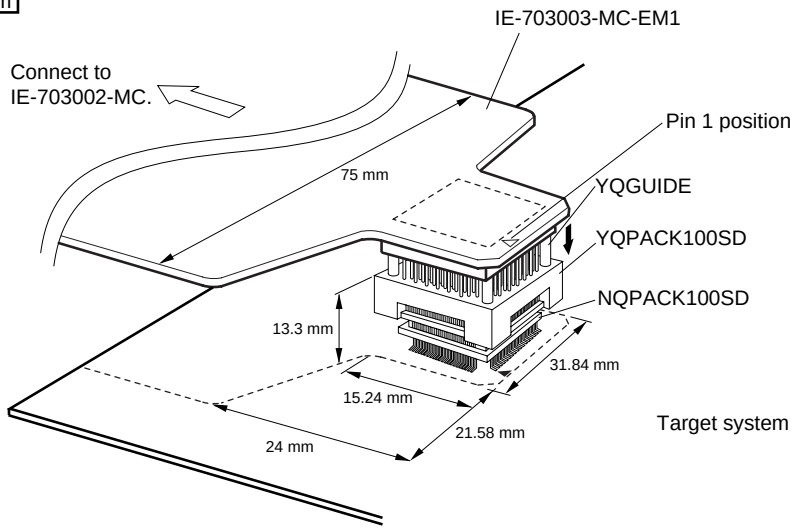


Note YQSOCKET100SDN (included with IE-703002-MC) can be inserted here to adjust the height (height: 3.2 mm).

Top view



Connection condition diagram



NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.