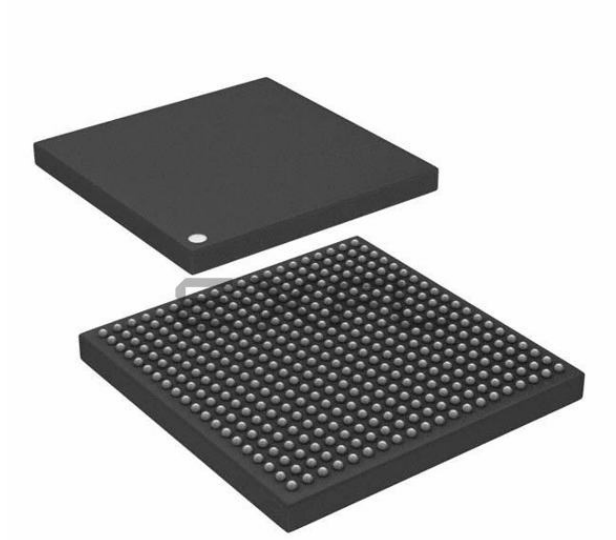

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx253cjm4

Table 2 shows the functional differences between the different parts in the i.MX25 family.

Table 2. i.MX25 Parts Functional Differences

Features	MCIMX253	MCIMX257	MCIMX258
Core	ARM 926EJ-S	ARM 926EJ-S	ARM 926EJ-S
CPU Speed	400 MHz	400 MHz	400 MHz
L1 I/D Cache	16K I/D	16K I/D	16K I/D
On-chip SRAM	128 KB	128 KB	128 KB
PATA/CE-ATA	Yes	Yes	Yes
LCD Controller	Yes	Yes	Yes
Touchscreen	—	Yes	Yes
CSI	—	Yes	Yes
FlexCAN (2)	—	Yes	Yes
ESAI	—	Yes	Yes
SIM (2)	—	Yes	Yes
Security	—	—	Yes
10/100 Ethernet	Yes	Yes	Yes
HS USB 2.0 OTG + PHY	Yes	Yes	Yes
HS USB 2.0 Host + PHY	Yes	Yes	Yes
12-bit ADC	Yes	Yes	Yes
SD/SDIO/MMC (2)	Yes	Yes	Yes
External Memory Controller	Yes	Yes	Yes
I^2C (3)	Yes	Yes	Yes
SSI/I2S (2)	Yes	Yes	Yes
CSPI (2)	Yes	Yes	Yes
UART (5)	Yes	Yes	Yes

3.4 Thermal Characteristics

The thermal resistance characteristics for the device are given in Table 16. These values are measured under the following conditions:

- Two-layer substrate
- Substrate solder mask thickness: 0.025 mm
- Substrate metal thicknesses: 0.016 mm
- Substrate core thickness: 0.200 mm
- Core through I.D: 0.118 mm, Core through plating 0.016 mm.
- Flag: Trace style with ground balls under the die connected to the flag
- Die Attach: 0.033 mm non-conductive die attach, k = 0.3 W/m K
- Mold compound: Generic mold compound; k = 0.9 W/m K

Table 16. Thermal Resistance Data

Rating	Condition	Symbol	Value	Unit
Junction to ambient[1] natural convection	Single layer board (1s)	$R_{\theta JA}$	55	°C/W
Junction to ambient[1] natural convection	Four layer board (2s2p)	$R_{\theta JA}$	33	°C/W
Junction to ambient[1] (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	46	°C/W
Junction to ambient[1] (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	29	°C/W
Junction to boards[2]	—	$R_{\theta JB}$	22	°C/W
Junction to case (top)[3]	—	$R_{\theta JCtop}$	13	°C/W
Junction to package top[4]	Natural convection	Ψ_{JT}	2	°C/W

1 Junction-to-ambient thermal resistance determined per JEDC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-board thermal resistance determined per JEDC JESD51-8. Thermal test board meets JEDEC specification for this package.

3 Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, this thermal characterization parameter is written as Psi-JT.

3.5 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- DDR I/O: Mobile DDR (mDDR), double data rate (DDR2), or synchronous dynamic random access memory (SDRAM)
- General purpose I/O (GPIO)

Figure 3 shows the load circuit for output. Figure 4 through Figure 6 show the output transition time and propagation waveforms.

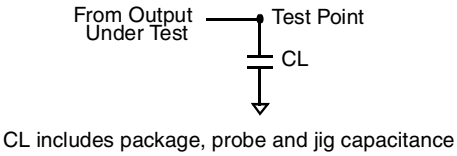


Figure 3. Load Circuit for Output

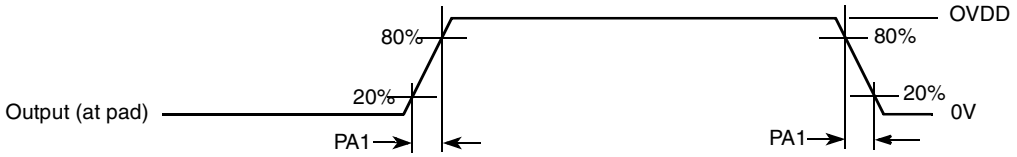


Figure 4. Output Pad Transition Time Waveform

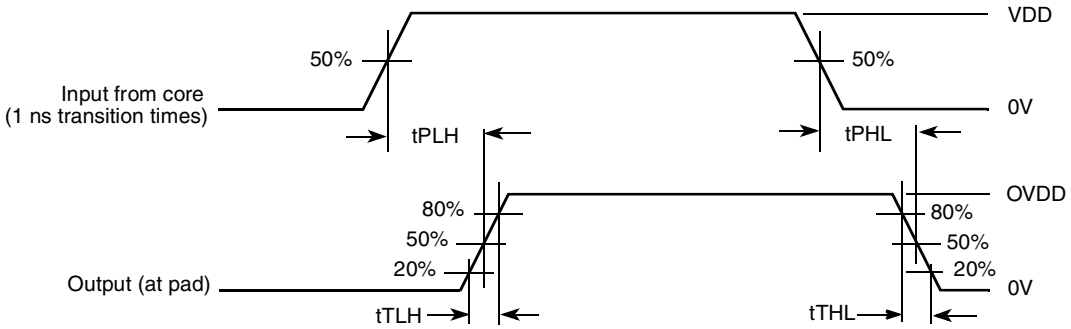


Figure 5. Output Pad Propagation and Transition Time Waveform

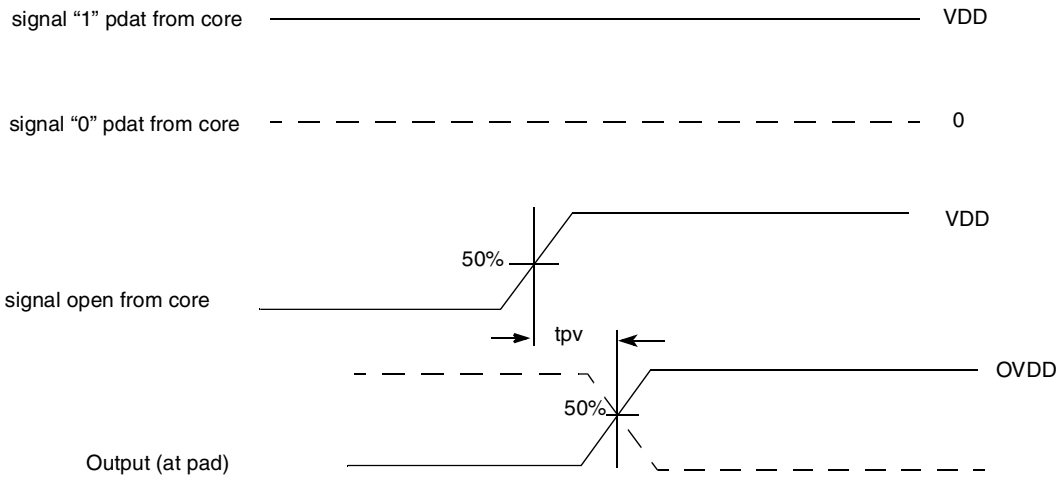


Figure 6. Output Enable to Output Valid

3.6.1 Slow I/O AC Parameters

Table 21 shows the slow I/O AC parameters.

Table 21. Slow I/O AC Parameters

Parameter	Symbol	Test Voltage	Test Capacitance	Min. Rise/Fall	Typ. Rise/Fall	Max. Rise/Fall	Units
Duty cycle	Fduty	—	—	40	—	60	%
Output pad transition times[1] (max. drive)	tpr	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	0.95/0.84 1.58/1.37 2.70/2.50 3.40/3.20	1.36/1.11 2.19/1.77 1.80/1.40 2.80/2.14	2.06/1.60 3.20/2.47 3.01/2.37 4.63/3.38	ns
Output pad transition times[1] (high drive)	tpr	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	1.60/1.39 2.94/2.51 1.85/1.48 2.93/2.37	2.23/1.79 4.05/3.17 2.90/2.17 4.56/3.40	3.26/2.50 5.72/4.27 4.75/3.43 7.33/5.26	
Output pad transition times[1] (standard drive)	tpr	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	3.07/2.62 5.82/4.95 3.04/2.47 5.37/4.40	4.22/3.30 7.94/6.19 4.73/3.50 7.70/8.10	6.03/4.48 11.28/8.28 3.01/2.36 4.63/3.38	
Output pad propagation delay[1] (max. drive), 50%–50%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	1.92/2.1 2.44/2.53 2.05/2.27 2.71/2.84	2.96/2.96 3.7/3.64 3.32/3.67 4.39/4.51	4.47/4.38 5.54/5.31 5.27/5.85 7.00/7.15	ns
Output pad propagation delay[1] (high drive), 50%–50%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	2.35/2.49 3.31/3.43 2.58/2.69 3.62/3.60	3.58/3.61 4.9/4.786 4.17/4.27 5.86/5.61	5.35/5.24 7.19/6.8 6.64/6.74 9.34/8.76	
Output pad propagation delay[1] (standard drive), 50%–50%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	3.39/3.51 5.28/5.35 3.71/3.68 5.52/5.32	5.03/4.89 7.6/7.14 6.03/5.75 8.80/7.96	7.39/6.95 10.97/9.45 9.64/8.97 13.9/11.3	
Output pad propagation delay[1] (max. drive), 40%–60%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	1.942/2.04 2.378/2.48 2.03/2.28 2.59/2.73	2.923/2.95 3.541/3.53 3.19/3.59 4.10/4.33	4.33/4.3 5.29/5.09 4.97/5.64 6.43/6.77	ns
Output pad propagation delay[1] (high drive), 40%–60%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	2.29/2.44 3.05/3.20 2.45/2.62 3.36/3.39	3.42/3.49 4.46/4.45 3.86/4.07 5.34/5.22	5.05/5.02 6.53/6.3 6.02/6.35 8.40/8.08	
Output pad propagation delay[1] (standard drive), 40%–60%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	3.12/3.26 4.60/4.73 3.43/3.46 4.89/4.79	4.58/4.53 6.61/6.32 5.48/5.34 7.75/7.16	6.69/6.42 9.5/8.32 8.65/8.26 12.2/9.97	

Table 23. Fast I/O AC Parameters for OVDD = 3.0–3.6 V (continued)

Input Pad Propagation Delay with Hysteresis, 40%–60%[4]	tpi	1.6pF	1.353/1.457	1.637/1.659	2.163/1.991	ns
Input Pad Transition Times without Hysteresis[4]	trfi	1.6pF	0.16/0.12	0.23/0.18	0.33/0.29	ns
Input Pad Transition Times with Hysteresis[4]	trfi	1.6pF	0.16/0.13	0.22/0.18	0.33/0.29	ns
Maximum Input Transition Times[5]	trm	—	—	—	—	ns

1 Maximum condition for tpr, tpo, and tpv: wcs model, 1.1 V, IO 3.0 V and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, IO 3.6 V and –40 °C. Input transition time from core is 1ns (20%–80%).

2 Minimum condition for tps: wcs model, 1.1 V, IO 3.0 V and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

3 Maximum condition for tdit: bcs model, 1.3 V, IO 3.6 V and –40 °C.

4 Maximum condition for tpi and trfi: wcs model, 1.1 V, IO 3.0 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, IO 3.6 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

5 Hysteresis mode is recommended for input with transition time greater than 25 ns.

3.6.3 DDR I/O AC Parameters

The DDR pad type is configured by the IOMUXC_SW_PAD_CTL_GRP_DDRTYPE register (see Chapter 4, “External Signals and Pin Multiplexing,” in the *i.MX25 Multimedia Applications Processor Reference Manual*).

3.6.3.1 DDR_TYPE = 00 Standard Setting I/O AC Parameters and Requirements

Table 24 shows AC parameters for mobile DDR I/O. These settings are suitable for mDDR and DDR2 1.8V (± 5%) applications.

Table 24. AC Parameters for Mobile DDR I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	50	60	%
Clock frequency[1]	f	—	—	—	133	MHz
Output pad transition times[1] (max. drive)	tpr	25 pF 50 pF	0.52/0.51 0.98/0.96	0.79/0.72 1.49/1.34	1.25/1.09 2.31/1.98	ns
Output pad transition times[1] (high drive)	tpr	25 pF 50 pF	1.13/1.10 2.15/2.10	1.74/1.55 3.28/2.92	2.71/2.30 5.11/4.31	ns
Output pad transition times[1] (standard drive)	tpr	25 pF 50 pF	2.26/2.19 4.30/4.18	3.46/3.07 6.59/5.79	5.39/4.56 10.13/8.55	ns
Output pad propagation delay[1] (max. drive), 50%–50%	tpo	15 pF 35 pF	0.80/1.03 1.06/1.32	1.36/1.50 1.76/1.90	2.21/2.40 2.83/2.82	ns
Output pad propagation delay[1] (high drive), 50%–50%	tpo	15 pF 35 pF	1.04/1.27 1.63/1.90	1.74/1.83 2.63/2.69	2.79/2.70 4.18/3.86	ns
Output pad propagation delay[1] (standard drive), 50%–50%	tpo	15 pF 35 pF	1.55/1.80 2.72/3.06	2.53/2.57 4.31/4.29	4.03/3.76 6.80/6.19	ns
Output pad propagation delay[1] (max. drive), 40%–60%	tpo	15 pF 35 pF	0.80/0.91 1.06/1.12	1.44/1.59 1.76/1.91	2.24/2.29 2.74/2.75	ns

Table 25 shows the AC parameters for mobile DDR pbijtov18_33_ddr_clk I/O.

Table 25. AC Parameters for Mobile DDR pbijtov18_33_ddr_clk I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	50	60	%
Clock frequency[1]	f	—	—	—	133	MHz
Output pad transition times[1] (max. drive)	tpr	25 pF 50 pF	0.52/0.51 0.98/0.96	0.79/0.72 1.49/1.34	1.25/1.09 2.31/1.98	ns
Output pad transition times[1] (high drive)	tpr	25 pF 50 pF	1.13/1.10 2.15/2.10	1.74/1.55 3.28/2.92	2.71/2.30 5.11/4.31	ns
Output pad transition times[1] (standard drive)	tpr	25 pF 50 pF	2.26/2.19 4.30/4.18	3.46/3.07 6.59/5.79	5.39/4.56 10.13/8.55	ns
Output pad propagation delay[1] (max. drive), 50%–50% input signals and crossing of output signals	tpo	15 pF 35 pF	1.28/1.19 1.56/1.47	1.97/1.83 2.37/2.23	2.98/2.78 3.57/3.37	ns
Output pad propagation delay[1] (high drive), 50%–50% input signals and crossing of output signals	tpo	15 pF 35 pF	1.54/1.43 2.14/2.04	2.34/2.20 3.22/3.08	3.54/3.33 4.85/4.65	ns
Output pad propagation delay[1] (standard drive), 50%–50% input signals and crossing of output signals	tpo	15 pF 35 pF	2.05/1.94 3.27/3.16	3.11/2.96 4.86/4.72	4.70/4.50 7.33/7.12	ns
Output pad propagation delay[1] (max. drive), 40%–60% input signals and crossing of output signals	tpo	15 pF 35 pF	1.45/1.36 1.73/1.64	2.13/2.00 2.53/2.40	3.14/2.94 3.74/3.54	ns
Output pad propagation delay[1] (high drive), 40%–60% input signals and crossing of output signals	tpo	15 pF 35 pF	1.70/1.60 2.31/2.21	2.51/2.37 3.38/3.24	3.70/3.50 5.02/4.82	ns
Output pad propagation delay[1] (standard drive), 40%–60% input signals and crossing of output signals	tpo	15 pF 35 pF	2.22/2.11 3.43/3.32	3.27/3.13 5.02/4.88	4.87/4.66 7.49/7.29	ns
Output enable to output valid delay[1] (max. drive), 50%–50%	tpv	15 pF 35 pF	1.16/1.12 1.42/1.41	1.91/1.81 2.31/2.20	3.10/2.89 3.72/3.47	ns
Output enable to output valid delay[1] (high drive), 50%–50%	tpv	15 pF 35 pF	1.39/1.39 1.98/2.02	2.28/2.18 3.18/3.04	3.69/3.43 5.08/4.69	ns
Output enable to output valid delay[1] (standard drive), 50%–50%	tpv	15 pF 35 pF	1.90/1.94 3.07/3.20	3.09/2.94 4.88/4.66	4.95/4.55 7.73/7.05	ns
Output enable to output valid delay[1] (max. drive), 40%–60%	tpv	15 pF 35 pF	1.28/1.24 1.49/1.47	2.00/1.90 2.32/2.21	3.14/2.93 3.64/3.41	ns
Output enable to output valid delay[1] (high drive), 40%–60%	tpv	15 pF 35 pF	1.45/1.44 1.92/1.95	2.28/2.19 2.99/2.87	3.60/3.36 4.69/4.36	ns
Output enable to output valid delay[1] (standard drive), 40%–60%	tpv	15 pF 35 pF	1.85/1.88 2.78/2.88	2.92/2.79 4.34/4.16	4.5894.25 6.79/6.24	ns
Output pad slew rate[2] (max. drive)	tps	25 pF 50 pF	0.37/0.45 0.30/0.36	0.64/0.79 0.52/0.61	1.14/1.36 0.90/1.02	V/ns

Figure 12 gives timing waveforms for PIO write mode.

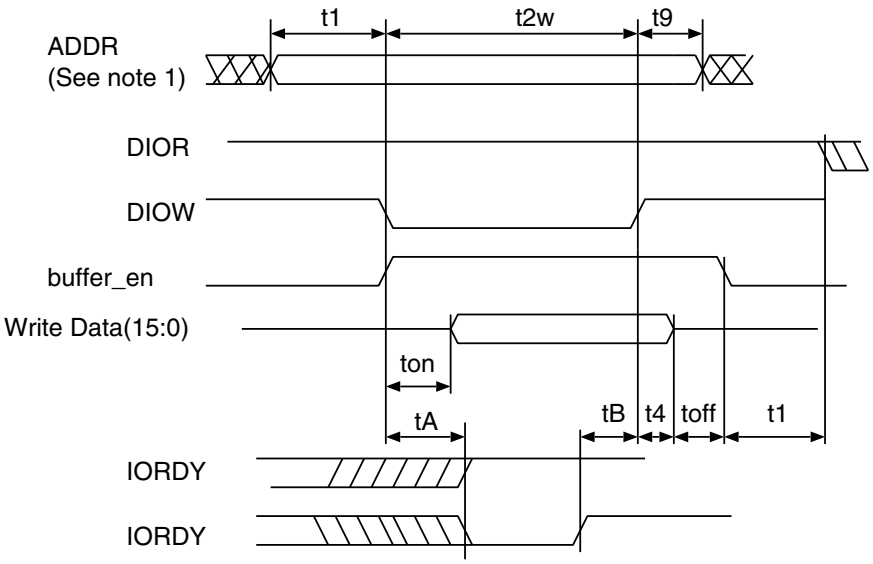


Figure 12. PIO Write Mode Timing

To meet PIO write mode timing requirements, a number of timing parameters must be controlled. Table 37 shows timing parameters and their determining relations, and indicates parameters that can be adjusted to meet required conditions.

Table 37. Timing Parameters for PIO Write Mode

ATA Parameter	PIO Write Mode Timing Parameter[1]	Relation	Adjustable Parameter(s)
t1	t1	t1(min.) = time_1 × T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2w	t2(min.) = time_2w × T – (tskew1 + tskew2 + tskew5)	time_2w
t9	t9	t9(min.) = time_9 × T – (tskew1 + tskew2 + tskew6)	time_9
t3	—	t3(min.) = (time_2w – time_on) × T – (tskew1 + tskew2 +tskew5)	if not met, increase time_2w
t4	t4	t4(min.) = time_4 × T – tskew1	time_4
tA	tA	tA = (1.5 + time_ax) × T – (tco + tsui + tcable2 + tcable2 + 2 × tbuf)	time_ax
t0	—	t0(min.) = (time_1 + time_2 + time_9) × T	time_1, time_2r, time_9
—	—	Avoid bus contention when switching buffer on by making ton long enough	—
—	—	Avoid bus contention when switching buffer off by making toff long enough	—

[1] See Figure 12.

Table 45. SDR SDRAM Write Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	SDRAM clock low-level width	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD4	CS, RAS, CAS, WE, DQM, CKE setup time	tCMS	2.0	—	ns
SD5	CS, RAS, CAS, WE, DQM, CKE hold time	tCMH	1.8	—	ns
SD6	Address setup time	tAS	2.0	—	ns
SD7	Address hold time	tAH	1.8	—	ns
SD11	Precharge cycle period[1]	tRP	1	4	clock
SD12	Active to read/write command delay[1]	tRCD	1	8	clock
SD13	Data setup time	tDS	2.0	—	ns
SD14	Data hold time	tDH	1.3	—	ns

[1] SD11 and SD12 are determined by SDRAM controller register settings.

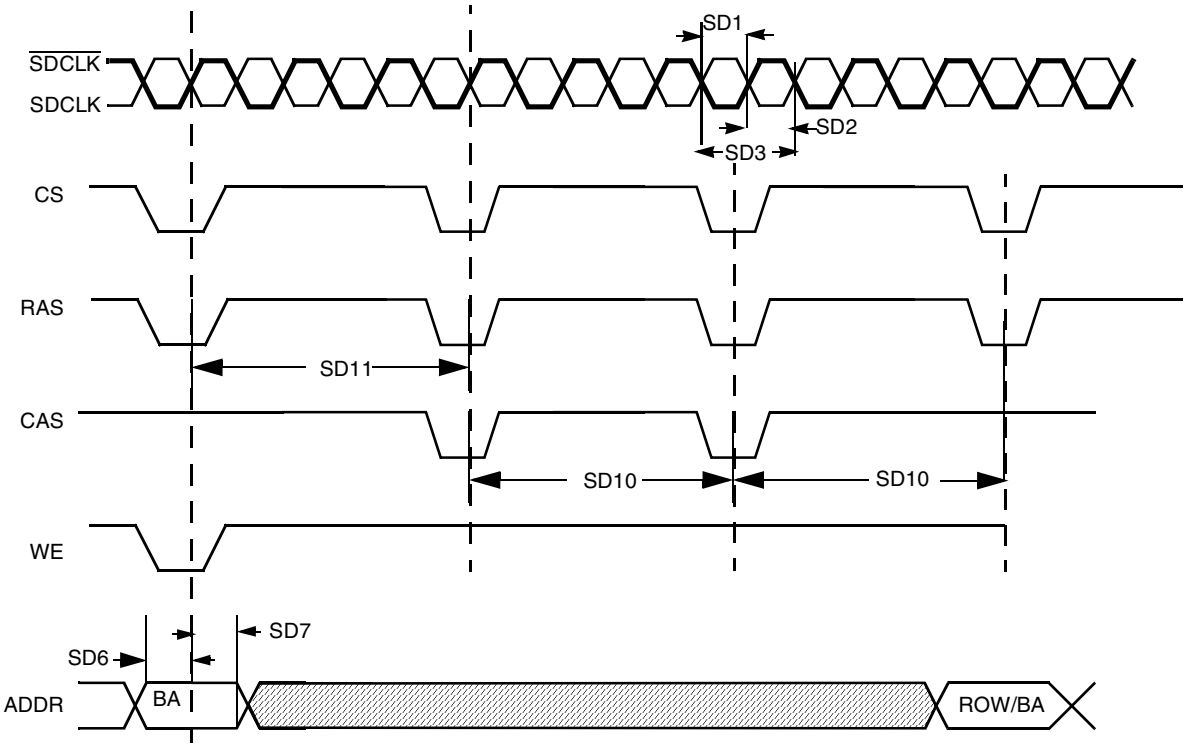


Figure 27. SDRAM Refresh Timing Diagram

Table 47. SDRAM Self-Refresh Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD16	CKE output delay time	tCKS	1.8	—	ns

3.7.6.1.2 Mobile DDR SDRAM–Specific Parameters

The following diagrams and tables specify the timings related to the SDRAMC module which interfaces with the mobile DDR SDRAM.

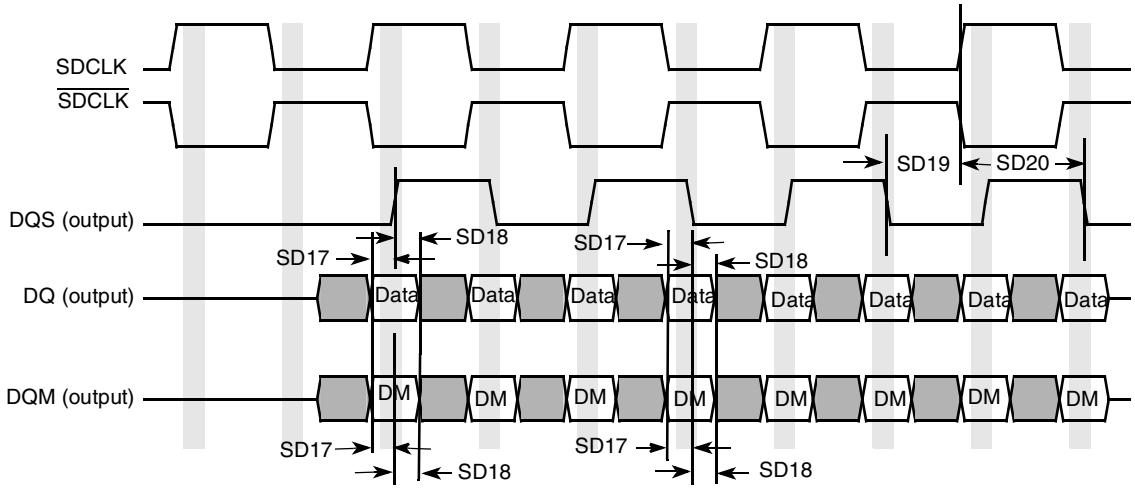


Figure 29. Mobile DDR SDRAM Write Cycle Timing Diagram

Table 48. Mobile DDR SDRAM Write Cycle Timing Parameters[1]

ID	Parameter	Symbol	Min.	Max.	Unit
SD17	DQ and DQM setup time to DQS	tDS	0.95	—	ns
SD18	DQ and DQM hold time to DQS	tDH	0.95	—	ns
SD19	Write cycle DQS falling edge to SDCLK output delay time	tDSS	1.8	—	ns
SD20	Write cycle DQS falling edge to SDCLK output hold time	tDSH	1.8	—	ns

[1] Test condition: Measured using delay line 5 programmed as follows: ESDCDLY5[15:0] = 0x0703.

3.7.6.1.3 DDR2 SDRAM–Specific Parameters

The following diagrams and tables specify timing related to the SDRAMC module, which interfaces with DDR2 SDRAM.

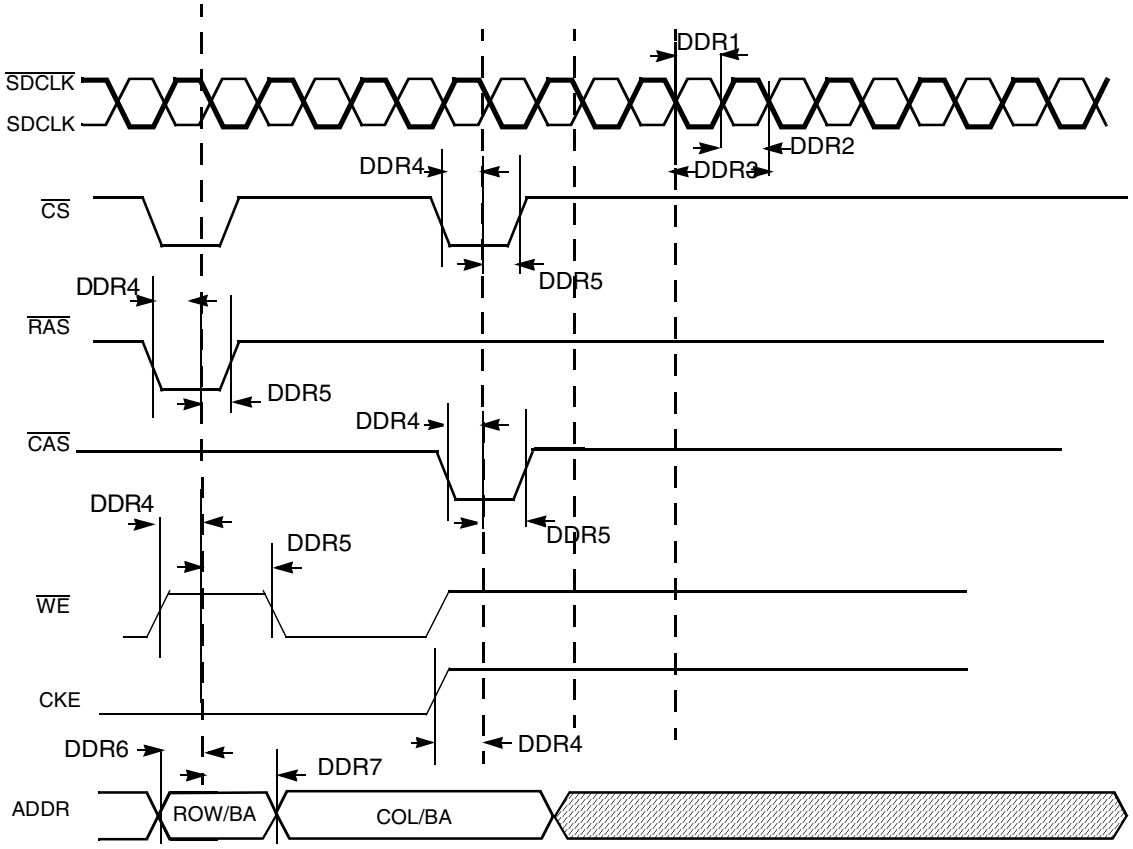


Figure 31. DDR2 SDRAM Basic Timing Parameters

Table 50 provides values for a command/address slew rate of 1 V/ns and an SDCLK, SDCLK_B differential slew rate of 2 V/ns. For additional values, use Table 51, “tlS, tlH Derating Values for DDR2-400, DDR2-533.”

Table 50. DDR2 SDRAM Timing Parameter Table

ID	Parameter	Symbol	DDR2-400		Unit
			Min.	Max.	
DDR1	SDRAM clock high-level width	t_{CH}	0.45	0.55	t_{CK}
DDR2	SDRAM clock low-level width	t_{CL}	0.45	0.55	t_{CK}
DDR3	SDRAM clock cycle time	t_{CK}	7.5	8	ns

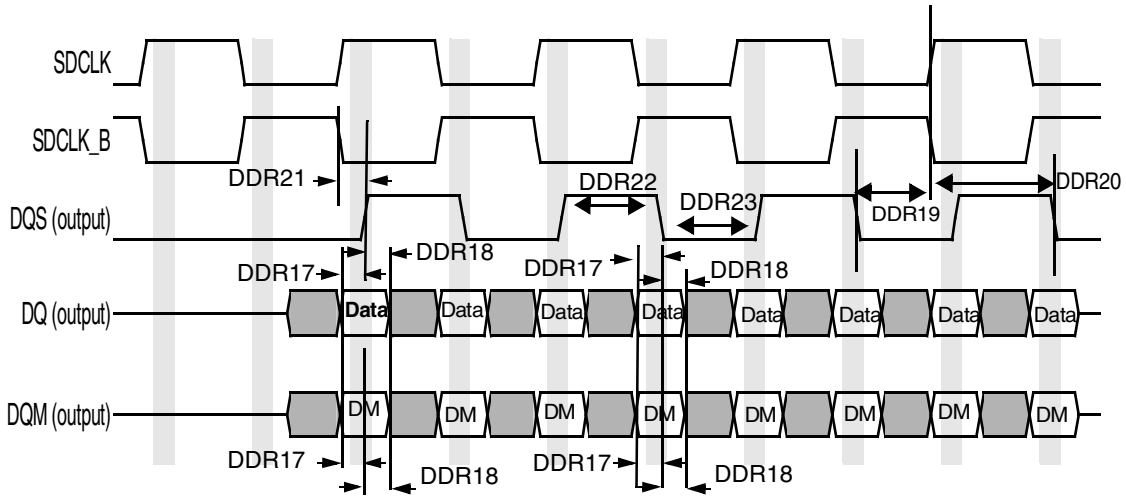


Figure 32. DDR2 SDRAM Write Cycle Timing Diagram

Table 52. DDR2 SDRAM Write Cycle Parameter Table

ID	Parameter	Symbol	DDR2-400		Unit
			Min.	Max.	
DDR17	DQ & DQM setup time to DQS (single-ended strobe)[1]	$t_{DS1(base)}$	0.6	—	ns
DDR18	DQ & DQM hold time to DQS (single-ended strobe)[1]	$t_{DH1(base)}$	0.6	—	ns
DDR19	Write cycle DQS falling edge to SDCLK output setup time	t_{DSS}	0.3	—	tCK
DDR20	Write cycle DQS falling edge to SDCLK output hold time	t_{DSH}	0.3	—	tCK
DDR21	DQS latching rising transitions to associated clock edges	t_{DQSS}	-0.2	0.2	tCK
DDR22	DQS high-level width	t_{DQSH}	0.35	—	tCK
DDR23	DQS low-level width	t_{DQSL}	0.35	—	tCK

[1] These values are for a DQ/DM slew rate of 1 V/ns and a DQS slew rate of 1 V/ns. For additional values use Table 53, “DtDS1, DtDH1 Derating Values for DDR2-400, DDR2-533.”

Table 53. ΔtDS1, ΔtDH1 Derating Values for DDR2-400, DDR2-533[1,2,3]

	DQS Single-Ended Slew Rate																	
	2.0 V/ns		1.5 V/ns		1.0 V/ns		0.9 V/ns		0.8 V/ns		0.7 V/ns		0.6 V/ns		0.5 Vns		0.4 V/ns	
	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1

Table 53. ΔtDS1, ΔtDH1 Derating Values for DDR2-400, DDR2-533[1,2,3] (continued)

		DQS Single-Ended Slew Rate																	
DQ Slew Rate V/ns	2.0	188	188	167	146	125	63	—	—	—	—	—	—	—	—	—	—	—	—
	1.5	146	167	125	125	83	42	81	43	—	—	—	—	—	—	—	—	—	—
	1.0	63	125	42	83	0	0	–2	1	–7	–13	—	—	—	—	—	—	—	—
	0.9	—	—	31	69	–11	–14	–13	–13	–18	–27	–29	–45	—	—	—	—	—	—
	0.8	—	—	—	—	–25	–31	–27	–30	–32	–44	–43	–62	–60	–86	—	—	—	—
	0.7	—	—	—	—	—	—	–45	–53	–50	–67	–61	–85	–78	–109	–108	–152	—	—
	0.6	—	—	—	—	—	—	—	—	–74	–96	–85	–114	–102	–138	–132	–181	–183	–246
	0.5	—	—	—	—	—	—	—	—	—	—	–128	–156	–145	–180	–175	–223	–226	–288
	0.4	—	—	—	—	—	—	—	—	—	—	—	—	–210	–243	–240	–286	–291	–351

1 All units in 'ps'.

2 Test conditions are at capacitance=15pF for DDR PADS. Recommended drive strengths are medium for SDCLK and high for address and controls.

3 SDRAM CLK and DQS related parameters are measured from the 50% point. That is, high is defined as 50% of the signal value, and low is defined as 50% of the signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and SDCLK (inverted clock).

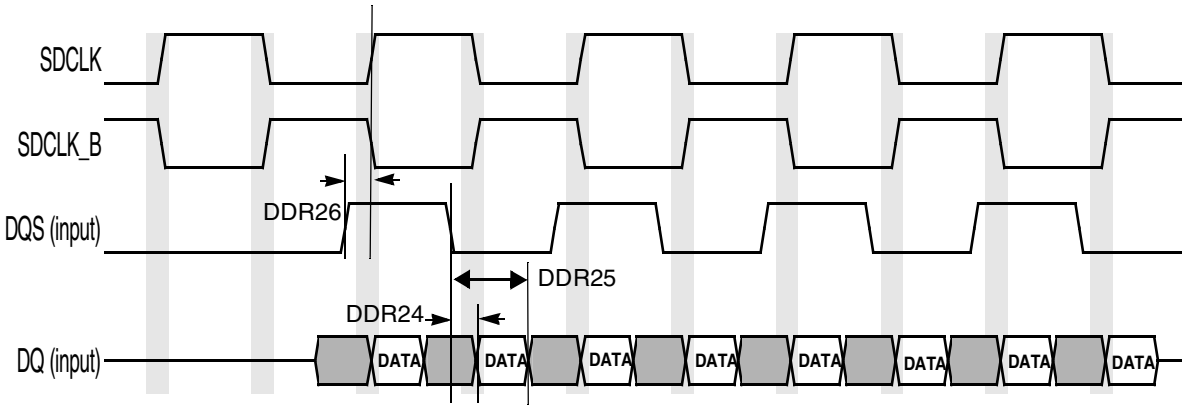


Figure 33. DDR2 SDRAM DQ vs. DQS and SDCLK READ Cycle Timing Diagram

Table 54. DDR2 SDRAM Read Cycle Parameter Table[1,2]

ID	Parameter	Symbol	DDR2-400		Unit
			Min.	Max.	
DDR24	DQS - DQ Skew (defines the Data valid window in read cycles related to DQS)	t_{DQSQ}	—	0.6	ns
DDR25	DQS DQ in HOLD time from DQS[3]	t_{QH}	2.5	—	ns
DDR26	DQS output access time from SDCLK posedge	t_{DQSCK}	–0.5	0.5	ns

1 Test conditions are at capacitance=15 pF for DDR PADS. Recommended drive strengths are medium for SDCLK and high for address and controls.

Figure 39 through Figure 44 give examples of basic WEIM accesses to external memory devices with the timing parameters described in Table 56 for specific control parameter settings.

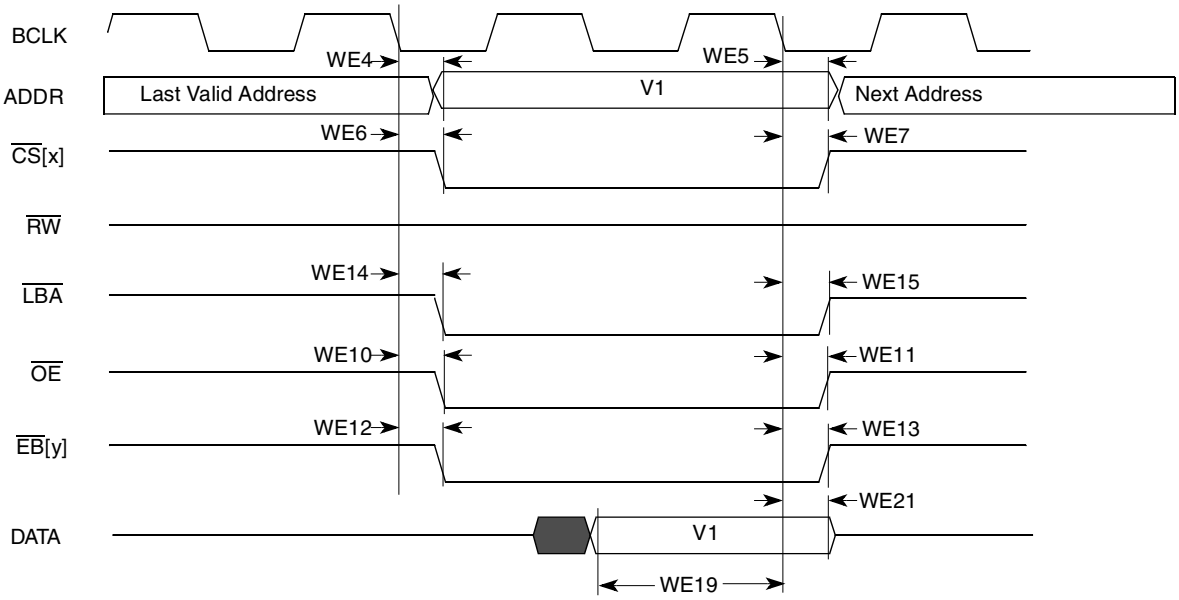


Figure 39. Synchronous Memory Timing Diagram for Read Access—WSC=1

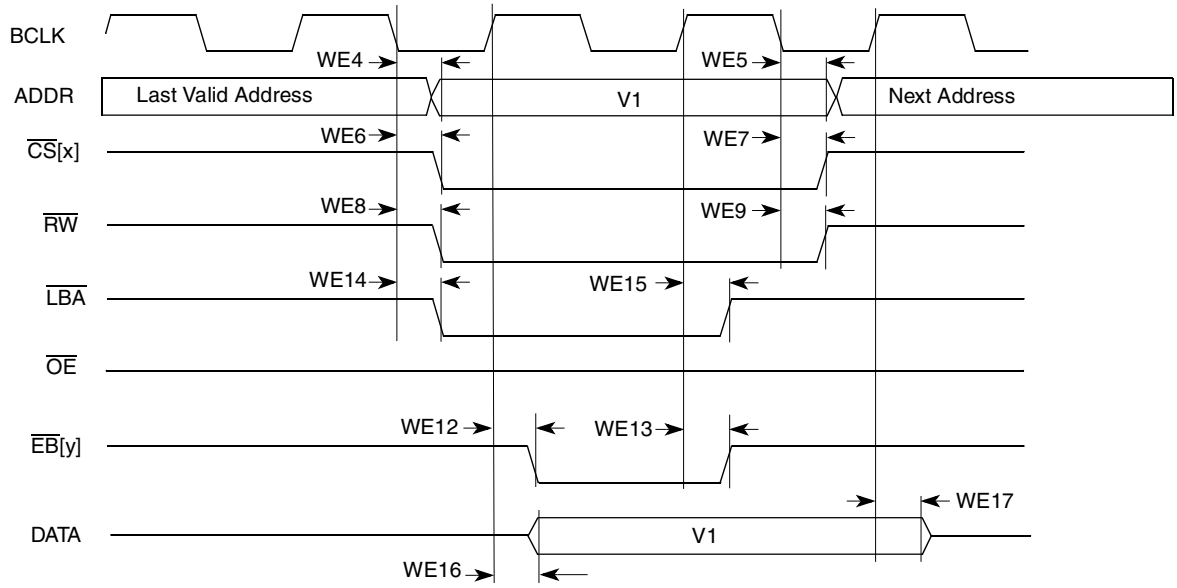


Figure 40. Synchronous Memory Timing Diagram for Write Access—WSC=1, EBWA=1, EBWN=1, LBN=1

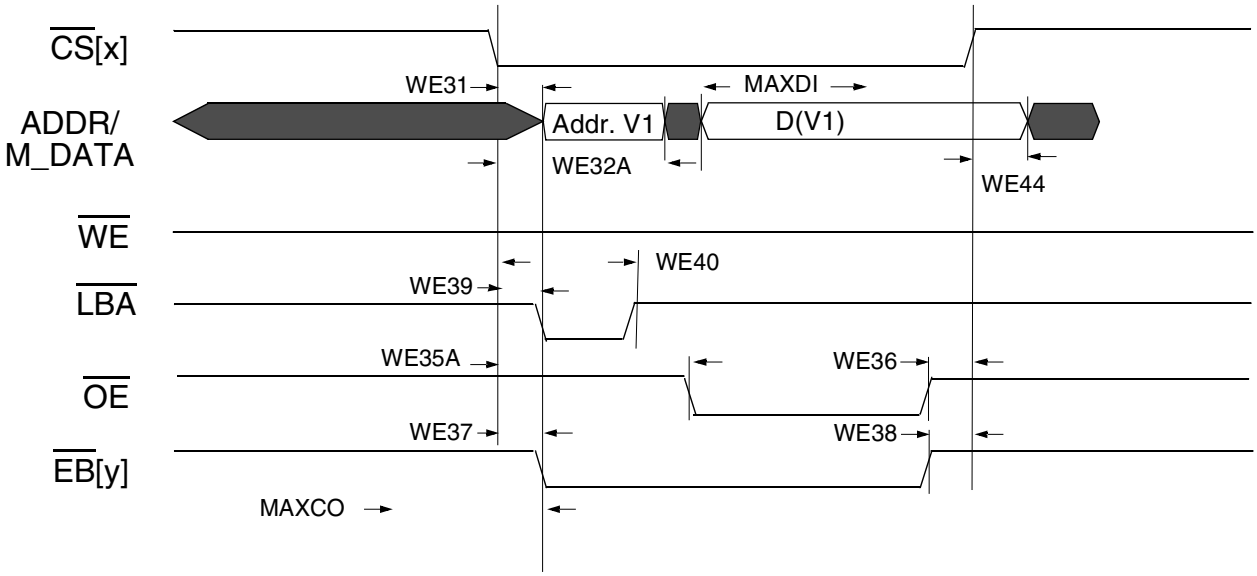


Figure 46. Asynchronous A/D Muxed Read Access (RWSC = 5)

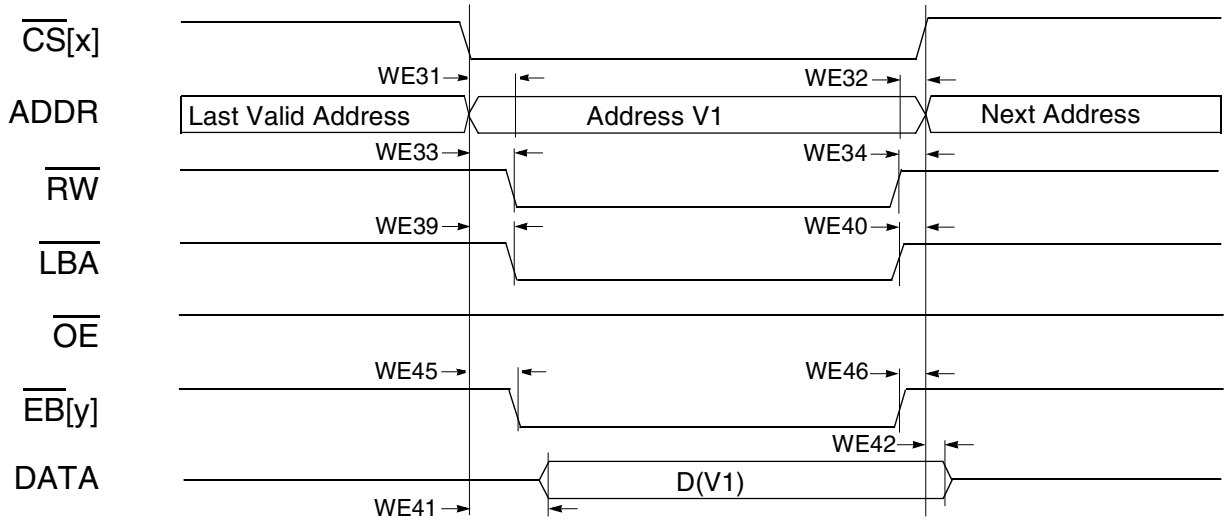


Figure 47. Asynchronous Memory Write Access

3.7.11 Inter IC Communication (I^2C) Timing

The I^2C communication protocol consists of the following seven elements:

- Start
- Data source/recipient
- Data direction
- Slave acknowledge
- Data
- Data acknowledge
- Stop

Figure 64 shows the timing of the I^2C module. Table 69 and Table 70 describe the I^2C module timing parameters (IC1–IC6) shown in the figure.

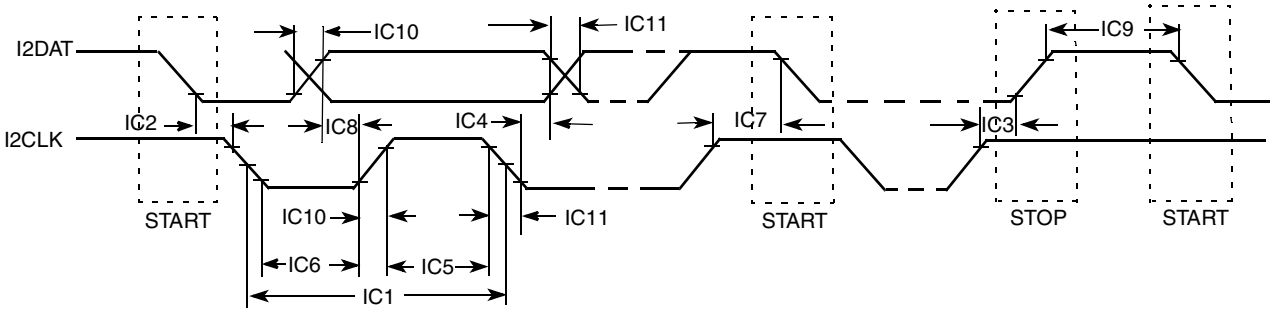


Figure 64. I^2C Module Timing Diagram

Table 69. I2C Module Timing Parameters: 3.0 V +/–0.30 V

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
IC1	I2CLK cycle time	10	-	2.5		µs
IC2	Hold time (repeated) START condition	4.0	-	0.6	-	µs
IC3	Set-up time for STOP condition	4.0	-	0.6	-	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	-	0.6	-	µs
IC6	LOW Period of the I2CLK Clock	4.7	-	1.3	-	µs
IC7	Set-up time for a repeated START condition	4.7	-	0.6	-	µs
IC8	Data set-up time	250	-	100[3]	-	ns
IC9	Bus free time between a STOP and START condition	4.7	-	1.3	-	µs
IC10	Rise time of both I2DAT and I2CLK signals	-	1000	$20+0.1C_b$[4]	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	-	300	$20+0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	-	400	-	400	pF

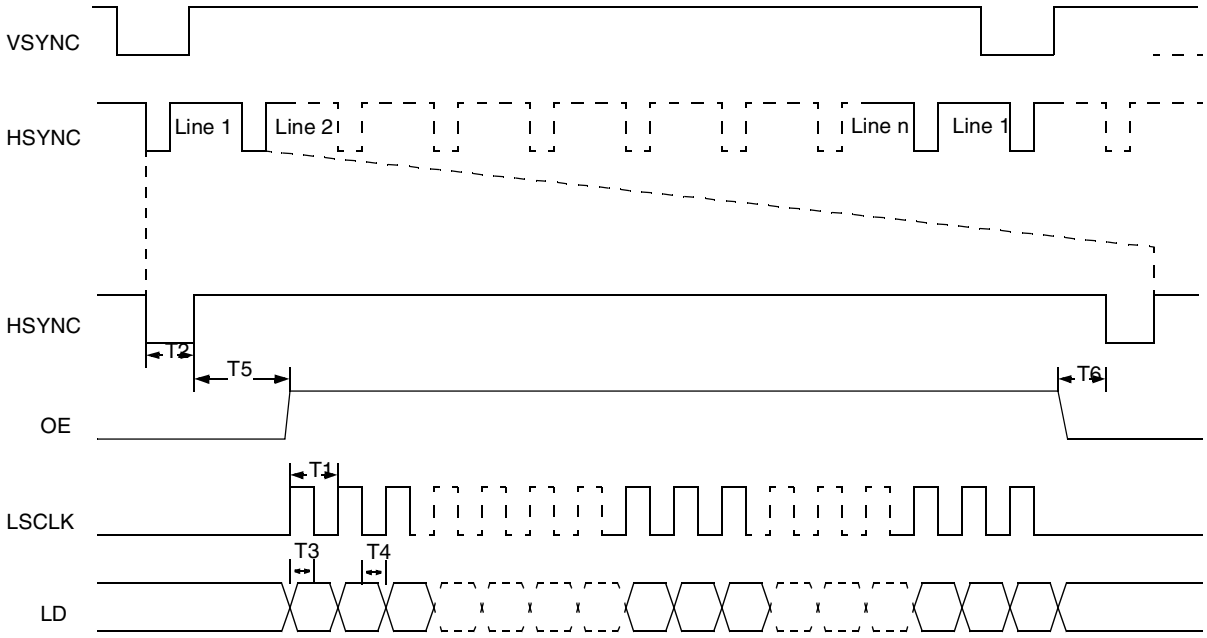


Figure 66. LCDC TFT Mode Timing Diagram

Table 72. LCDC TFT Mode Timing Parameters

ID	Description	Min.	Ma	Unit
T1	Pixel clock period	22.5	1000	ns
T2	HSYNC width	1	—	T[1]
T3	LD setup time	5	—	ns
T4	LD hold time	5	—	ns
T5	Delay from the end of HSYNC to the beginning of the OE pulse	3	—	T[1]
T6	Delay from end of OE to the beginning of the HSYNC pulse	1	—	T[1]

1 T is pixel clock period

3.7.13 Pulse Width Modulator (PWM) Timing Parameters

Figure 67 depicts the timing of the PWM, and Table 73 lists the PWM timing characteristics.

The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse width modulator output (PWMO) external pin.

Table 82. SSI Receiver Timing with Internal Clock (continued)

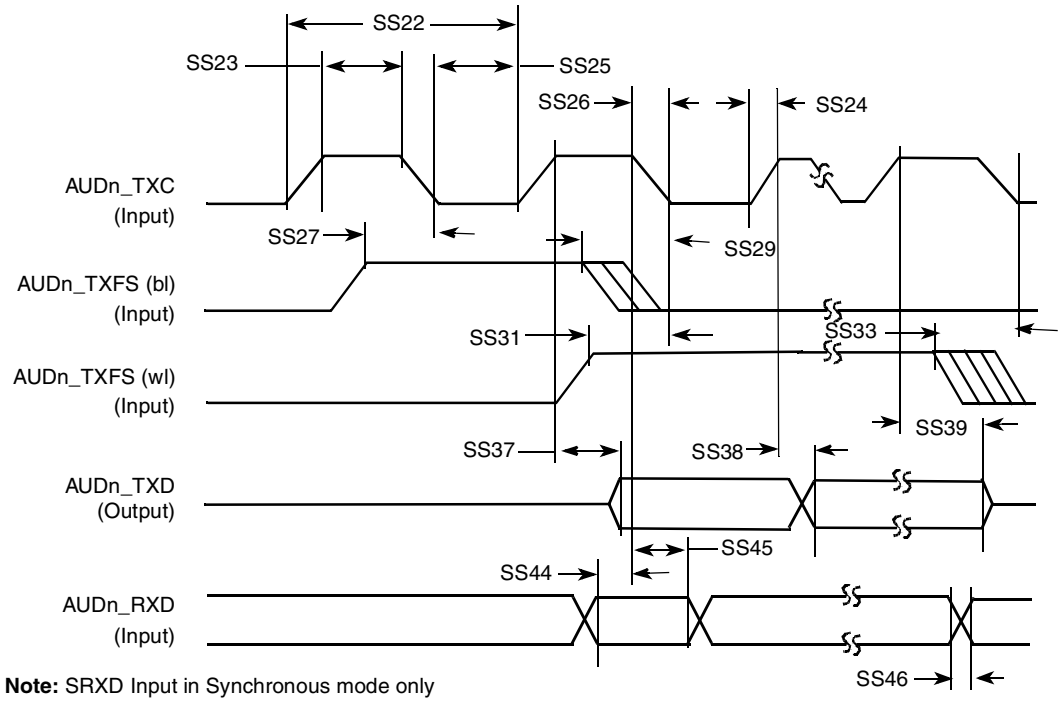
ID	Parameter	Min.	Max.	Unit
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

Note:

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on pads when SSI is being used for a data transfer.
- ”Tx” and “Rx” refer to the transmit and receive sections of the SSI.
- For internal frame sync operation using external clock, the FS timing is the same as that of Tx Data (for example, during AC97 mode of operation).

3.7.17.3 SSI Transmitter Timing with External Clock

Figure 80 shows the timing for the SSI transmitter with external clock. Table 83 describes the timing parameters (SS22-SS46) shown in the figure.



Note: SRXD Input in Synchronous mode only

Figure 80. SSI Transmitter with External Clock Timing Diagram

3.7.17.4 SSI Receiver Timing with External Clock

Figure 81 shows the timing for SSI receiver with external clock. Table 84 describes the timing parameters (SS22–SS41) used in the figure.

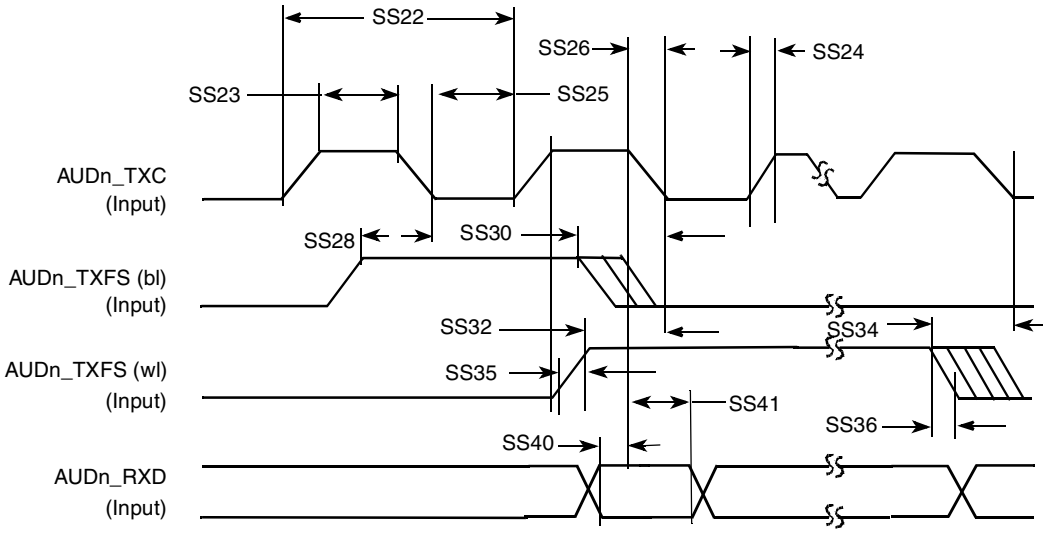


Figure 81. SSI Receiver with External Clock Timing Diagram

Table 84. SSI Receiver Timing with External Clock

ID	Parameter	Min.	Max.	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	FS (bl) low/high setup before (Tx) CK falling	–10.0	15.0	ns
SS30	FS (bl) low/high setup before (Tx) CK falling	10.0	—	ns
SS32	FS (wl) low/high setup before (Tx) CK falling	–10.0	15.0	ns
SS34	FS (wl) low/high setup before (Tx) CK falling	10.0	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10.0	—	ns
SS41	SRXD hold time after (Rx) CK low	2.0	—	ns

Note:

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on pads when SSI is being used for data transfer.

3.7.19.2 UART Infrared (IrDA) Mode Timing

The following subsections describe the UART transmit and receive timing in IrDA mode.

3.7.19.2.3 UART IrDA Mode Transmit Timing

Figure 87 depicts the UART transmit timing in IrDA mode, showing only 8 data bits and 1 stop bit. Table 88 describes the timing parameters (UA3–UA4) shown in the figure.

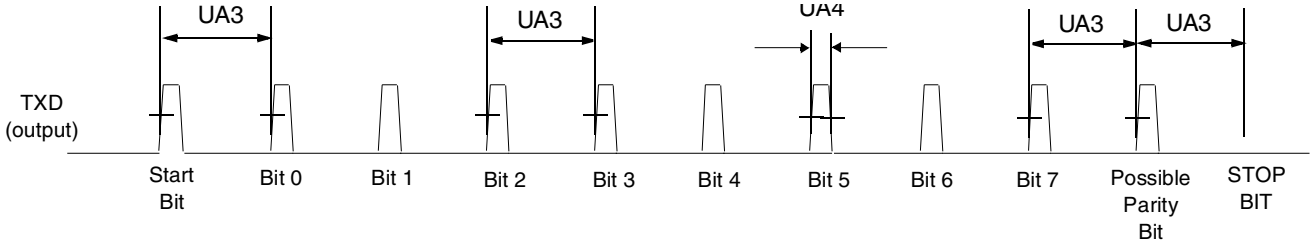


Figure 87. UART IrDA Mode Transmit Timing Diagram

Table 88. UART IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA3	Transmit bit time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR pulse duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16) \times (1/F_{baud\_rate}) + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

3.7.19.2.4 UART IrDA Mode Receive Timing

Figure 88 shows the UART receive timing for IrDA mode, for a format of 8 data bits and 1 stop bit. Table 89 describes the timing parameters (UA5–UA6) shown in the figure.

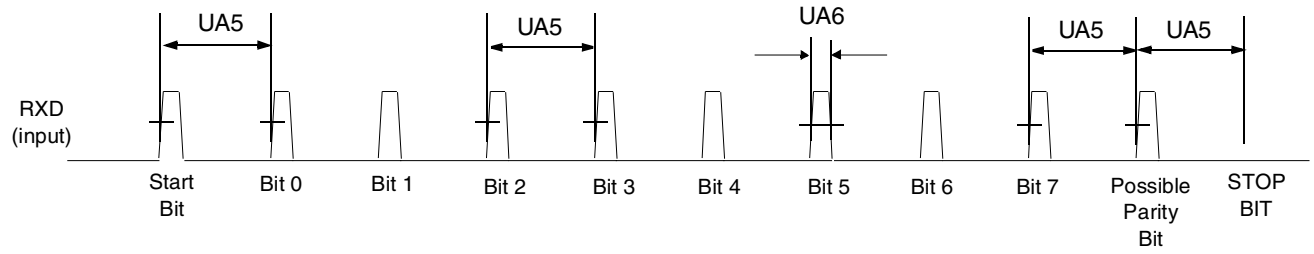


Figure 88. UART IrDA Mode Receive Timing Diagram

Table 89. UART IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA5	Receive bit time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR pulse duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

3.7.20.1.3 VP_VM Bidirectional Mode Timing

Table 94 defines the VP_VM bidirectional mode signals.

Table 94. Signal Definitions—VP_VM Bidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	• Transmit enable, active low
USB_DAT_VP	Out (Tx) In (Rx)	• Tx VP data when USB_TXOE_B is low • Rx VP data when USB_TXOE_B is high
USB_SE0_VM	Out (Tx) In (Rx)	• Tx VM data when USB_TXOE_B low • Rx VM data when USB_TXOE_B high
USB_RCV	In	• Differential Rx data

Figure 93 shows the USB transmit waveform in VP_VM bidirectional mode diagram.

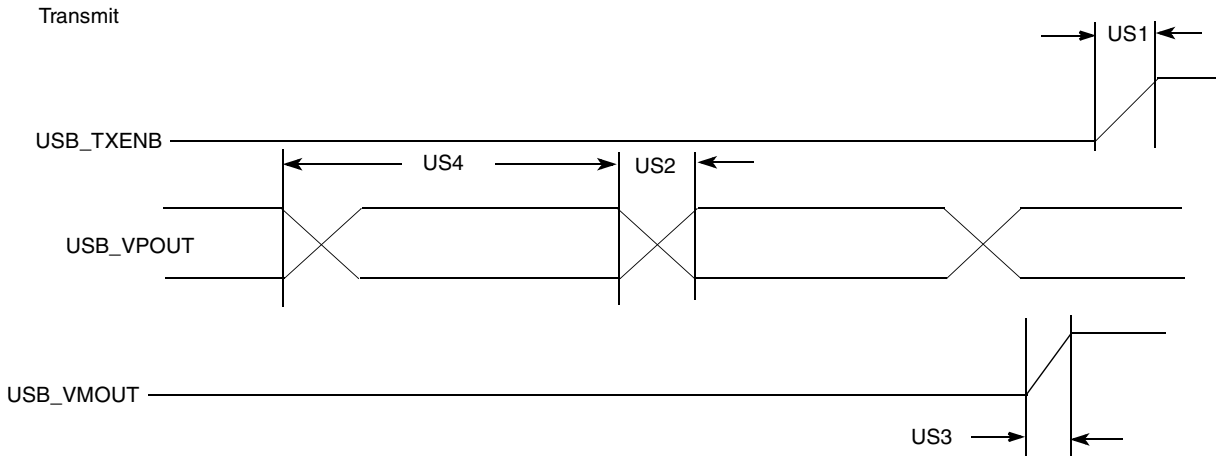


Figure 93. USB Transmit Waveform in VP_VM Bidirectional Mode

Figure 94 shows the USB receive waveform in VP_VM bidirectional mode diagram.

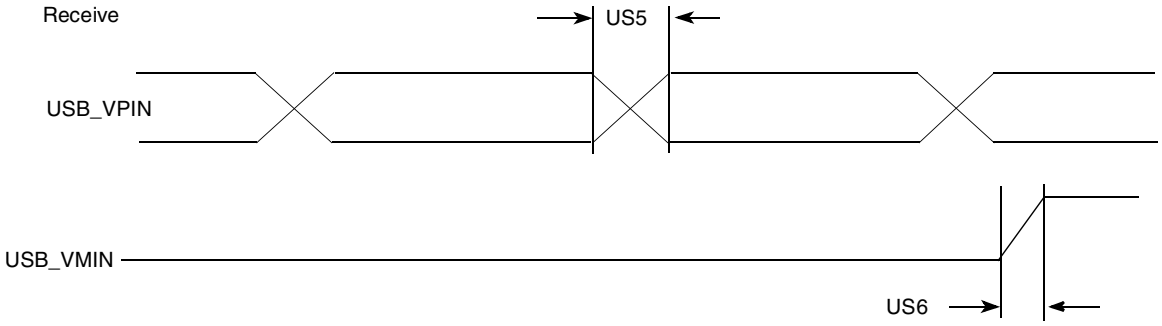


Figure 94. USB Receive Waveform in VP_VM Bidirectional Mode