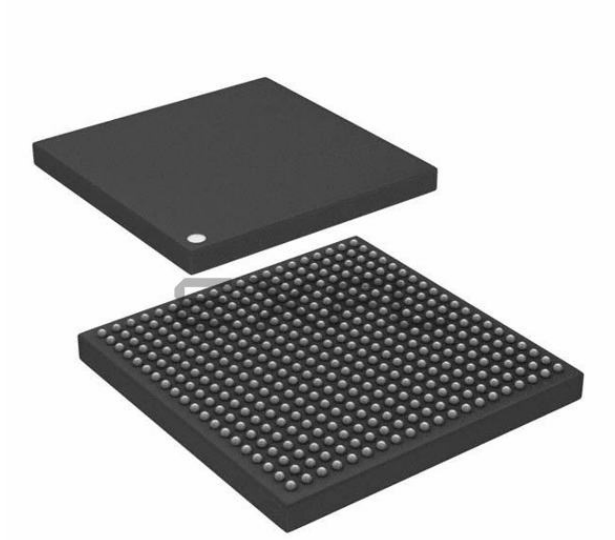

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx253cjm4a

Features of the i.MX25 processor include the following:

- Advanced power management—The heart of the device is a level of power management throughout the IC that enables the multimedia features and peripherals to achieve minimum system power consumption in active and various low-power modes. Power management techniques allow the designer to deliver a feature-rich product that requires levels of power far lower than typical industry expectations.
- Multimedia powerhouse—The multimedia performance of the i.MX25 processor is boosted by a 16 KB L1 instruction and data cache system and further enhanced by an LCD controller (with alpha blending), a CMOS image sensor interface, an A/D controller (integrated touchscreen controller), and a programmable Smart DMA (SDMA) controller.
- 128 Kbytes on-chip SRAM—The additional 128 Kbyte on-chip SRAM makes the device ideal for eliminating external RAM in applications with small footprint RTOS. The on-chip SRAM allows the designer to enable an ultra low power LCD refresh.
- Interface flexibility—The device interface supports connection to all common types of external memories: MobileDDR, DDR, DDR2, NOR Flash, PSRAM, SDRAM and SRAM, NAND Flash, and managed NAND.
- Increased security—Because the need for advanced security for tethered and untethered devices continues to increase, the i.MX25 processor delivers hardware-enabled security features that enable secure e-commerce, Digital Rights Management (DRM), information encryption, robust tamper detection, secure boot, and secure software downloads.
- On-chip PHY—The device includes an HS USB OTG PHY and FS USB HOST PHY.
- Fast Ethernet—For rapid external communication, a Fast Ethernet Controller (FEC) is included.
- i.MX25 only supports Little Endian mode.

Table 3. i.MX25 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
I^2C(3)	I^2C module	Connectivity peripherals	Inter-IC Communication (I^2C) is an industry-standard, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. I^2C is suitable for applications requiring occasional communications over a short distance between many devices. The interface operates up to 100 kbps with maximum bus loading and timing. The I^2C system is a true multiple-master bus, including arbitration and collision detection that prevents data corruption if multiple devices attempt to control the bus simultaneously. This feature supports complex applications with multiprocessor control and can be used for rapid testing and alignment of end products through external connections to an assembly-line computer.
IIM	IC Identification Module	Security	The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, and various control signals requiring a fixed value.
IOMUX	I/O multiplexer	Pins	Each I/O multiplexer provides a flexible, scalable multiplexing solution: • Up to eight output sources multiplexed per pin • Up to four destinations for each input pin • Unselected input paths are held at constant level for reduced power consumption
KPP	Keypad port	Connectivity peripherals	KPP can be used for either keypad matrix scanning or general purpose I/O.
LCDC	LCD Controller	Multimedia peripherals	LCDC provides display data for external gray-scale or color LCD panels. LCDC is capable of supporting black-and-white, gray-scale, passive-matrix color (passive color or CSTN), and active-matrix color (active color or TFT) LCD panels.
MAX	ARM platform multilayer AHB crossbar switch	ARM platform	MAX concurrently supports up to five simultaneous connections between master ports and slave ports. MAX allows for concurrent transactions to occur from any master port to any slave port.
PWM(4)	Pulse width modulation	Connectivity peripherals	The Pulse-Width Modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. The PWM uses 16-bit resolution and a 4x16 data FIFO to generate sound.
SDMA	Smart DMA engine	System control	The SDMA provides DMA capabilities inside the processor. It is a shared module that implements 32 DMA channels.
SIM(2)	Subscriber identity module interface	Connectivity peripherals	The SIM is an asynchronous interface designed to facilitate communication with SIM cards or pre-paid phone cards. This module was designed based on the ISO7816 standard; however, the module does require an external companion controller to allow communication to certain smart cards or to pass certain certifications, such as EMV. The SIM supports only 11 and 12ETU cards and can communicate at the default rate, which is obtained at Fi/Di=372/1. An external companion controller is required to support cards aligned on 10.8 or 11.8ETU and to support other rates, such as those obtained at Fi/Di=372/2 and Fi/Di=372/4.
SJC	Secure JTAG interface	System control peripherals	The System JTAG Controller (SJC) provides debug and test control with maximum security.

Table 3. i.MX25 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SLCD	Smart LCD controller	Multimedia peripherals	The SLCDC module transfers data from the display memory buffer to the external display device.
SPBA	Shared peripheral bus arbiter	System control	The SPBA controls access to the shared peripherals. It supports shared peripheral ownership and access rights to an owned peripheral.
SSI(2)	I2S/SSI/AC97 interface	Connectivity peripherals	The SSI is a full-duplex serial port that allows the processor to communicate with a variety of serial protocols, including the Freescale Semiconductor SPI standard and the inter-IC sound bus standard (I2S). The SSIs interface to the AUDMUX for flexible audio routing.
TSC (and ADC)	Touchscreen controller (and A/D converter)	Multimedia peripherals	The touchscreen controller and associated Analog-to-Digital Converter (ADC) together provide a resistive touchscreen solution. The module implements simultaneous touchscreen control and auxiliary ADC operation for temperature, voltage, and other measurement functions.
UART(5)	UART interface	Connectivity peripherals	Each of the UART modules supports the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, one or two stop bits, programmable parity (even, odd, or none) • Programmable baud rates up to 4 MHz. This is a higher maximum baud rate than the 1.875 MHz specified by the TIA/EIA-232-F standard and previous Freescale UART modules. 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA-1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOTG USBHOST	High-speed USB on-the-go	Connectivity peripherals	The USB module provides high-performance USB On-The-Go (OTG) and host functionality (up to 480 Mbps), compliant with the USB 2.0 specification, the OTG supplement, and the ULPI 1.0 Low Pin Count specification. The module has DMA capabilities for handling data transfer between internal buffers and system memory. An OTG HS PHY and HOST FS PHY are also integrated.

2.1 Special Signal Considerations

Special signal considerations are listed in Table 4. The package contact assignment is found in Section 4, "Package Information and Contact Assignment." Signal descriptions are provided in the reference manual.

Table 4. Signal Considerations

Signal	Description
BAT_VDD	DryIce backup power supply input.
CLK0	Clock-out pin; renders the internal clock visible to users for debugging. The clock source is controllable through CRM registers. This pin can also be configured (through muxing) to work as a normal GPIO.
CLK_SEL	Used to select the ARM clock source from MPLL out or from external EXT_ARMCLK. In normal operation, CLK_SEL should be connected to GND.
EXT_ARMCLK	Primarily for Freescale factory use. There is no internal on-chip pull-up/down on this pin, so it must be externally connected to GND or VDD. Aside from factory use, this pin can also be configured (through muxing) to work as a normal GPIO.

3.6.3.2 DDR_TYPE = 01 SDRAM I/O AC Parameters and Requirements

Table 27 shows AC parameters for SDRAM I/O.

Table 27. AC Parameters for SDRAM I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	50	60	%
Clock frequency[1]	f	—	—	—	133	MHz
Output pad transition times[1] (max. drive)	tpr	25 pF 50 pF	0.82/0.87 1.56/1.67	1.14/1.13 2.13/2.09	1.62/1.50 3.015/2.77	ns
Output pad transition times[1] (high drive)	tpr	25 pF 50 pF	1.23/1.31 2.31/2.47	1.71/1.68 3.22/3.12	2.39/2.22 4.53/4.16	ns
Output pad transition times[1] (standard drive)	tpr	25 pF 50 pF	2.44/2.60 4.65/4.99	3.38/3.27 6.38/6.23	4.73/4.38 9.05/8.23	ns
Output pad propagation delay[1] (max. drive), 50%–50%	tpo	15 pF 35 pF	0.97/1.19 2.85/3.21	1.69/0.75 2.02/2.30	2.17/2.46 2.93/3.27	ns
Output pad propagation delay[1] (high drive), 50%–50%	tpo	15 pF 35 pF	1.15/1.39 3.57/3.91	1.72/1.93 2.54/2.85	2.51/2.77 3.66/3.97	ns
Output pad propagation delay[1] (standard drive), 50%–50%	tpo	15 pF 35 pF	2.01/1.57 5.73/6.05	2.45/2.69 4.10/4.51	3.54/3.77 5.84/6.13	ns
Output pad propagation delay[1] (max. drive), 40%–60%	tpo	15 pF 35 pF	1.06/1.26 1.38/1.38	1.53/1.73 1.96/2.23	2.18/2.47 2.78/3.12	ns
Output pad propagation delay[1] (high drive), 40%–60%	tpo	15 pF 35 pF	1.15/1.20 1.75/1.67	1.72/1.93 2.37/2.66	2.45/2.71 3.35/3.67	ns
Output pad propagation delay[1] (standard drive), 40%–60%	tpo	15 pF 35 pF	1.91/2.01 2.88/2.56	2.30/2.52 3.59/3.97	3.26/3.50 5.06/5.36	ns
Output enable to output valid delay[1] (max. drive), 50%–50%	tpv	15 pF 35 pF	0.90/1.27 1.07/1.77	1.44/1.89 1.66/2.51	2.19/2.87 2.51/3.69	ns
Output enable to output valid delay[1] (high drive), 50%–50%	tpv	15 pF 35 pF	1.01/1.48 1.37/2.33	1.58/2.16 2.06/3.09	2.38/3.23 3.06/4.46	ns
Output enable to output valid delay[1] (standard drive), 50%–50%	tpv	15 pF 35 pF	1.32/2.14 2.04/3.67	2.02/3.00 3.00/4.91	3.01/4.36 4.40/6.90	ns
Output enable to output valid delay[1] (max. drive), 40%–60%	tpv	15 pF 35 pF	1.03/1.34 1.16/1.74	1.54/1.94 1.74/2.44	2.26/2.88 2.55/3.54	ns
Output enable to output valid delay[1] (high drive), 40%–60%	tpv	15 pF 35 pF	1.11/1.51 1.39/2.10	1.65/2.15 2.03/2.89	2.43/3.16 2.95/4.13	ns
Output enable to output valid delay[1] (standard drive), 40%–60%	tpv	15 pF 35 pF	1.35/2.03 1.91/3.23	1.99/2.83 2.76/4.30	2.89/4.03 3.98/6.01	ns
Output pad slew rate[2] (max. drive)	tps	25 pF 50 pF	1.11/1.20 0.97/0.65	1.74/1.75 0.92/0.94	2.42/2.46 1.39/1.30	V/ns
Output pad slew rate[2] (high drive)	tps	25 pF 50 pF	0.76/0.80 0.40/0.43	1.16/1.19 0.61/0.63	1.76/1.66 0.93/0.87	V/ns

3.6.3.3 DDR_TYPE = 10 Max Setting I/O AC Parameters and Requirements

Table 29 shows AC parameters for DDR2 I/O.

Table 29. AC Parameters for DDR2 I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	50	60	%
Clock frequency	f	—	—	—	133	MHz
Output pad transition times[1]	tpr	25 pF 50 pF	0.53/0.52 1.01/0.98	0.80/0.72 1.49/1.34	1.19/1.04 2.21/1.90	ns
Output pad propagation delay, 50%–50%[1]	tpo	25 pF 50 pF	0.93/1.25 1.26/1.54	1.56/1.70 2.07/2.19	2.52/2.53 3.29/3.24	ns
Output pad propagation delay, 40%–60%[1]	tpo	25 pF 50 pF	1.01/1.17 1.27/1.53	1.60/1.75 2.00/2.14	2.49/2.52 3.11/3.10	ns
Output enable to output valid delay, 50%–50%[1]	tpv	25 pF 50 pF	1.30/1.19 1.62/1.54	2.17/1.81 2.56/2.29	3.35/2.84 3.35/2.54	ns
Output enable to output valid delay, 40%–60%[1]	tpv	25 pF 50 pF	1.39/1.27 1.64/1.55	2.13/1.86 2.62/2.23	3.38/2.83 4.14/2.38	ns
Output pad slew rate[2]	tps	25 pF 50 pF	0.86/0.98 0.46/054	1.35/1.5 0.72/0.81	2.15/2.19 1.12/1.16	V/ns
Output pad dI/dt[3]	tdit	25 pF 50 pF	65 70	157 167	373 396	mA/ns
Input pad transition times[4]	trfi	1.0 pF	0.07/0.08	0.10/0.12	0.17/0.20	ns
Input pad propagation delay, 50%–50%[4]	tpi	1.0 pF	0.83/0.99	1.23/1.49	1.79/2.04	ns
Input pad propagation delay, 40%–60%[4]	tpi	1.0 pF	1.65/1.81	2.05/2.31	2.60/2.84	ns

1 Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 1. V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.9 V and –40 °C. Input transition time from core is 1 ns (20%–80%).

2 Minimum condition for tps: wcs model, 1.1 V, I/O 1.7 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

3 Maximum condition for tdit: bcs model, 1.3 V, I/O 1.9 V, and –40 °C.

4 Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.7 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.9 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

Table 30 shows AC parameters for DDR2 pbijtov18_33_ddr_clk I/O.

Table 30. AC Parameters for DDR2 pbijtov18_33_ddr_clk I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	50	60	%
Clock frequency	f	—	—	—	133	MHz
Output pad transition times[1]	tpr	25 pF 50 pF	0.53/0.52 1.01/0.98	0.80/0.72 1.49/1.34	1.19/1.04 2.21/1.90	ns
Output pad propagation delay[1], 50%–50% input signals and crossing of output signals	tpo	25 pF 50 pF	1.3/1.21 1.59/1.5	1.97/1.84 2.37/2.24	2.91/2.71 3.48/3.28	ns

3.7 Module Timing and Electrical Parameters

This section contains the timing and electrical parameters for i.MX25 modules.

3.7.1 1-Wire Timing Parameters

Figure 7 shows the reset and presence pulses (RPP) timing for 1-Wire.

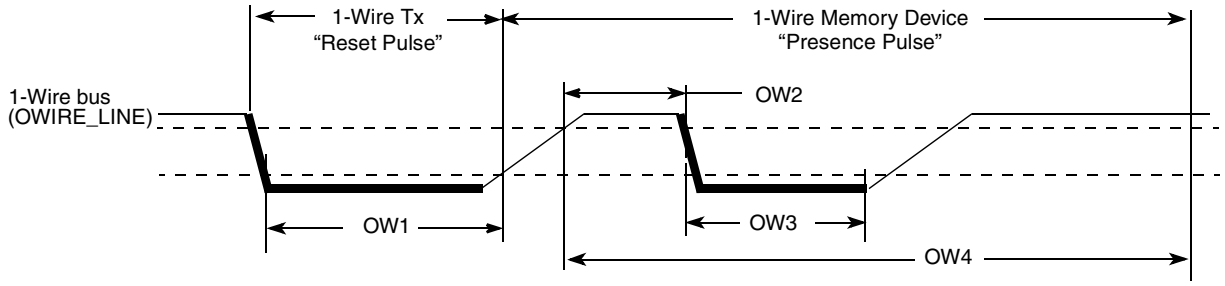


Figure 7. 1-Wire RPP Timing Diagram

Table 32 lists the RPP timing parameters.

Table 32. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min.	Typ.	Max.	Units
OW1	Reset Time Low	t_{RSTL}	480	511	—	µs
OW2	Presence Detect High	t_{PDH}	15	—	60	µs
OW3	Presence Detect Low	t_{PDL}	60	—	240	µs
OW4	Reset Time High	t_{RSTH}	480	512	—	µs

Figure 8 shows write 0 sequence timing, and Table 33 describes the timing parameters (OW5–OW6) that are shown in the figure.

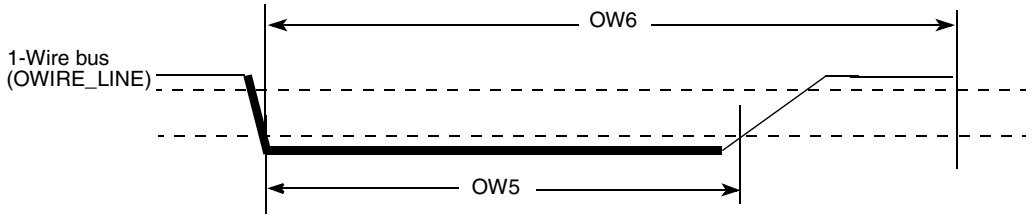


Figure 8. Write 0 Sequence Timing Diagram

Table 33. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW5	Write 0 Low Time	t_{WR0_low}	60	100	120	µs
OW6	Transmission Time Slot	t_{SLOT}	OW5	117	120	µs

To meet timing requirements, a number of timing parameters must be controlled. See Table 38 for details on timing parameters for MDMA read and write modes.

Table 38. Timing Parameters for MDMA Read and Write Modes

ATA Parameter	MDMA Read[1] and Write[2] Timing Parameters	Relation	Adjustable Parameter(s)
tm, ti	tm	tm(min.) = ti(min.) = time_m × T – (tskew1 + tskew2 + tskew5)	time_m
td	td, td1	td1(min.) = td(min.) = time_d × T – (tskew1 + tskew2 + tskew6)	time_d
tk	tk	tk(min.) = time_k × T – (tskew1 + tskew2 + tskew6)	time_k
t0	—	t0(min.) = (time_d + time_k) × T	time_d, time_k
tg(read)	tgr	tgr(min.–read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 tgr(min.–drive) = td – te(drive)	time_d
tf(read)	tfr	tfr(min.–drive) =0 k	—
tg(write)	—	tg(min.–write) = time_d × T –(tskew1 + tskew2 + tskew5)	time_d
tf(write)	—	tf(min.–write) = time_k × T – (tskew1 + tskew2 + tskew6)	time_k
tL	—	tL(max.) = (time_d + time_k–2) × T – (tsu + tco + 2 × tbuf + 2 × tcable2)	time_d, time_k[3]
tn, tj	tkjn	tn= tj= tkjn = (max.(time_k,. time_jn) × T – (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

1 See Figure 13.

2 See Figure 14.

3 tk1 in the UDMA figures equals (tk –2 × T).

3.7.2.3 Ultra DMA (UDMA) Mode Timing

UDMA mode timing is more complicated than PIO mode or MDMA mode. In this section, timing diagrams for UDMA in- and out-transfers are provided.

Table 53. ΔtDS1, ΔtDH1 Derating Values for DDR2-400, DDR2-533[1,2,3] (continued)

		DQS Single-Ended Slew Rate																	
DQ Slew Rate V/ns	2.0	188	188	167	146	125	63	—	—	—	—	—	—	—	—	—	—	—	—
	1.5	146	167	125	125	83	42	81	43	—	—	—	—	—	—	—	—	—	—
	1.0	63	125	42	83	0	0	–2	1	–7	–13	—	—	—	—	—	—	—	—
	0.9	—	—	31	69	–11	–14	–13	–13	–18	–27	–29	–45	—	—	—	—	—	—
	0.8	—	—	—	—	–25	–31	–27	–30	–32	–44	–43	–62	–60	–86	—	—	—	—
	0.7	—	—	—	—	—	—	–45	–53	–50	–67	–61	–85	–78	–109	–108	–152	—	—
	0.6	—	—	—	—	—	—	—	—	–74	–96	–85	–114	–102	–138	–132	–181	–183	–246
	0.5	—	—	—	—	—	—	—	—	—	—	–128	–156	–145	–180	–175	–223	–226	–288
	0.4	—	—	—	—	—	—	—	—	—	—	—	—	–210	–243	–240	–286	–291	–351

1 All units in 'ps'.

2 Test conditions are at capacitance=15pF for DDR PADS. Recommended drive strengths are medium for SDCLK and high for address and controls.

3 SDRAM CLK and DQS related parameters are measured from the 50% point. That is, high is defined as 50% of the signal value, and low is defined as 50% of the signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and SDCLK (inverted clock).

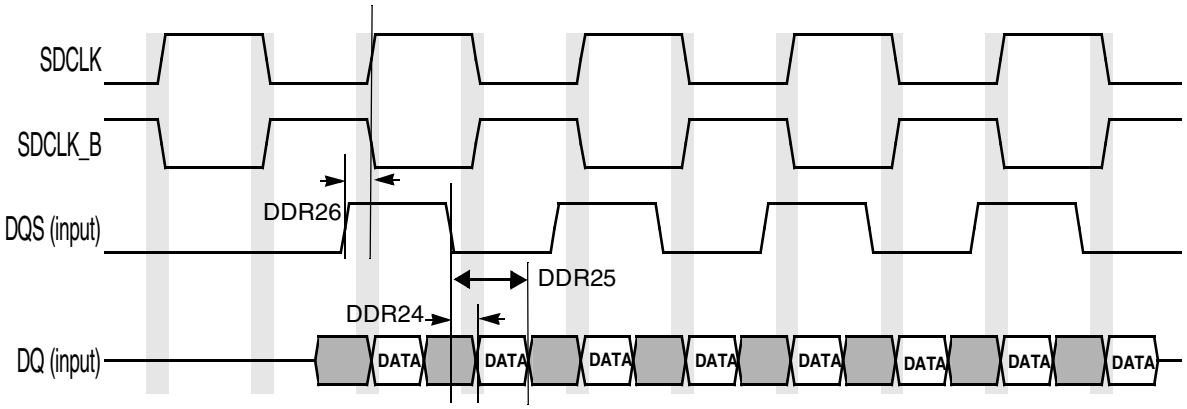


Figure 33. DDR2 SDRAM DQ vs. DQS and SDCLK READ Cycle Timing Diagram

Table 54. DDR2 SDRAM Read Cycle Parameter Table[1,2]

ID	Parameter	Symbol	DDR2-400		Unit
			Min.	Max.	
DDR24	DQS - DQ Skew (defines the Data valid window in read cycles related to DQS)	t_{DQSQ}	—	0.6	ns
DDR25	DQS DQ in HOLD time from DQS[3]	t_{QH}	2.5	—	ns
DDR26	DQS output access time from SDCLK posedge	t_{DQSCK}	–0.5	0.5	ns

1 Test conditions are at capacitance=15 pF for DDR PADS. Recommended drive strengths are medium for SDCLK and high for address and controls.

3.7.9.3 RMII Mode Timing

In RMII mode, FEC_TX_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. FEC_RX_DV is used as the CRS_DV in RMII. Other signals under RMII mode include FEC_TX_EN, FEC_TXD[1:0], FEC_RXD[1:0] and FEC_RX_ER.

Figure 59 shows RMII mode timings. Table 66 describes the timing parameters (M16–M21) shown in the figure.

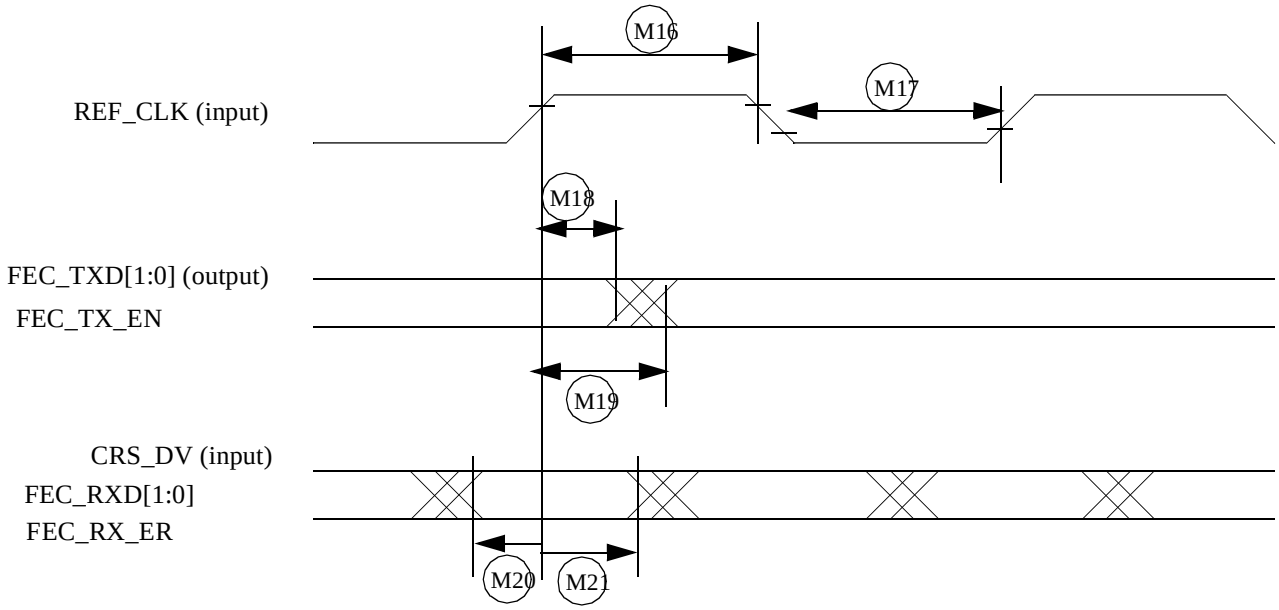


Figure 59. RMII Mode Signal Timing Diagram

Table 66. RMII Signal Timing

ID	Characteristic	Min.	Max.	Unit
M16	REF_CLK(FEC_TX_CLK) pulse width high	35%	65%	REF_CLK period
M17	REF_CLK(FEC_TX_CLK) pulse width low	35%	65%	REF_CLK period
M18	REF_CLK to FEC_TXD[1:0], FEC_TX_EN invalid	3	—	ns
M19	REF_CLK to FEC_TXD[1:0], FEC_TX_EN valid	—	12	ns
M20	FEC_RXD[1:0], CRS_DV(FEC_RX_DV), FEC_RX_ER to REF_CLK setup	2	—	ns
M21	REF_CLK to FEC_RXD[1:0], FEC_RX_DV, FEC_RX_ER hold	2	—	ns

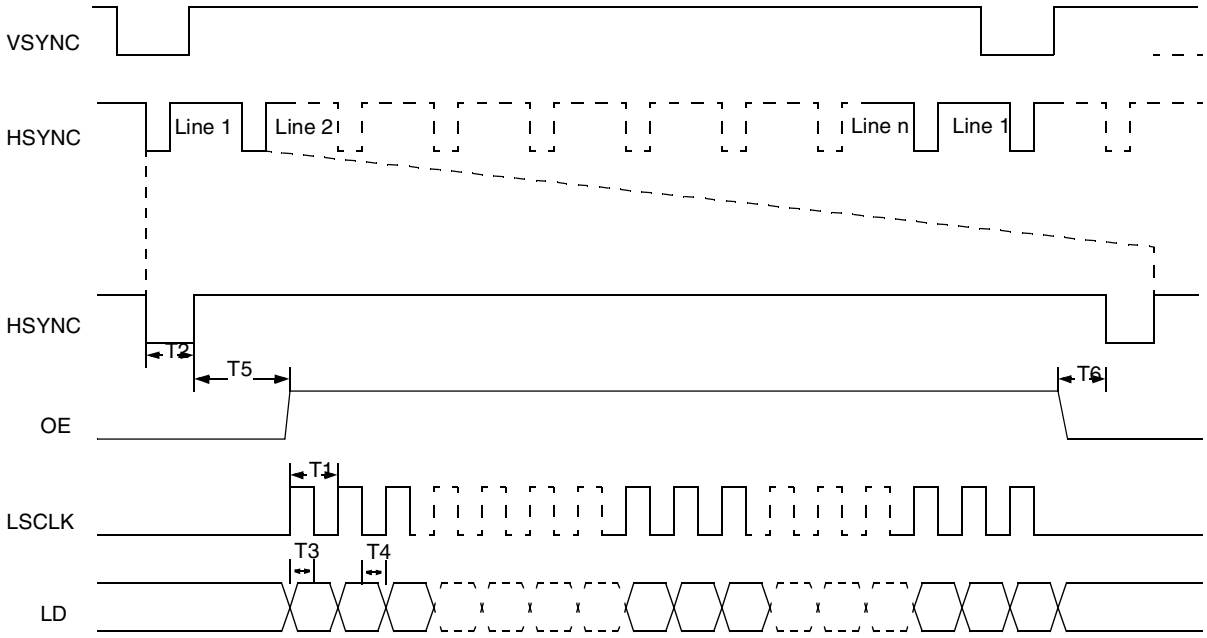


Figure 66. LCDC TFT Mode Timing Diagram

Table 72. LCDC TFT Mode Timing Parameters

ID	Description	Min.	Ma	Unit
T1	Pixel clock period	22.5	1000	ns
T2	HSYNC width	1	—	T[1]
T3	LD setup time	5	—	ns
T4	LD hold time	5	—	ns
T5	Delay from the end of HSYNC to the beginning of the OE pulse	3	—	T[1]
T6	Delay from end of OE to the beginning of the HSYNC pulse	1	—	T[1]

1 T is pixel clock period

3.7.13 Pulse Width Modulator (PWM) Timing Parameters

Figure 67 depicts the timing of the PWM, and Table 73 lists the PWM timing characteristics.

The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse width modulator output (PWMO) external pin.

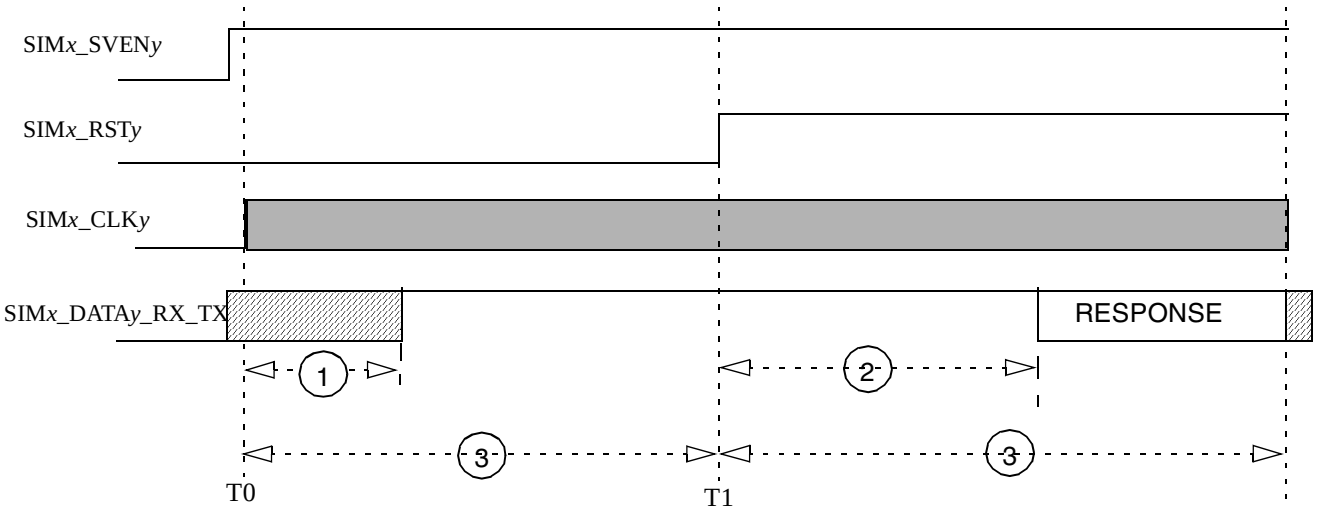


Figure 70. Active-Low-Reset SIM Card Reset Sequence

Table 76 defines the general timing requirements for the SIM interface.

Table 76. Timing Specifications, Active-Low-Reset SIM Card Reset Sequence

Ref No.	Min.	Max.	Unit
1	—	200	clk cycles
2	400	40,000	clk cycles
3	40,000	—	clk cycles

3.7.14.2 SIM Power-Down Sequence

Figure 71 shows the SIM interface power-down AC timing diagram. Table 77 shows the timing requirements for parameters (SI7–SI10) shown in the figure.

The power-down sequence for the SIM interface is as follows:

- SIM*x*_SIMPD*y* port detects the removal of the SIM Card
- SIM*x*_RST*y* is negated
- SIM*x*_CLK*y* is negated
- SIM*x*_DATA*y*_RX_TX is negated
- SIM*x*_SVEN*y* is negated

Each of the above steps requires one CKIL period (usually 32 kHz). Power-down may be initiated by a SIM card removal detection; or it may be launched by the processor.

Table 80. SLCDC Parallel Interface Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{cyc}	Parallel clock cycle time	78 (±) t_{prop}	—	4923	ns
t_{ds}	Data setup time	(t_{cyc} / 2) (±) t_{prop}	—	—	—
t_{dh}	Data hold time	(t_{cyc} / 2) (±) t_{prop}	—	—	—
t_{rss}	Register select setup time	(t_{cyc} / 2) (±) t_{prop}	—	—	—
t_{rsh}	Register select hold time	(t_{cyc} / 2) (±) t_{prop}	—	—	—

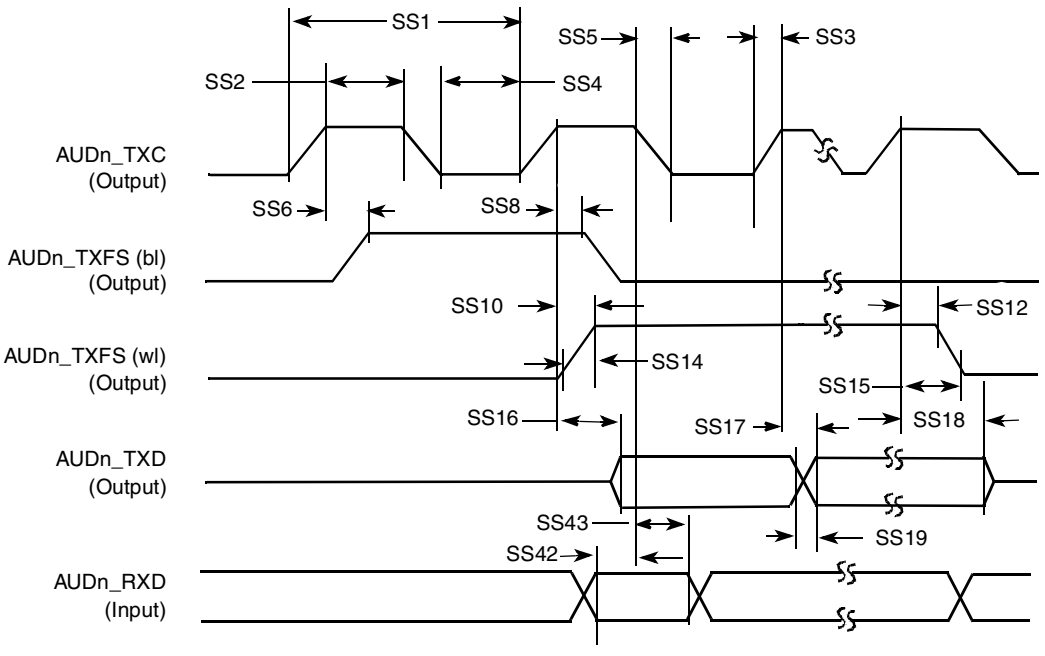
3.7.17 Synchronous Serial Interface (SSI) Timing

The following subsections describe SSI timing in four cases:

- Transmitter with external clock
- Receiver with external clock
- Transmitter with internal clock
- Receiver with internal clock

3.7.17.1 SSI Transmitter Timing with Internal Clock

Figure 78 shows the timing for SSI transmitter with internal clock, and Table 81 describes the timing parameters (SS1–SS52).



Note: SRXD Input in Synchronous mode only

Figure 78. SSI Transmitter with Internal Clock Timing Diagram

Table 82. SSI Receiver Timing with Internal Clock (continued)

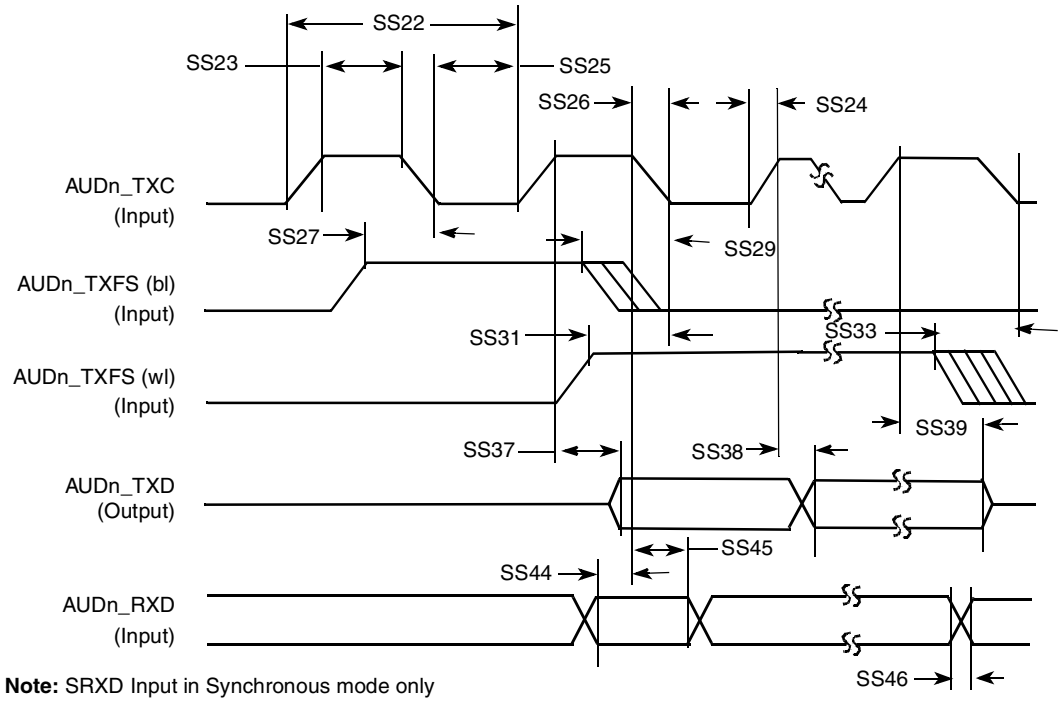
ID	Parameter	Min.	Max.	Unit
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

Note:

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on pads when SSI is being used for a data transfer.
- ”Tx” and “Rx” refer to the transmit and receive sections of the SSI.
- For internal frame sync operation using external clock, the FS timing is the same as that of Tx Data (for example, during AC97 mode of operation).

3.7.17.3 SSI Transmitter Timing with External Clock

Figure 80 shows the timing for the SSI transmitter with external clock. Table 83 describes the timing parameters (SS22-SS46) shown in the figure.



Note: SRXD Input in Synchronous mode only

Figure 80. SSI Transmitter with External Clock Timing Diagram

3.7.19.1 UART RS-232 Serial Mode Timing

3.7.19.1.1 UART Transmit Timing in RS-232 Serial Mode

Figure 85 shows the UART transmit timing in RS-232 serial mode, showing only 8 data bits and 1 stop bit. Table 86 describes the timing parameter (UA1) shown in the figure.

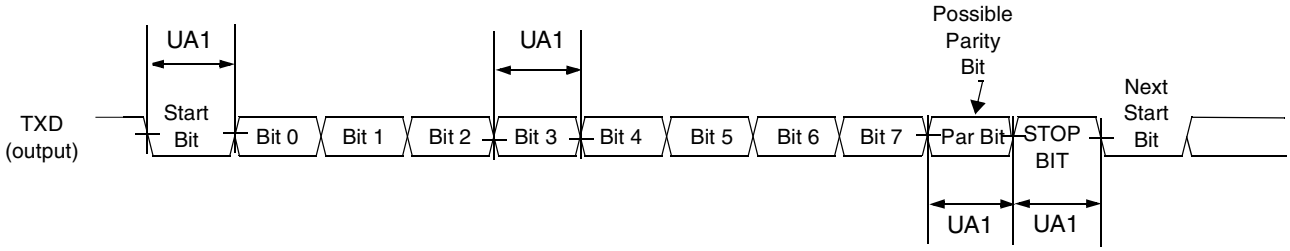


Figure 85. UART RS-232 Serial Mode Transmit Timing Diagram

Table 86. UART RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

3.7.19.1.2 UART Receive Timing in RS-232 Serial Mode

Figure 86 shows the UART receive timing in RS-232 serial mode, showing only 8 data bits and 1 stop bit. Table 87 describes the timing parameter (UA2) shown in the figure.

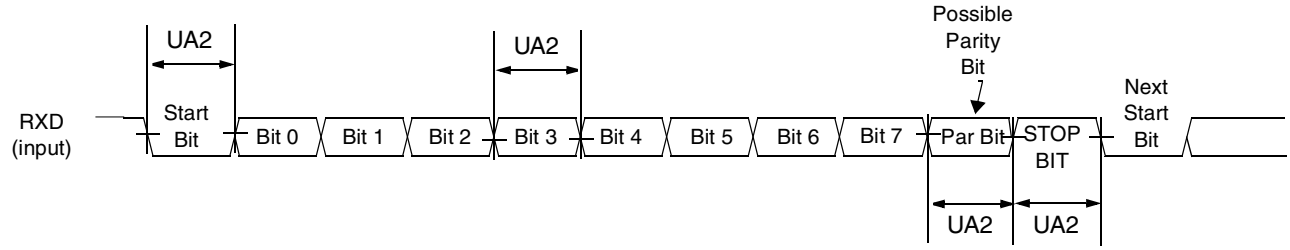


Figure 86. UART RS-232 Serial Mode Receive Timing Diagram

Table 87. UART RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA2	Receive bit time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

Table 97 shows the timing specifications for USB in VP_VM unidirectional mode.

Table 97. USB Timing Specifications in VP_VM Unidirectional Mode

No.	Parameter	Signal	Direction	Min.	Max.	Unit	Conditions/ Reference Signal
US30	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US31	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US32	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US33	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US34	Tx high overlap	USB_SE0_VM	Out	0.0	—	ns	USB_DAT_VP
US35	Tx low overlap	USB_SE0_VM	Out	—	0.0	ns	USB_DAT_VP
US36	Enable delay	USB_DAT_VP USB_SE0_VM	In	—	8.0	ns	USB_TXOE_B
US37	Disable delay	USB_DAT_VP USB_SE0_VM	In	—	10.0	ns	USB_TXOE_B
US38	Rx rise/fall time	USB_VP1	In	—	3.0	ns	35 pF
US39	Rx rise/fall time	USB_VM1	In	—	3.0	ns	35 pF
US40	Rx skew	USB_VP1	Out	–4.0	+4.0	ns	USB_SE0_VM
US41	Rx skew	USB_RCV	Out	–6.0	+2.0	ns	USB_DAT_VP

3.7.20.2 USB Parallel Interface Timing

Table 98 defines the USB parallel interface signals.

Table 98. Signal Definitions for USB Parallel Interface

Name	Direction	Signal Description
USB_Clk	In	Interface clock—All interface signals are synchronous to USB_Clk
USB_Data[7:0]	I/O	Bidirectional data bus, driven low by the link during idle—Bus ownership is determined by the direction
USB_Dir	In	Direction—Control the direction of the data bus
USB_Stp	Out	Stop—The link asserts this signal for one clock cycle to stop the data stream currently on the bus
USB_Nxt	In	Next—The PHY asserts this signal to throttle the data

Figure 97 shows the USB parallel mode transmit/receive waveform. Table 99 describes the timing parameters (USB15–USB17) shown in the figure.

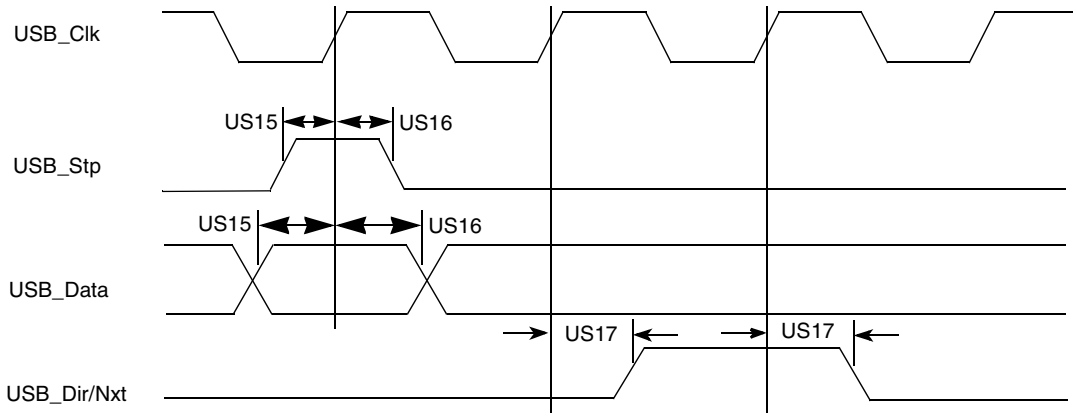


Figure 97. USB Parallel Mode Transmit/Receive Waveform

Table 99. USB Timing Specification in Parallel Mode

ID	Parameter	Min.	Max.	Unit	Conditions/Reference Signal
US15	Setup time (Dir&Nxt in, Data in)	6.0	—	ns	10 pF
US16	Hold time (Dir&Nxt in, Data in)	0.0	—	ns	10 pF
US17	Output delay time (Stp out, Data out	—	9.0	ns	10 pF

4 Package Information and Contact Assignment

4.1 400 MAPBGA—Case 17x17 mm, 0.8 mm Pitch

Figure 98 shows the 17×17 mm i.MX25 production package. The following notes apply to Figure 98:

- All dimensions in millimeters.
- Dimensioning and tolerancing per ASME Y14.5M-1994.
- Maximum solder bump diameter measured parallel to datum A.
- Datum A, the seating plane, is determined by the spherical crowns of the solder bumps.
- Parallelism measurement shall exclude any effect of mark on top surface of package.

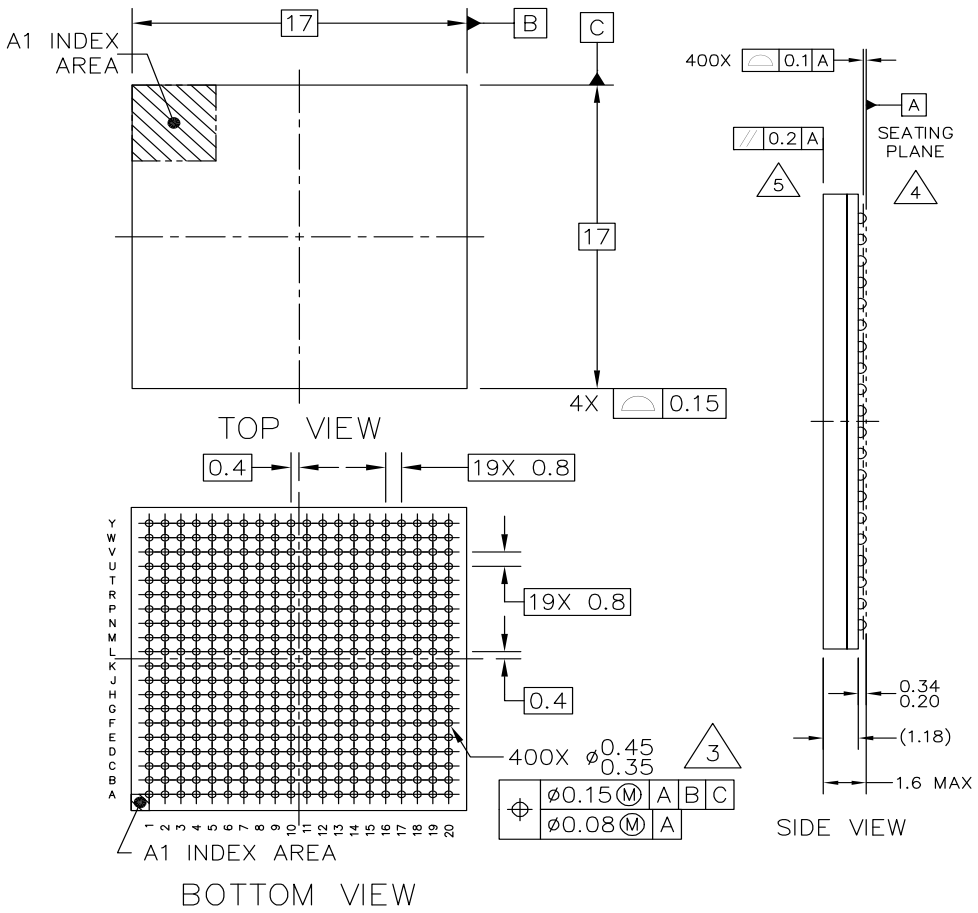


Figure 98. 17×17 i.MX25 Production Package

4.2 Ground, Power, Sense, and Reference Contact Assignments Case 17x17 mm, 0.8 mm Pitch

Table 100 shows the 17×17 mm package ground, power, sense, and reference contact assignments.

Table 100. 17×17 mm Package Ground, Power Sense, and Reference Contact Assignments

Contact Name	Contact Assignment
BATT_VDD	P10
FUSE_VDD	T17
MPLL_GND	U17
MPLL_VDD	U18
NGND_ADC	Y13
NVCC_ADC	W13
NVCC_CRM	N14
NVCC_CSI	J13, J14

4.5 347 MAPBGA—Case 12 x 12 mm, 0.5 mm Pitch

Figure 99 shows the 12×12 mm i.MX25 production package. The following notes apply to Figure 99:

- All dimensions in millimeters.Dimensioning and tolerancing per ASME Y14.5M-1994.
- Maximum solder ball diameter measured parallel to datum A.
- Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
- Parallelism measurement shall exclude any effect of mark on package's top surface.

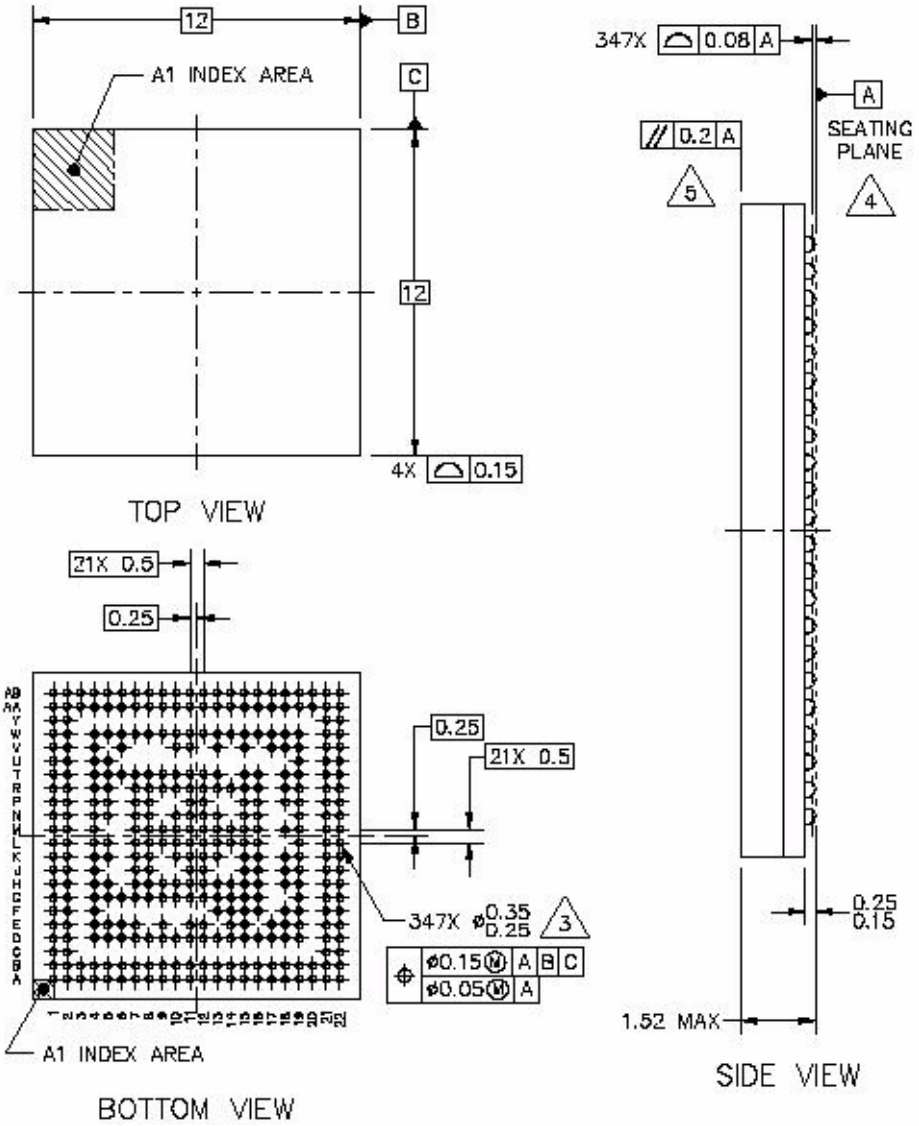


Figure 99. 12×12 mm i.MX25 Production Package

Table 105. 12x12 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
FEC_RDATA0	M4	MISC	GPIO	INPUT	100 KΩ Pull-Down
FEC_RDATA1	N2	MISC	GPIO	INPUT	100 KΩ Pull-Down
FEC_RX_DV	L5	MISC	GPIO	INPUT	100 KΩ Pull-Down
FEC_TX_CLK	N1	MISC	GPIO	INPUT	100 KΩ Pull-Down
RTCK	W13	JTAG	GPIO	OUTPUT	Low
TCK	AA13	JTAG	GPIO	INPUT	100 KΩ Pull-Down
TMS	AA12	JTAG	GPIO	INPUT	47 KΩ Pull-Up
TDI	W12	JTAG	GPIO	INPUT	47 KΩ Pull-Up
TDO	AA11	JTAG	GPIO	INPUT	-
TRSTB	AB14	JTAG	GPIO	INPUT	47 KΩ Pull-Up
DE_B	W11	JTAG	GPIO	INPUT	47 KΩ Pull-Up
SJC_MOD	AB11	JTAG	GPIO	INPUT	100 KΩ Pull-Up
USBPHY1_VBUS	K22	USBPHY1	ANALOG	ANALOG	-
USBPHY1_DP	K21	USBPHY1	ANALOG	ANALOG	-
USBPHY1_DM	J21	USBPHY1	ANALOG	ANALOG	-
USBPHY1_UID	J22	USBPHY1	ANALOG	ANALOG	-
USBPHY1_RREF	L19	USBPHY1_BIAS	ANALOG	ANALOG	-
USBPHY2_DM	W18	USBPHY2	ANALOG	ANALOG	-
USBPHY2_DP	W17	USBPHY2	ANALOG	ANALOG	-
GPIO_A	T22	CRM	GPIO	INPUT	-
GPIO_B	P21	CRM	GPIO	INPUT	100 KΩ Pull-Down
GPIO_C	U22	CRM	GPIO	INPUT	100 KΩ Pull-Down
GPIO_D	P19	CRM	GPIO	INPUT	-

Table 105. 12x12 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
GPIO_E	R21	CRM	GPIO	INPUT	100 KΩ Pull-Up
GPIO_F	R19	CRM	GPIO	INPUT	-
EXT_ARMCLK	V22	CRM	GPIO	INPUT	-
UPLL_BYPCLK	U21	CRM	GPIO	INPUT	-
VSTBY_REQ	T21	CRM	GPIO	OUTPUT	Low
VSTBY_ACK[3]	W22	CRM	GPIO	OUTPUT	Low
POWER_FAIL	T19	CRM	GPIO	INPUT	100 KΩ Pull-Down
RESET_B	U19	CRM	GPIO	INPUT	100 KΩ Pull-Up
POR_B	V21	CRM	GPIO	INPUT	100 KΩ Pull-Up
CLKO	Y22	CRM	GPIO	OUTPUT	Low
BOOT_MODE0[2]	AA22	CRM	GPIO	INPUT	100 KΩ Pull-Down
BOOT_MODE1[2]	W21	CRM	GPIO	INPUT	100 KΩ Pull-Down
CLK_SEL	AA20	CRM	GPIO	INPUT	100 KΩ Pull-Down
TEST_MODE	AA19	CRM	GPIO	INPUT	100 KΩ Pull-Down
OSC24M_EXTAL	AB19	OSC24M	ANALOG	ANALOG	-
OSC24M_XTAL	AB20	OSC24M	ANALOG	ANALOG	-
OSC32K_EXTAL	AB13	DRYICE	ANALOG	ANALOG	-
OSC32K_XTAL	AB12	DRYICE	ANALOG	ANALOG	-
TAMPER_A	V11	DRYICE	ANALOG	ANALOG	-
TAMPER_B	V13	DRYICE	ANALOG	ANALOG	-
MESH_C	T13	DRYICE	ANALOG	ANALOG	-
MESH_D	R13	DRYICE	ANALOG	ANALOG	-
OSC_BYP	AB15	DRYICE	ANALOG	ANALOG	-
XP	AA18	ADC	ANALOG	ANALOG	-
XN	AA16	ADC	ANALOG	ANALOG	-
YP	AB17	ADC	ANALOG	ANALOG	-
YN	W15	ADC	ANALOG	ANALOG	-