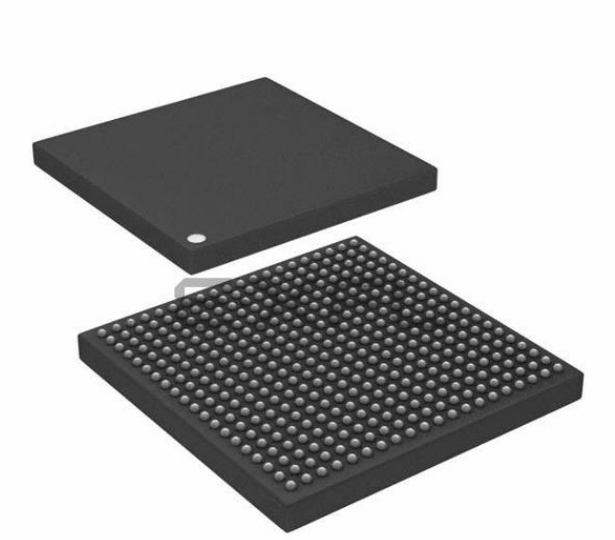

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-20°C ~ 70°C (TA)
Security Features	-
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx253djm4

1.1 Ordering Information

Table 1 provides ordering information for the i.MX25.

Table 1. Ordering Information

Description	Part Number	Silicon Version	Projected Temperature Range (°C)	Package	Ballmap
i.MX253	MCIMX253DVM4	1.1	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257DVM4	1.1	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX253	MCIMX253CVM4	1.1	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257CVM4	1.1	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX258	MCIMX258CVM4	1.1	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX253	MCIMX253DJM4	1.1	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257DJM4	1.1	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX253	MCIMX253CJM4	1.1	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257CJM4	1.1	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX258	MCIMX258CJM4	1.1	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX253	MCIMX253DJM4A	1.2	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257DJM4A	1.2	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257DJM4AR2	1.2	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX253	MCIMX253CJM4A	1.2	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257CJM4A	1.2	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX258	MCIMX258CJM4A	1.2	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257CJN4A	1.2	–40 to +85	12 x 12mm, 0.5mm pitch, MAPBGA-347	Table 107

NOTE

- The user is advised to connect FUSEVDD to GND except when fuses are programmed, to prevent unintentional blowing of fuses.
- Other power-up sequences may be possible; however, the above sequence has been verified and is recommended.
- There is a 1 ms minimum time between supplies coming up, and a 1 ms minimum time between POR_B assert and de-assert.
- The dV/dT should be no faster than 0.25 V/µs for all power supplies, to avoid triggering ESD circuit.

Figure 2 shows the power-up sequence diagram. After POR_B is asserted, Core VDD and NVDDx can be powered up. After Core VDD and NVDDx are stable, the analog supplies can be powered up.

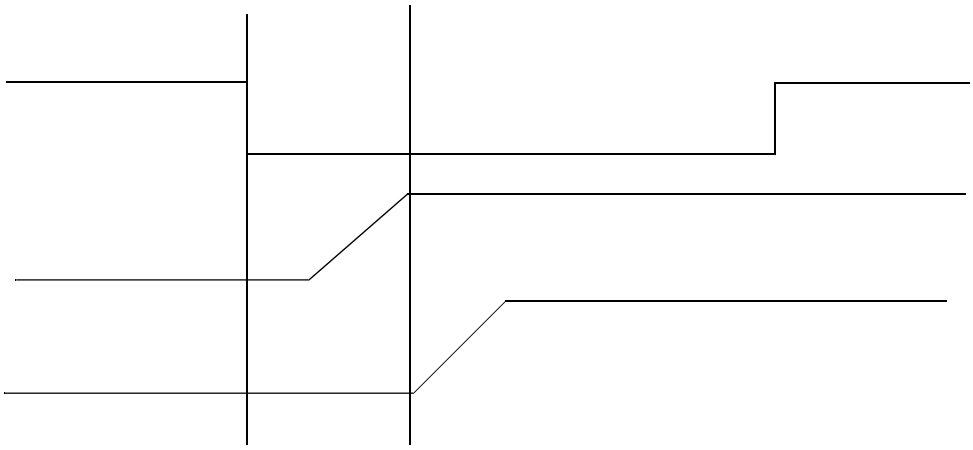

Figure 2. Power-Up Sequence Diagram

3.2.2 Power-Down Sequence

There are no special requirements for the power-down sequence. All power supplies can be shut down at the same time.

3.2.3 SRTC DryIce Power-Up/Down Sequence

In order to guarantee DryIce power-loss protection, including retention of SRTC time data during power down, users must do the following:

- Place a proper capacitor on the NVCC_DRYICE output pin, and
- Implement the below power-up/down sequence

1. Assert power on reset (POR).
2. Turn on NVCC_CRM.
3. Turn on QVDD digital logic domain supplies for not less than 1 ms and not more than 32 ms, after NVCC_CRM reaches 90% of 3.3 V.

current measurements are taken with customer-specific use-cases to reflect the normal operating conditions in the end system.

Table 15. Power Consumption

Power Supply	Voltage (V)	Max Current (mA)
QVDD	1.52	360
NVCC_EMI1, NVCC_EMI2	1.9	30
NVCC_CRM, NVCC_SDIO, NVCC_CSI, NVCC_NFC, NVCC_JTAG, NVCC_LCDC, NVCC_MISC	3.6	110
MPLL_VDD, UPLL_VDD	1.65	20
USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD, USBPHY1_VDDA, USBPHY2_VDD, OSC24M_VDD, NVCC_ADC	3.3	40
FUSE_VDD[1]	3.6	62
BATT_VDD	1.55	0.030

[1] The FUSE_VDD rail is connected to ground. it only needs a voltage if the system fuse burning is needed.

The method for obtaining the maximum current is as follows:

1. Measure the worst case power consumption on individual rails using directed test on i.MX25.
2. Correlate the worst case power consumption power measurements with the worst case power consumption simulations.
3. Combine common voltage rails based on the power supply sequencing requirements (add the worst case power consumption on each rail within some test cases from several test cases run, to maximize different rails in the power group).
4. Guard the worst case numbers for temperature and process variation.
5. The sum of individual rails is greater than the real world power consumption, since a real system does not typically maximize the power consumption on all peripherals simultaneously.
6. BATT_VDD current is measured when the system is in reduced power mode maintaining the RTC. When the system is in run mode, QVDD is used to supply the DryIce, so this current becomes negligible. See Table 12, for more details on the power modes.

NOTE

The values mentioned above should not be taken as a typical max run data for specific use cases. These values are Absolute MAX data. Freescale recommends that the system current measurements are taken with customer-specific use-cases to reflect normal operating conditions in the end system.

3.4 Thermal Characteristics

The thermal resistance characteristics for the device are given in Table 16. These values are measured under the following conditions:

- Two-layer substrate
- Substrate solder mask thickness: 0.025 mm
- Substrate metal thicknesses: 0.016 mm
- Substrate core thickness: 0.200 mm
- Core through I.D: 0.118 mm, Core through plating 0.016 mm.
- Flag: Trace style with ground balls under the die connected to the flag
- Die Attach: 0.033 mm non-conductive die attach, k = 0.3 W/m K
- Mold compound: Generic mold compound; k = 0.9 W/m K

Table 16. Thermal Resistance Data

Rating	Condition	Symbol	Value	Unit
Junction to ambient[1] natural convection	Single layer board (1s)	$R_{\theta JA}$	55	°C/W
Junction to ambient[1] natural convection	Four layer board (2s2p)	$R_{\theta JA}$	33	°C/W
Junction to ambient[1] (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	46	°C/W
Junction to ambient[1] (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	29	°C/W
Junction to boards[2]	—	$R_{\theta JB}$	22	°C/W
Junction to case (top)[3]	—	$R_{\theta JCtop}$	13	°C/W
Junction to package top[4]	Natural convection	Ψ_{JT}	2	°C/W

1 Junction-to-ambient thermal resistance determined per JEDC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-board thermal resistance determined per JEDC JESD51-8. Thermal test board meets JEDEC specification for this package.

3 Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, this thermal characterization parameter is written as Psi-JT.

3.5 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- DDR I/O: Mobile DDR (mDDR), double data rate (DDR2), or synchronous dynamic random access memory (SDRAM)
- General purpose I/O (GPIO)

Figure 3 shows the load circuit for output. Figure 4 through Figure 6 show the output transition time and propagation waveforms.

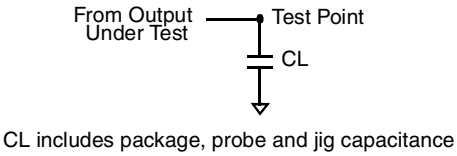

Figure 3. Load Circuit for Output

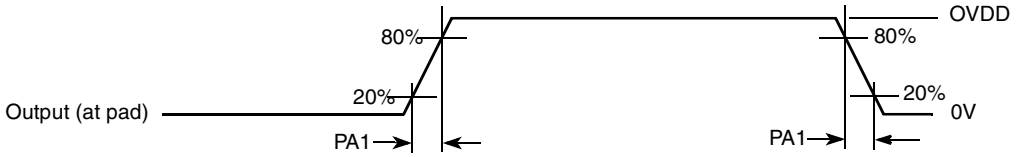

Figure 4. Output Pad Transition Time Waveform

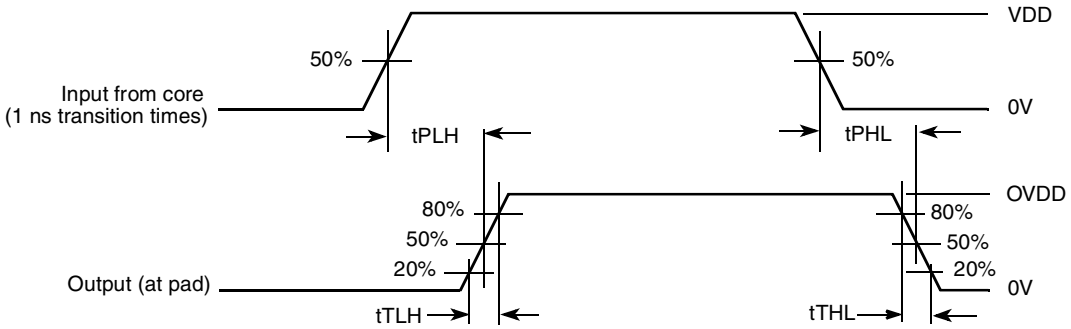

Figure 5. Output Pad Propagation and Transition Time Waveform

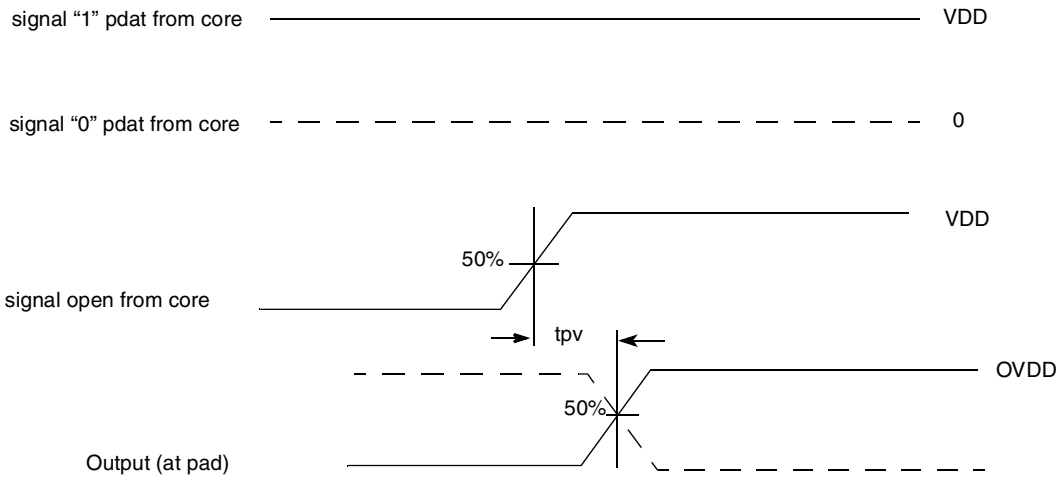

Figure 6. Output Enable to Output Valid

Table 25 shows the AC parameters for mobile DDR pbijtov18_33_ddr_clk I/O.

Table 25. AC Parameters for Mobile DDR pbijtov18_33_ddr_clk I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	50	60	%
Clock frequency[1]	f	—	—	—	133	MHz
Output pad transition times[1] (max. drive)	tpr	25 pF 50 pF	0.52/0.51 0.98/0.96	0.79/0.72 1.49/1.34	1.25/1.09 2.31/1.98	ns
Output pad transition times[1] (high drive)	tpr	25 pF 50 pF	1.13/1.10 2.15/2.10	1.74/1.55 3.28/2.92	2.71/2.30 5.11/4.31	ns
Output pad transition times[1] (standard drive)	tpr	25 pF 50 pF	2.26/2.19 4.30/4.18	3.46/3.07 6.59/5.79	5.39/4.56 10.13/8.55	ns
Output pad propagation delay[1] (max. drive), 50%–50% input signals and crossing of output signals	tpo	15 pF 35 pF	1.28/1.19 1.56/1.47	1.97/1.83 2.37/2.23	2.98/2.78 3.57/3.37	ns
Output pad propagation delay[1] (high drive), 50%–50% input signals and crossing of output signals	tpo	15 pF 35 pF	1.54/1.43 2.14/2.04	2.34/2.20 3.22/3.08	3.54/3.33 4.85/4.65	ns
Output pad propagation delay[1] (standard drive), 50%–50% input signals and crossing of output signals	tpo	15 pF 35 pF	2.05/1.94 3.27/3.16	3.11/2.96 4.86/4.72	4.70/4.50 7.33/7.12	ns
Output pad propagation delay[1] (max. drive), 40%–60% input signals and crossing of output signals	tpo	15 pF 35 pF	1.45/1.36 1.73/1.64	2.13/2.00 2.53/2.40	3.14/2.94 3.74/3.54	ns
Output pad propagation delay[1] (high drive), 40%–60% input signals and crossing of output signals	tpo	15 pF 35 pF	1.70/1.60 2.31/2.21	2.51/2.37 3.38/3.24	3.70/3.50 5.02/4.82	ns
Output pad propagation delay[1] (standard drive), 40%–60% input signals and crossing of output signals	tpo	15 pF 35 pF	2.22/2.11 3.43/3.32	3.27/3.13 5.02/4.88	4.87/4.66 7.49/7.29	ns
Output enable to output valid delay[1] (max. drive), 50%–50%	tpv	15 pF 35 pF	1.16/1.12 1.42/1.41	1.91/1.81 2.31/2.20	3.10/2.89 3.72/3.47	ns
Output enable to output valid delay[1] (high drive), 50%–50%	tpv	15 pF 35 pF	1.39/1.39 1.98/2.02	2.28/2.18 3.18/3.04	3.69/3.43 5.08/4.69	ns
Output enable to output valid delay[1] (standard drive), 50%–50%	tpv	15 pF 35 pF	1.90/1.94 3.07/3.20	3.09/2.94 4.88/4.66	4.95/4.55 7.73/7.05	ns
Output enable to output valid delay[1] (max. drive), 40%–60%	tpv	15 pF 35 pF	1.28/1.24 1.49/1.47	2.00/1.90 2.32/2.21	3.14/2.93 3.64/3.41	ns
Output enable to output valid delay[1] (high drive), 40%–60%	tpv	15 pF 35 pF	1.45/1.44 1.92/1.95	2.28/2.19 2.99/2.87	3.60/3.36 4.69/4.36	ns
Output enable to output valid delay[1] (standard drive), 40%–60%	tpv	15 pF 35 pF	1.85/1.88 2.78/2.88	2.92/2.79 4.34/4.16	4.5894.25 6.79/6.24	ns
Output pad slew rate[2] (max. drive)	tps	25 pF 50 pF	0.37/0.45 0.30/0.36	0.64/0.79 0.52/0.61	1.14/1.36 0.90/1.02	V/ns

3.7.2.2 Multiword DMA (MDMA) Mode Timing

Figure 13 and Figure 14 show the timing for MDMA read and write modes, respectively.

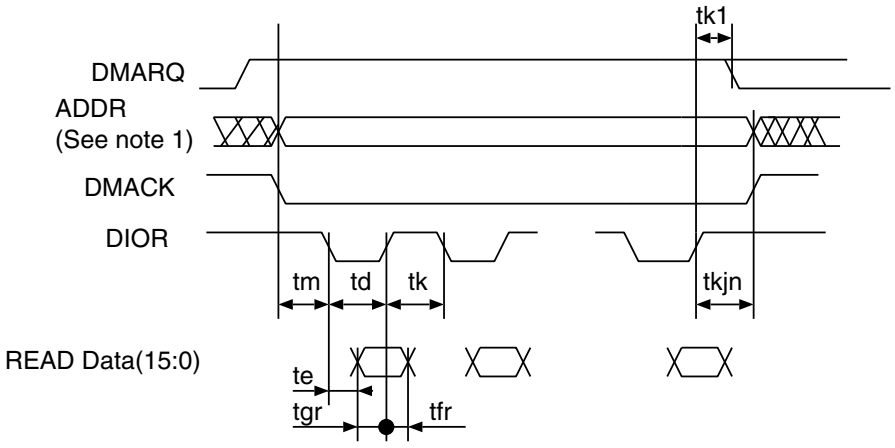

Figure 13. MDMA Read Mode Timing

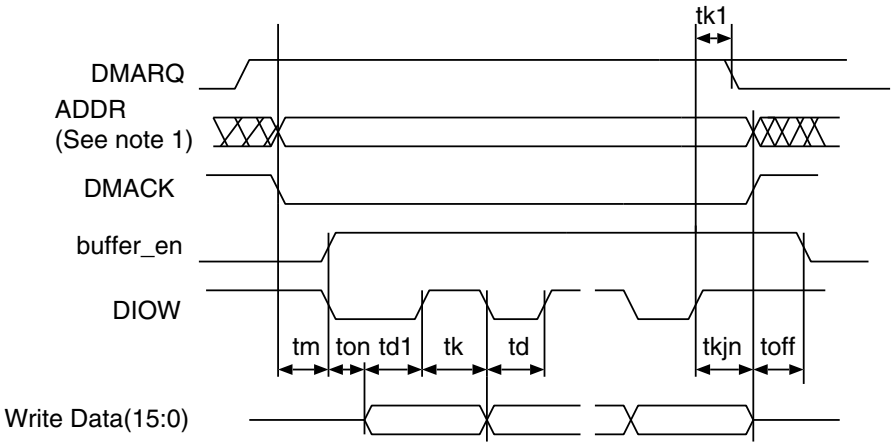

Figure 14. MDMA Write Mode Timing

Table 43. CSPI Interface Timing Parameters

ID	Parameter Description	Symbol	Minimum	Maximum	Units
t1	CSPI master SCLK cycle time	t_{clko}	60.2	—	ns
t2	CSPI master SCLK high time	t_{clkoH}	22.65	—	ns
t3	CSPI master SCLK low time	t_{clkoL}	22.47	—	ns
t1’	CSPI slave SCLK cycle time	t_{clki}	60.2	—	ns
t2’	CSPI slave SCLK high time	t_{clkiH}	30.1	—	ns
t3’	CSPI slave SCLK low time	t_{clkiL}	30.1	—	ns
t4	CSPI SCLK transition time	t_{pr}[1]	2.6	8.5	ns
t5	SS*n* output pulse width	t_{Wsso}	$2T_{sclk}$[2] $+T_{wait}$[3]	—	—
t5’	SS*n* input pulse width	t_{Wssi}	T_{per}[4]	—	—
t6	SS*n* output asserted to first SCLK edge (SS output setup time)	t_{Ssso}	$3T_{sclk}$	—	—
t6’	SS*n* input asserted to first SCLK edge (SS input setup time)	t_{Sssi}	T_{per}	—	—
t7	CSPI master: Last SCLK edge to SS*n* negated (SS output hold time)	t_{Hsso}	$2T_{sclk}$	—	—
t7’	CSPI slave: Last SCLK edge to SS*n* negated (SS input hold time)	t_{Hssi}	30	—	ns
t8	CSPI master: CSPI1_RDY low to SS*n* asserted (CSPI1_RDY setup time)	t_{Srdy}	$2T_{per}$	$5T_{per}$	—
t9	CSPI master: SS*n* negated to CSPI1_RDY low	t_{Hrdy}	0	—	ns
t10	Output data setup time	t_{Sdatao}	(t_{clkoL} or t_{clkoH} or t_{clkiL} or t_{clkiH}) – T_{ipg}[5]	—	—
t11	Output data hold time	t_{Hdatao}	t_{clkoL} or t_{clkoH} or t_{clkiL} or t_{clkiH}	—	—
t12	Input data setup time	t_{Sdatai}	T_{ipg} + 0.5	—	ns
t13	Input data hold time	t_{Hdatai}	0	—	ns
t14	Pause between data word	t_{pause}	0	—	ns

1 The output SCLK transition time is tested with 25 pF drive.

2 T_{sclk} = CSPI clock period

3 T_{wait} = Wait time, as specified in the sample period control register

4 T_{per} = CSPI reference baud rate clock period (PERCLK2)

5 T_{ipg} = CSPI main clock IPG_CLOCK period

3.7.6 External Memory Interface (EMI) Timing

The EMI module includes the enhanced SDRAM/LPDDR memory controller (ESDCTL), NAND Flash controller (NFC), and wireless external interface module (WEIM). The following subsections give timing information for these submodules.

Table 47. SDRAM Self-Refresh Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD16	CKE output delay time	tCKS	1.8	—	ns

3.7.6.1.2 Mobile DDR SDRAM–Specific Parameters

The following diagrams and tables specify the timings related to the SDRAMC module which interfaces with the mobile DDR SDRAM.

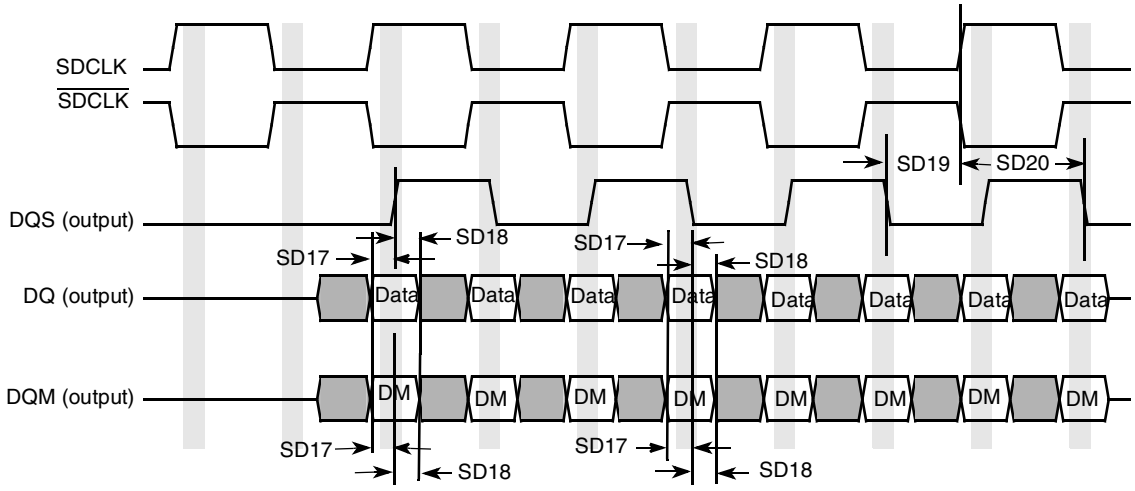

Figure 29. Mobile DDR SDRAM Write Cycle Timing Diagram

Table 48. Mobile DDR SDRAM Write Cycle Timing Parameters[1]

ID	Parameter	Symbol	Min.	Max.	Unit
SD17	DQ and DQM setup time to DQS	tDS	0.95	—	ns
SD18	DQ and DQM hold time to DQS	tDH	0.95	—	ns
SD19	Write cycle DQS falling edge to SDCLK output delay time	tDSS	1.8	—	ns
SD20	Write cycle DQS falling edge to SDCLK output hold time	tDSH	1.8	—	ns

[1] Test condition: Measured using delay line 5 programmed as follows: ESDCDLY5[15:0] = 0x0703.

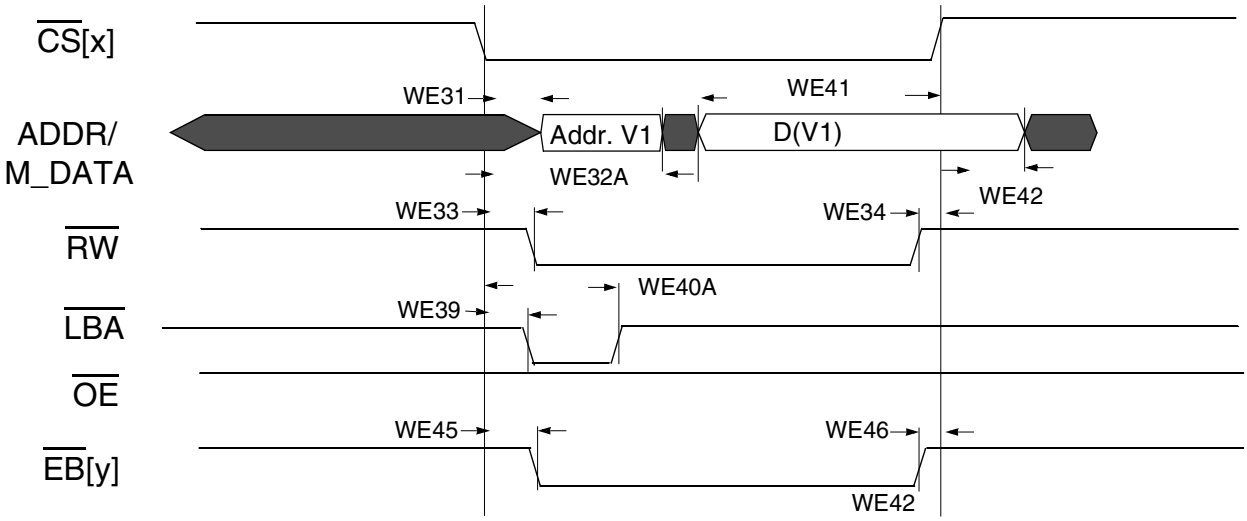

Figure 48. Asynchronous A/D Mux Write Access

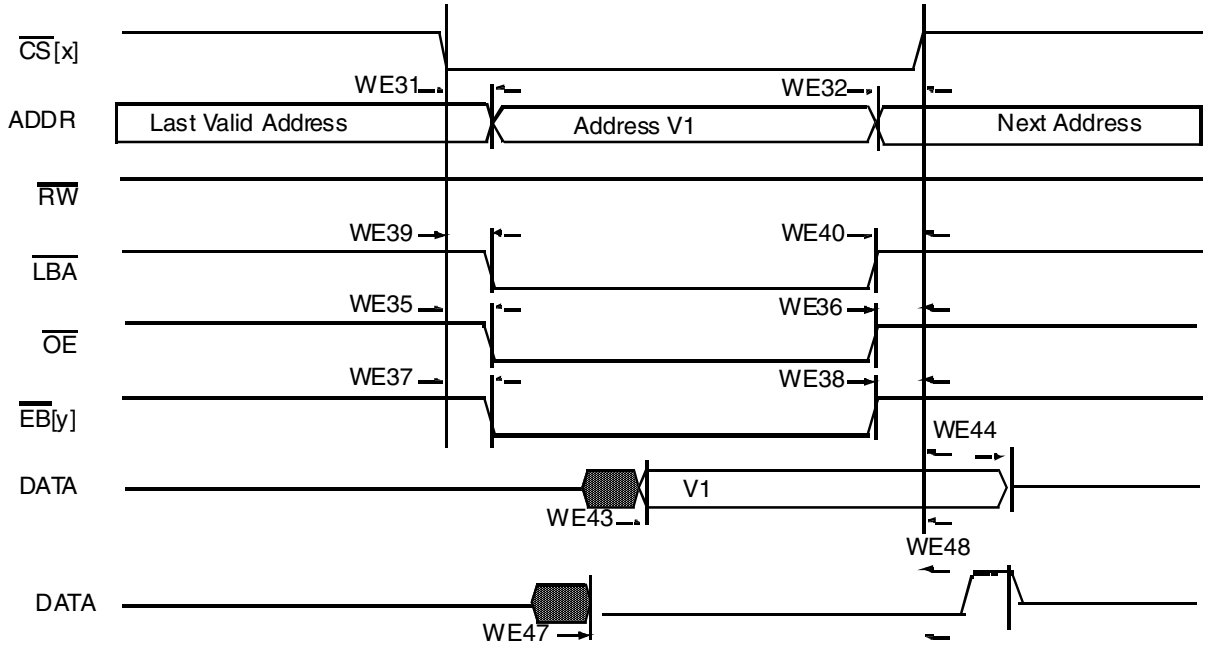

Figure 49. DTACK Read Access

Table 57. WEIM Asynchronous Timing Parameters Relative to Chip Select Table

Ref No.	Parameter	Determination By Synchronous Measured Parameters[1]	Min	Max (If 133 MHz is supported by SoC)	Unit
WE31	$\overline{CS}$[x] valid to Address Valid	WE4 – WE6 – CSA[2]	—	3 – CSA	ns
WE32	Address Invalid to $\overline{CS}$[x] invalid	WE7 – WE5 – CSN[3]	—	3 – CSN	ns

Table 57. WEIM Asynchronous Timing Parameters Relative to Chip Select Table (continued)

Ref No.	Parameter	Determination By Synchronous Measured Parameters[1]	Min	Max (If 133 MHz is supported by SoC)	Unit
WE32A(muxed A/D	$\overline{CS}$[x] valid to Address Invalid	WE4 – WE7 + (LBN + LBA + 1 – CSA[2])	–3 + (LBN + LBA + 1 – CSA)	—	ns
WE33	$\overline{CS}$[x] Valid to $\overline{RW}$ Valid	WE8 – WE6 + (RWA – CSA)	—	3 + (RWA – CSA)	ns
WE34	$\overline{RW}$ Invalid to $\overline{CS}$[x] Invalid	WE7 – WE9 + (RWN – CSN)	—	3 – (RWN_CSN)	ns
WE35	$\overline{CS}$[x] Valid to $\overline{OE}$ Valid	WE10 – WE6 + (OEA – CSA)	—	3 + (OEA – CSA)	ns
WE35A (muxed A/D)	$\overline{CS}$[x] Valid to $\overline{OE}$ Valid	WE10 – WE6 + (OEA + LBN + LBA + LAH + 1 – CSA)	–3 + (OEA + LBN + LBA + LAH + 1 – CSA)	3 + (OEA + LBN + LBA + LAH + 1 – CSA)	ns
WE36	$\overline{OE}$ Invalid to $\overline{CS}$[x] Invalid	WE7 – WE11 + (OEN – CSN)	—	3 – (OEN – CSN)	ns
WE37	$\overline{CS}$[x] Valid to $\overline{EB}$[y] Valid (Read access)	WE12 – WE6 + (EBRA – CSA)	—	3 + (EBRA[4] – CSA)	ns
WE38	$\overline{EB}$[y] Invalid to $\overline{CS}$[x] Invalid (Read access)	WE7 – WE13 + (EBRN – CSN)	—	3 – (EBRN[5] – CSN)	ns
WE39	$\overline{CS}$[x] Valid to $\overline{LBA}$ Valid	WE14 – WE6 + (LBA – CSA)	—	3 + (LBA – CSA)	ns
WE40	$\overline{LBA}$ Invalid to $\overline{CS}$[x] Invalid	WE7 – WE15 – CSN	—	3 – CSN	ns
WE40A (muxed A/D)	$\overline{CS}$[x] Valid to $\overline{LBA}$ Invalid	WE14 – WE6 + (LBN + LBA + 1 – CSA)	–3 + (LBN + LBA + 1 – CSA)	3 + (LBN + LBA + 1 – CSA)	ns
WE41	$\overline{CS}$[x] Valid to Output Data Valid	WE16 – WE6 – CSA	—	3 – CSA	ns
WE41A (muxed A/D)	$\overline{CS}$[x] Valid to Output Data Valid	WE16 – WE6 + (LBN + LBA + LAH + 1 – CSA)	—	3 + (LBN + LBA + LAH + 1 – CSA)	ns
WE42	Output Data Invalid to $\overline{CS}$[x] Invalid	WE17 – WE7 – CSN	—	3 – CSN	ns
WE43	Input Data Valid to $\overline{CS}$[x] Invalid	MAXCO – MAXCSO + MAXDI	MAXCO[6] – MAXCSO[7] + MAXDI[8]	—	ns
WE44	$\overline{CS}$[x] Invalid to Input Data invalid	0	0	—	ns
WE45	$\overline{CS}$[x] Valid to $\overline{EB}$[y] Valid (Write access)	WE12 – WE6 + (EBWA – CSA)	—	3 + (EBWA – CSA)	ns
WE46	$\overline{EB}$[y] Invalid to $\overline{CS}$[x] Invalid (Write access)	WE7 – WE13 + (EBWN – CSN)	—	–3 + (EBWN – CSN)	ns
WE47	$\overline{DTACK}$ Valid to $\overline{CS}$[x] Invalid	MAXCO – MAXCSO + MAXDTI	MAXCO[6] – MAXCSO[7] + MAXDTI[9]	—	ns
WE48	$\overline{CS}$[x] Invalid to $\overline{DTACK}$ invalid	0	0	—	ns

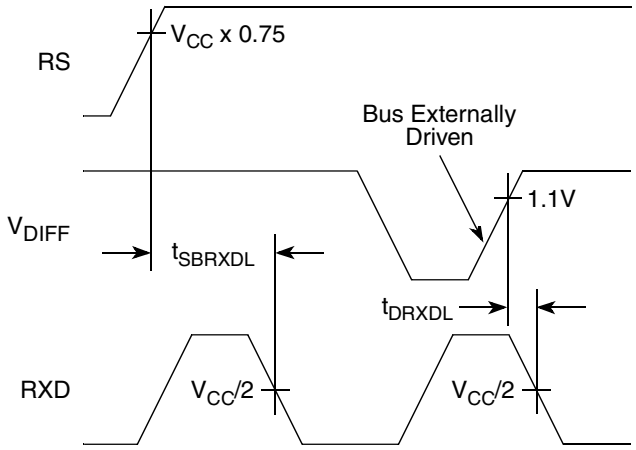

Figure 61. Timing Diagram for FlexCAN Standby Signal

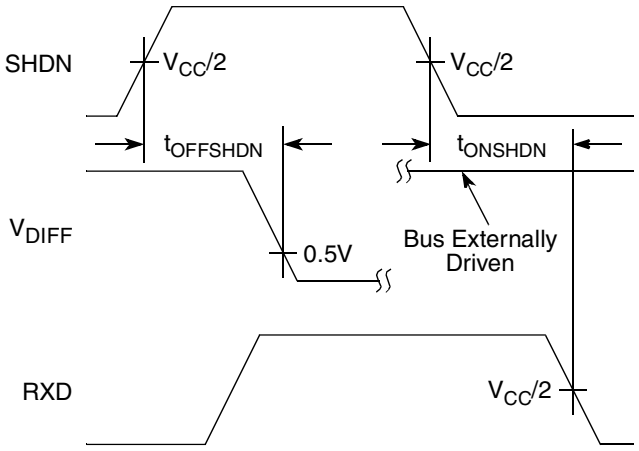

Figure 62. Timing Diagram for FlexCAN Shutdown Signal

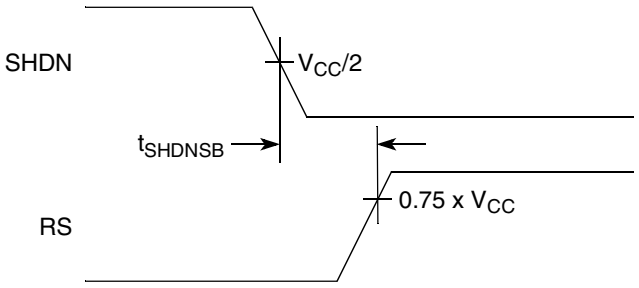

Figure 63. Timing Diagram for FlexCAN Shutdown-to-Standby Signal

Because integer multiples are not possible, taking into account the range of frequencies at which the SoC has to operate, DPLLs work in FOL mode only.

3.7.11 Inter IC Communication (I^2C) Timing

The I^2C communication protocol consists of the following seven elements:

- Start
- Data source/recipient
- Data direction
- Slave acknowledge
- Data
- Data acknowledge
- Stop

Figure 64 shows the timing of the I^2C module. Table 69 and Table 70 describe the I^2C module timing parameters (IC1–IC6) shown in the figure.

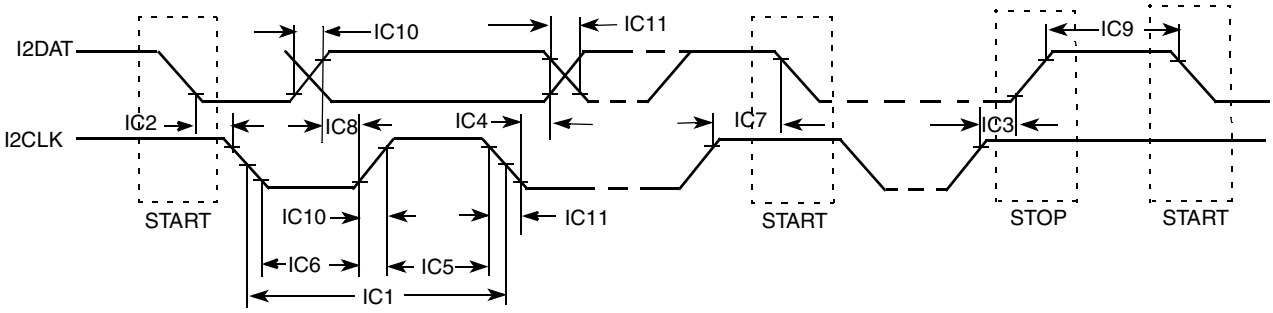

Figure 64. I^2C Module Timing Diagram

Table 69. I2C Module Timing Parameters: 3.0 V +/–0.30 V

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
IC1	I2CLK cycle time	10	-	2.5		µs
IC2	Hold time (repeated) START condition	4.0	-	0.6	-	µs
IC3	Set-up time for STOP condition	4.0	-	0.6	-	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	-	0.6	-	µs
IC6	LOW Period of the I2CLK Clock	4.7	-	1.3	-	µs
IC7	Set-up time for a repeated START condition	4.7	-	0.6	-	µs
IC8	Data set-up time	250	-	100[3]	-	ns
IC9	Bus free time between a STOP and START condition	4.7	-	1.3	-	µs
IC10	Rise time of both I2DAT and I2CLK signals	-	1000	$20+0.1C_b$[4]	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	-	300	$20+0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	-	400	-	400	pF

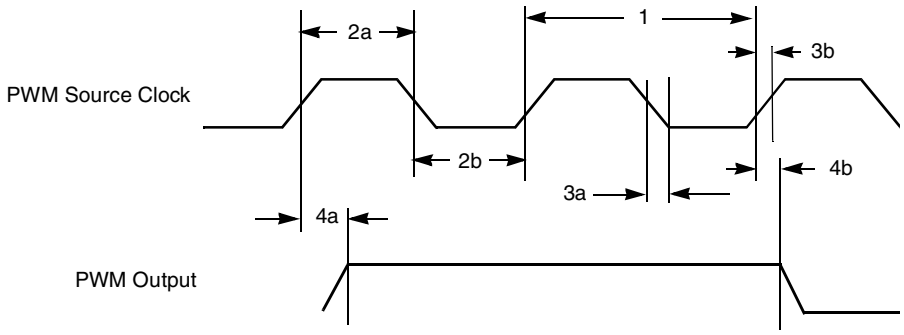

Figure 67. PWM Timing

Table 73. PWM Output Timing Parameter

Ref No.	Parameter	Minimum	Maximum	Unit
1	System CLK frequency[1]	0	ipg_clk	MHz
2a	Clock high time	12.29	—	ns
2b	Clock low time	9.91	—	ns
3a	Clock fall time	—	0.5	ns
3b	Clock rise time	—	0.5	ns
4a	Output delay time	—	9.37	ns
4b	Output setup time	8.71	—	ns

[1] CL of PWMO = 30 pF

3.7.14 Subscriber Identity Module (SIM) Timing

Each SIM module interface consists of a total of 12 pins (two separate ports, each containing six signals). Typically a port uses five signals.

The interface is designed to be used with synchronous SIM cards, meaning the SIM module provides the clock used by the SIM card. The clock frequency is typically 372 times the Tx/Rx data rate; however, the SIM module can also work with CLK frequencies of 16 times the Tx/Rx data rate.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the SIM card is used by the SIM card to recover the clock from the data in the same manner as standard UART data exchanges. All six signals (five for bidirectional Tx/Rx) of the SIM module are asynchronous with each other.

There are no required timing relationships between signals in normal mode. The SIM card is initiated by the interface device; the SIM card responds with Answer to Reset. Although the SIM interface has no defined requirements, the ISO/IEC 7816 defines reset and power-down sequences (for detailed information see ISO/IEC 7816).

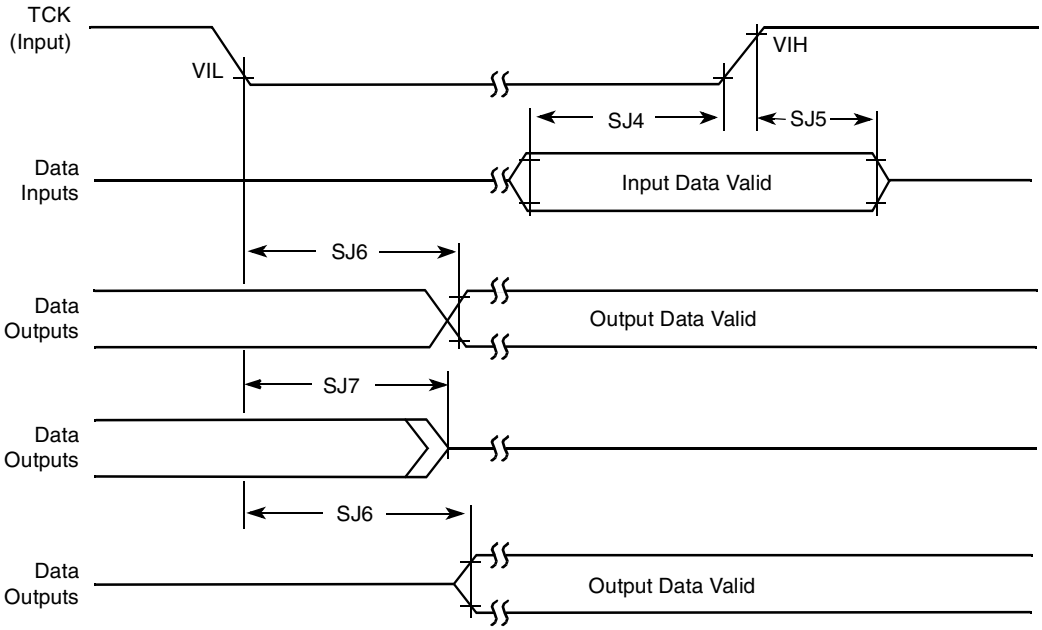

Figure 73. Boundary Scan (JTAG) Timing Diagram

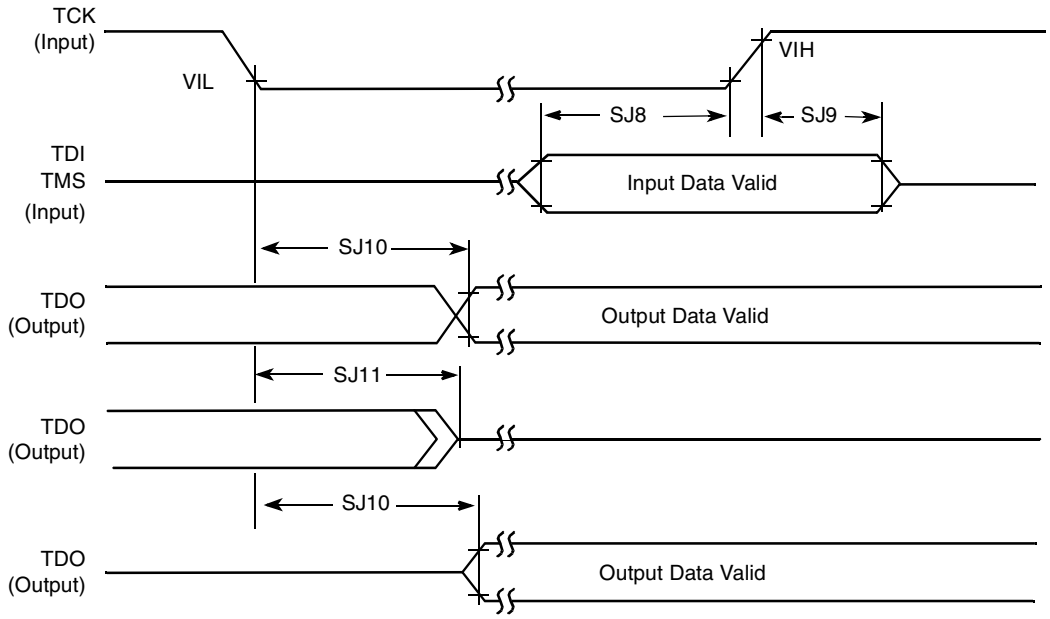

Figure 74. Test Access Port Timing Diagram

3.7.19.2 UART Infrared (IrDA) Mode Timing

The following subsections describe the UART transmit and receive timing in IrDA mode.

3.7.19.2.3 UART IrDA Mode Transmit Timing

Figure 87 depicts the UART transmit timing in IrDA mode, showing only 8 data bits and 1 stop bit. Table 88 describes the timing parameters (UA3–UA4) shown in the figure.

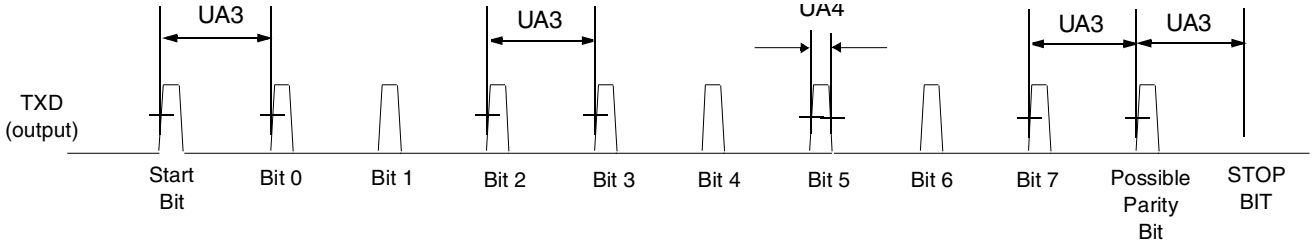

Figure 87. UART IrDA Mode Transmit Timing Diagram

Table 88. UART IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA3	Transmit bit time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR pulse duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16) \times (1/F_{baud\_rate}) + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

3.7.19.2.4 UART IrDA Mode Receive Timing

Figure 88 shows the UART receive timing for IrDA mode, for a format of 8 data bits and 1 stop bit. Table 89 describes the timing parameters (UA5–UA6) shown in the figure.

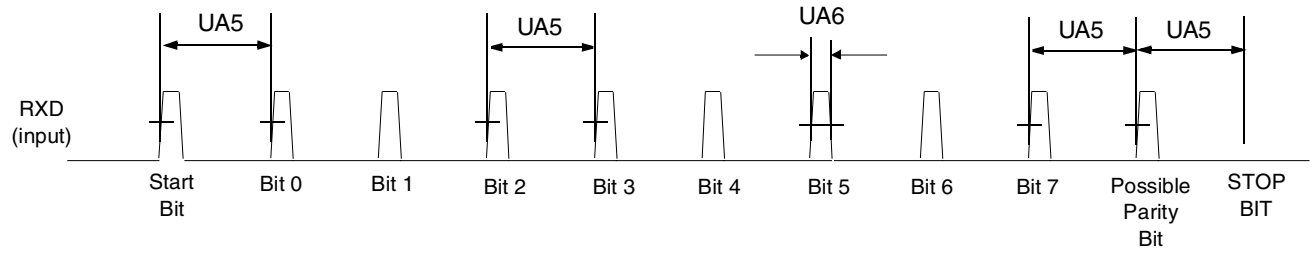

Figure 88. UART IrDA Mode Receive Timing Diagram

Table 89. UART IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA5	Receive bit time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR pulse duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

Table 97 shows the timing specifications for USB in VP_VM unidirectional mode.

Table 97. USB Timing Specifications in VP_VM Unidirectional Mode

No.	Parameter	Signal	Direction	Min.	Max.	Unit	Conditions/ Reference Signal
US30	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US31	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US32	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US33	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US34	Tx high overlap	USB_SE0_VM	Out	0.0	—	ns	USB_DAT_VP
US35	Tx low overlap	USB_SE0_VM	Out	—	0.0	ns	USB_DAT_VP
US36	Enable delay	USB_DAT_VP USB_SE0_VM	In	—	8.0	ns	USB_TXOE_B
US37	Disable delay	USB_DAT_VP USB_SE0_VM	In	—	10.0	ns	USB_TXOE_B
US38	Rx rise/fall time	USB_VP1	In	—	3.0	ns	35 pF
US39	Rx rise/fall time	USB_VM1	In	—	3.0	ns	35 pF
US40	Rx skew	USB_VP1	Out	–4.0	+4.0	ns	USB_SE0_VM
US41	Rx skew	USB_RCV	Out	–6.0	+2.0	ns	USB_DAT_VP

3.7.20.2 USB Parallel Interface Timing

Table 98 defines the USB parallel interface signals.

Table 98. Signal Definitions for USB Parallel Interface

Name	Direction	Signal Description
USB_Clk	In	Interface clock—All interface signals are synchronous to USB_Clk
USB_Data[7:0]	I/O	Bidirectional data bus, driven low by the link during idle—Bus ownership is determined by the direction
USB_Dir	In	Direction—Control the direction of the data bus
USB_Stp	Out	Stop—The link asserts this signal for one clock cycle to stop the data stream currently on the bus
USB_Nxt	In	Next—The PHY asserts this signal to throttle the data

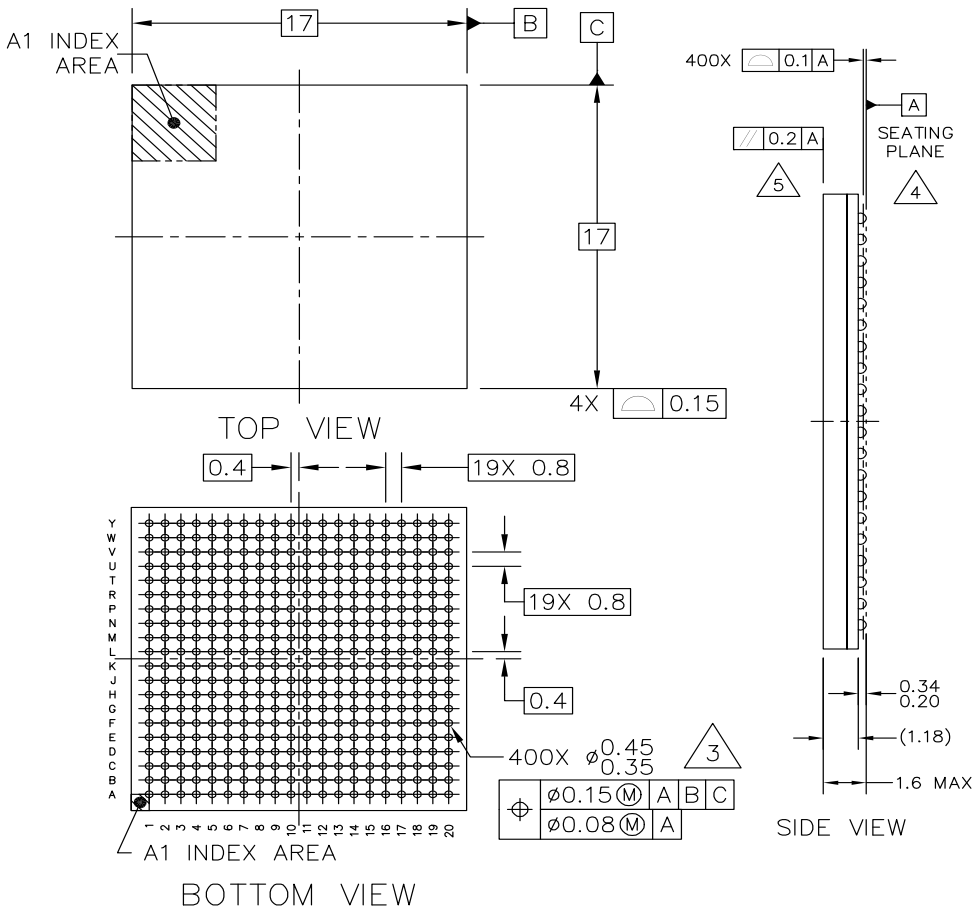

Figure 98. 17×17 i.MX25 Production Package

4.2 Ground, Power, Sense, and Reference Contact Assignments Case 17x17 mm, 0.8 mm Pitch

Table 100 shows the 17×17 mm package ground, power, sense, and reference contact assignments.

Table 100. 17×17 mm Package Ground, Power Sense, and Reference Contact Assignments

Contact Name	Contact Assignment
BATT_VDD	P10
FUSE_VDD	T17
MPLL_GND	U17
MPLL_VDD	U18
NGND_ADC	Y13
NVCC_ADC	W13
NVCC_CRM	N14
NVCC_CSI	J13, J14

Table 105. 12x12 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
GPIO_E	R21	CRM	GPIO	INPUT	100 KΩ Pull-Up
GPIO_F	R19	CRM	GPIO	INPUT	-
EXT_ARMCLK	V22	CRM	GPIO	INPUT	-
UPLL_BYPCLK	U21	CRM	GPIO	INPUT	-
VSTBY_REQ	T21	CRM	GPIO	OUTPUT	Low
VSTBY_ACK[3]	W22	CRM	GPIO	OUTPUT	Low
POWER_FAIL	T19	CRM	GPIO	INPUT	100 KΩ Pull-Down
RESET_B	U19	CRM	GPIO	INPUT	100 KΩ Pull-Up
POR_B	V21	CRM	GPIO	INPUT	100 KΩ Pull-Up
CLKO	Y22	CRM	GPIO	OUTPUT	Low
BOOT_MODE0[2]	AA22	CRM	GPIO	INPUT	100 KΩ Pull-Down
BOOT_MODE1[2]	W21	CRM	GPIO	INPUT	100 KΩ Pull-Down
CLK_SEL	AA20	CRM	GPIO	INPUT	100 KΩ Pull-Down
TEST_MODE	AA19	CRM	GPIO	INPUT	100 KΩ Pull-Down
OSC24M_EXTAL	AB19	OSC24M	ANALOG	ANALOG	-
OSC24M_XTAL	AB20	OSC24M	ANALOG	ANALOG	-
OSC32K_EXTAL	AB13	DRYICE	ANALOG	ANALOG	-
OSC32K_XTAL	AB12	DRYICE	ANALOG	ANALOG	-
TAMPER_A	V11	DRYICE	ANALOG	ANALOG	-
TAMPER_B	V13	DRYICE	ANALOG	ANALOG	-
MESH_C	T13	DRYICE	ANALOG	ANALOG	-
MESH_D	R13	DRYICE	ANALOG	ANALOG	-
OSC_BYP	AB15	DRYICE	ANALOG	ANALOG	-
XP	AA18	ADC	ANALOG	ANALOG	-
XN	AA16	ADC	ANALOG	ANALOG	-
YP	AB17	ADC	ANALOG	ANALOG	-
YN	W15	ADC	ANALOG	ANALOG	-

5 Revision History

Table 108 summarizes revisions to this document.

Table 108. Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 10	05/2013	• Updated DDR timing parameters in – Table 47, “SDRAM Self-Refresh Cycle Timing Parameters” – Table 49, “Mobile DDR SDRAM Read Cycle Timing Parameters” – Table 51, “tIS, tIH Derating Values for DDR2-400, DDR2-533” • Table 101, “17×17 mm Package i.MX25 Signal Contact Assignment”: Updated configuration after reset for contact D11 to “100 KΩ Pull-Up”
Rev. 9	06/2012	• In Table 1, "Ordering Information," on page 3, removed exclamation marks from table rows and also removed table footnote. • In Table 3, "i.MX25 Digital and Analog Modules," on page 6, modified description of block mnemonic, SIM. • Updated Section 3.2.1, “Power-Up Sequence.” • Updated Section 3.2.3, “SRTC DryIce Power-Up/Down Sequence.” • In Figure 38 and Table 56: —Removed “_B” and added an overbar to signal names, CSx_B, RW_B, OE_B, EBy_B, LBA_B, ECB_B, and DTACK_B —Changed CSx and CSy to CS[x] and CS[y], respectively • In Table 57, "WEIM Asynchronous Timing Parameters Relative to Chip Select Table," on page 76: —Changed $\overline{WE}$ and WEA to $\overline{RW}$ and RWA, respectively, for reference number, WE33 —Changed $\overline{WE}$ and WEN to $\overline{RW}$ and RWN, respectively, for reference number, WE34 —Changed RLBA, RLBN, and ADH to LBA, LBN, and LAH, respectively, for reference number, WE35A —Changed RBEA to EBRA for reference number, WE37 —Changed RBEN to EBRN for reference number, WE38 —Changed WCSA to CSA for reference numbers, WE41 and WE41A —Changed WLBA, WLBN, and ADH to LBA, LBN, and LAH, respectively, for reference number, WE41A —Changed WBEA and WBEN to EBWA and EBWN, respectively, for reference numbers, WE45 and WE46 • Updated the note after Table 57. • In Table 99, "USB Timing Specification in Parallel Mode," on page 124, swapped the values of Min and Max columns for IDs, US15 and US16.
Rev. 8	01/2011	• In Table 27, "AC Parameters for SDRAM I/O," on page 36, the frequency specification has been updated to 133 MHz. • In Table 28, "AC Parameters for SDRAM pbijtov18_33_ddr_clk I/O," on page 37, the frequency specification has been updated to 133 MHz.