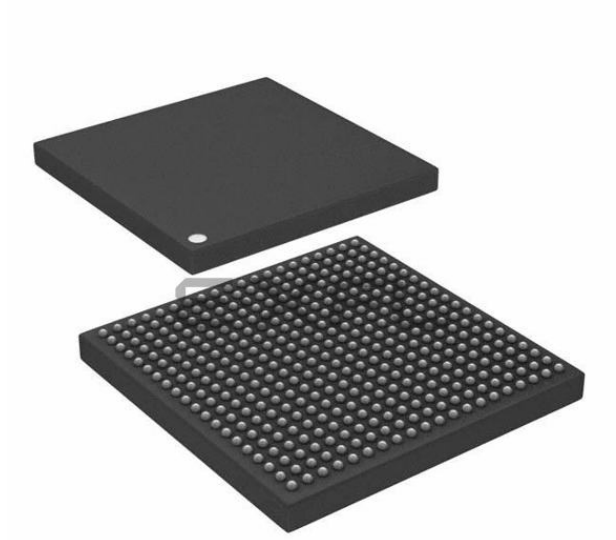

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-20°C ~ 70°C (TA)
Security Features	-
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx253djm4a

Figure 17 shows timing for device-terminated UDMA in-transfer.

Figure 17. Timing for Device-Terminated UDMA Transfer

Timing parameters for UDMA in-burst are listed in Table 39.

Table 39. Timing Parameters for UDMA In-Burst

ATA Parameter	Spec. Parameter	Value	Required Conditions
tack	tack	tack(min.) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv(min.) = (time_env × T) – (tskew1 + tskew2) tenv(max.) = (time_env × T) + (tskew1 + tskew2)	time_env
tds	tds1	tds – (tskew3) – ti_ds > 0	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	tdh – (tskew3) –ti_dh > 0	

3.7.4.1 Gated Clock Mode Timing

Figure 20 and Figure 21 shows the gated clock mode timings for CSI, and Table 41 describes the timing parameters (P1–P7) shown in the figures. A frame starts with a rising/falling edge on VSYNC, then HSYNC is asserted and holds for the entire line. The pixel clock is valid as long as HSYNC is asserted.

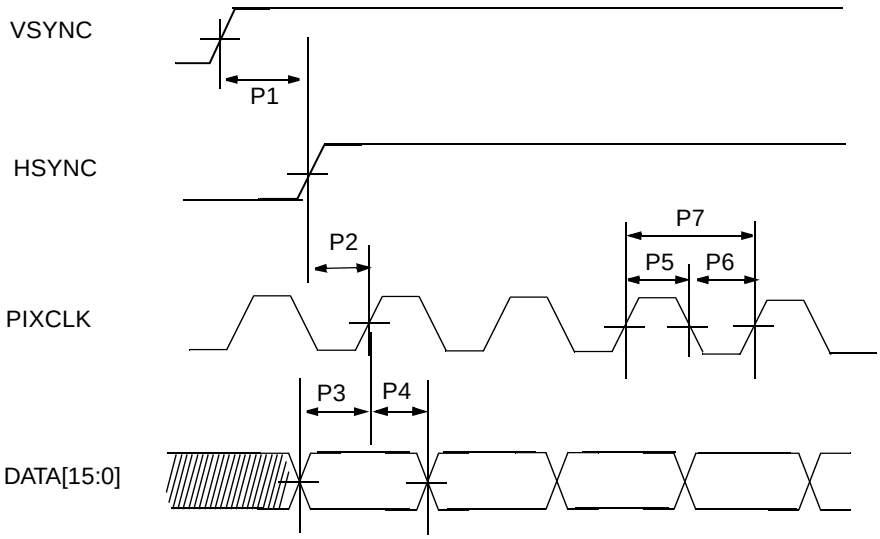

Figure 20. CSI Gated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

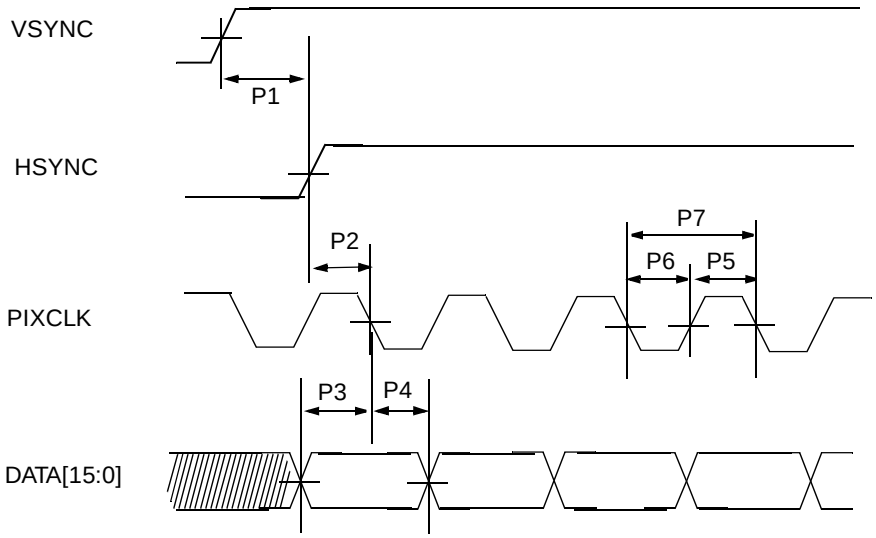

Figure 21. CSI Gated Clock Mode—Sensor Data at Rising Edge, Latch Data at Falling Edge

3.7.6.1 ESDCTL Electrical Specifications

3.7.6.1.1 SDRAM Memory Controller

The following diagrams and tables specify the timing related to the SDRAMC module which interfaces SDRAM.

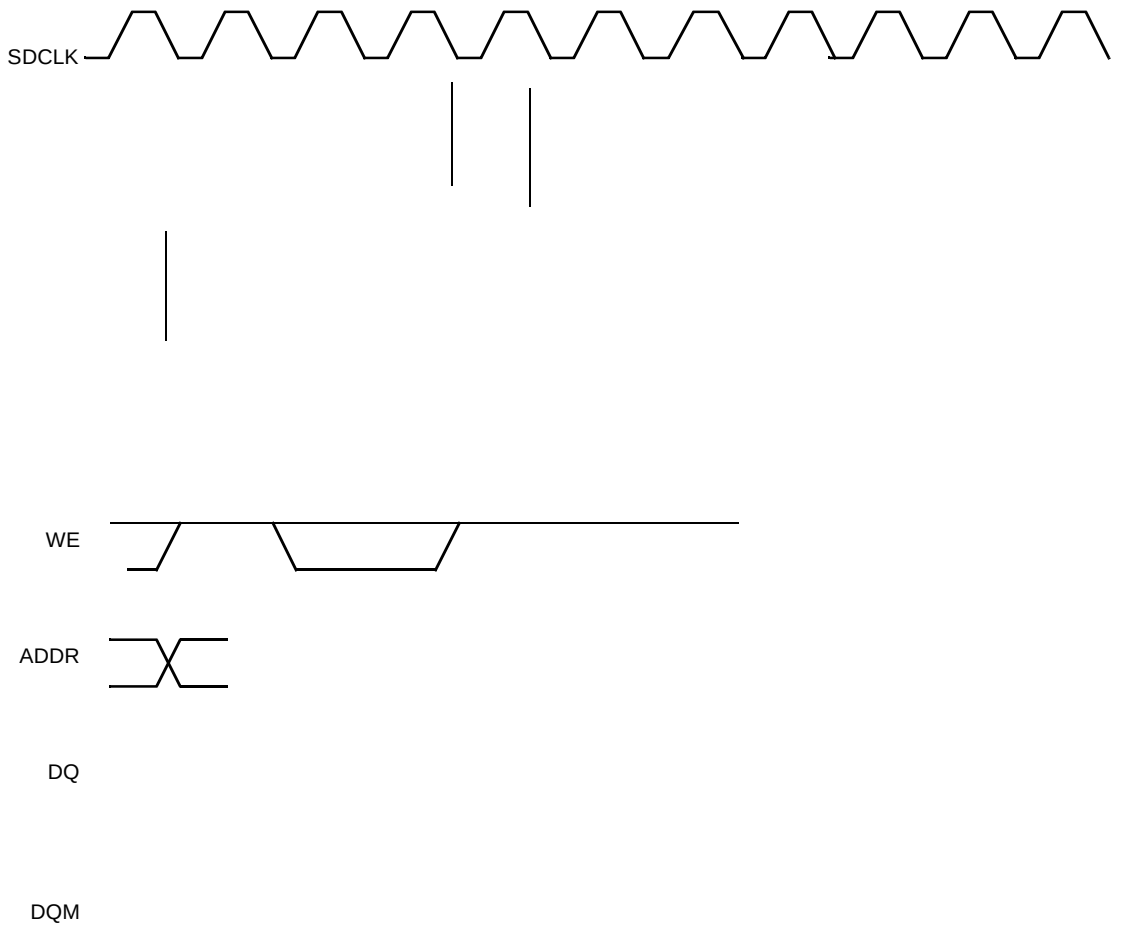

Figure 25. SDRAM Read Cycle Timing Diagram

Table 44. DDR/SDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width[1]	tCH	3.4	4.1	ns
SD2	SDRAM clock low-level width[1]	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD4	CS, RAS, CAS, WE, DQM, CKE setup time	tCMS	2.0	—	ns
SD5	CS, RAS, CAS, WE, DQM, CKE hold time	tCMH	1.8	—	ns

3.7.6.1.3 DDR2 SDRAM–Specific Parameters

The following diagrams and tables specify timing related to the SDRAMC module, which interfaces with DDR2 SDRAM.

Figure 31. DDR2 SDRAM Basic Timing Parameters

Table 50

Table 60. ESAI General Timing Requirements (continued)

No.	Characteristics [1 2]	Symbol	Expression [3]	Min.	Max.	Condition	Unit
65	SCKR rising edge to FSR out (bl) high	—	—	— —	17.0 7.0	x ck i ck a	ns
66	SCKR rising edge to FSR out (bl) low	—	—	— —	17.0 7.0	x ck i ck a	ns
67	SCKR rising edge to FSR out (wr) high[5]	—	—	— —	19.0 9.0	x ck i ck a	ns
68	SCKR rising edge to FSR out (wr) low[5]	—	—	— —	19.0 9.0	x ck i ck a	ns
69	SCKR rising edge to FSR out (wl) high	—	—	— —	16.0 6.0	x ck i ck a	ns
70	SCKR rising edge to FSR out (wl) low	—	—	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before SCKR (SCK in synchronous mode) falling edge	—	—	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR falling edge	—	—	3.5 9.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR falling edge[5]	—	—	2.0 12.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR falling edge	—	—	2.0 12.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR falling edge	—	—	2.5 8.5	— —	x ck i ck a	ns
76	Flags input setup before SCKR falling edge	—	—	0.0 19.0	— —	x ck i ck s	ns
77	Flags input hold time after SCKR falling edge	—	—	6.0 0.0	— —	x ck i ck s	ns
78	SCKT rising edge to FST out (bl) high	—	—	— —	18.0 8.0	x ck i ck	ns
79	SCKT rising edge to FST out (bl) low	—	—	— —	20.0 10.0	x ck i ck	ns
80	SCKT rising edge to FST out (wr) high[5]	—	—	— —	20.0 10.0	x ck i ck	ns
81	SCKT rising edge to FST out (wr) low[5]	—	—	— —	22.0 12.0	x ck i ck	ns
82	SCKT rising edge to FST out (wl) high	—	—	— —	19.0 9.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	—	—	— —	20.0 10.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	—	—	— —	22.0 17.0	x ck i ck	ns
85	SCKT rising edge to transmitter #0 drive enable assertion	—	—	— —	17.0 11.0	x ck i ck	ns

3.7.14.1 SIM Reset Sequences

SIM cards may have internal reset, or active low reset. The following subset describes the reset sequences in these two cases.

3.7.14.1.1 SIM Cards with Internal Reset

Figure 69 shows the reset sequence for SIM cards with internal reset. The reset sequence comprises the following steps:

- After power-up, the clock signal is enabled on SIM*x*_CLK*y* (time T0)
- After 200 clock cycles, SIM*x*_DATA*y*_RX_TX must be asserted.
- The card must send a response on SIM*x*_DATA*y*_RX_TX acknowledging the reset between 400–40000 clock cycles after T0.

Figure 69. Internal Reset Card Reset Sequence

Table 75 defines the general timing requirements for the SIM interface.

3.7.14.1.2 SIM Cards with Active Low Reset

Figure 70 shows the reset sequence for SIM cards with active low reset. The reset sequence comprises the following steps:

- After power-up, the clock signal is enabled on SIM*x*_CLK*y* (time T0)
- After 200 clock cycles, SIM*x*_DATA*y*_RX_TX must be asserted.
- SIM*x*_RST*y*

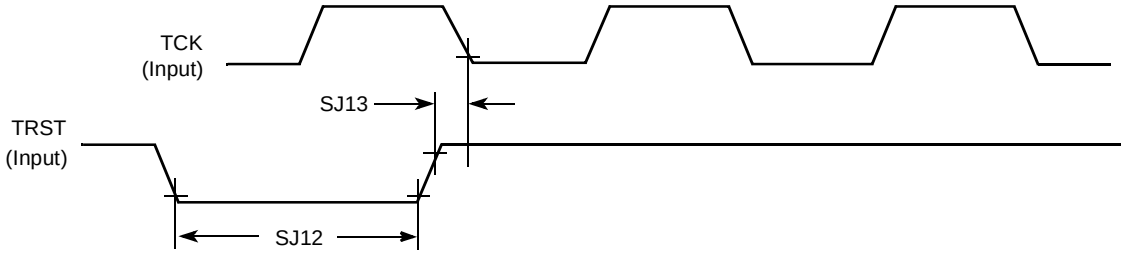

Figure 75. $\overline{\text{TRST}}$ Timing Diagram

Table 78. SJC Timing Parameters

ID	Parameter	All Frequencies		Unit
		Min.	Max.	
SJ1	TCK cycle time	100[1]	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	40	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	10	—	ns
SJ5	Boundary scan input data hold time	50	—	ns
SJ6	TCK low to output data valid	—	50	ns
SJ7	TCK low to output high impedance	—	50	ns
SJ8	TMS, TDI data set-up time	10	—	ns
SJ9	TMS, TDI data hold time	50	—	ns
SJ10	TCK low to TDO data valid	—	44	ns
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

1 In cases where SDMA TAP is put in the chain, the maximum TCK frequency is limited by the maximum ratio of 1:8 of SDMA core frequency to TCK. This implies a maximum frequency of 8.25 MHz (or 121.2 ns) for a 66 MHz IPG clock.

2 $V_{M_}$ mid point voltage

Figure 95 shows the USB transmit waveform in VP_VM unidirectional mode diagram.

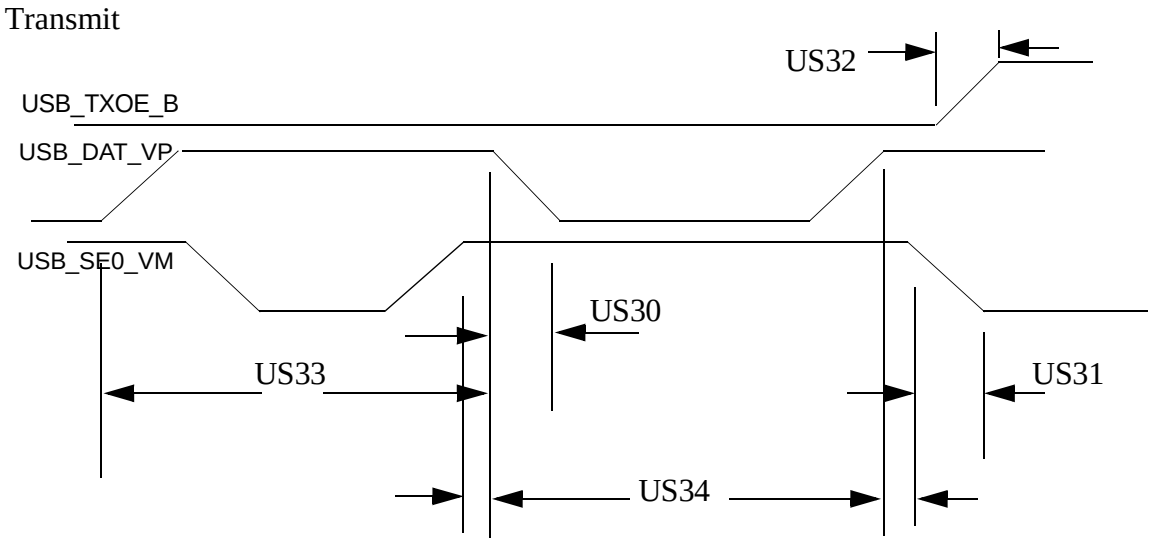

Figure 95. USB Transmit Waveform in VP_VM Unidirectional Mode

Figure 96 shows the USB receive waveform in VP_VM unidirectional mode diagram.

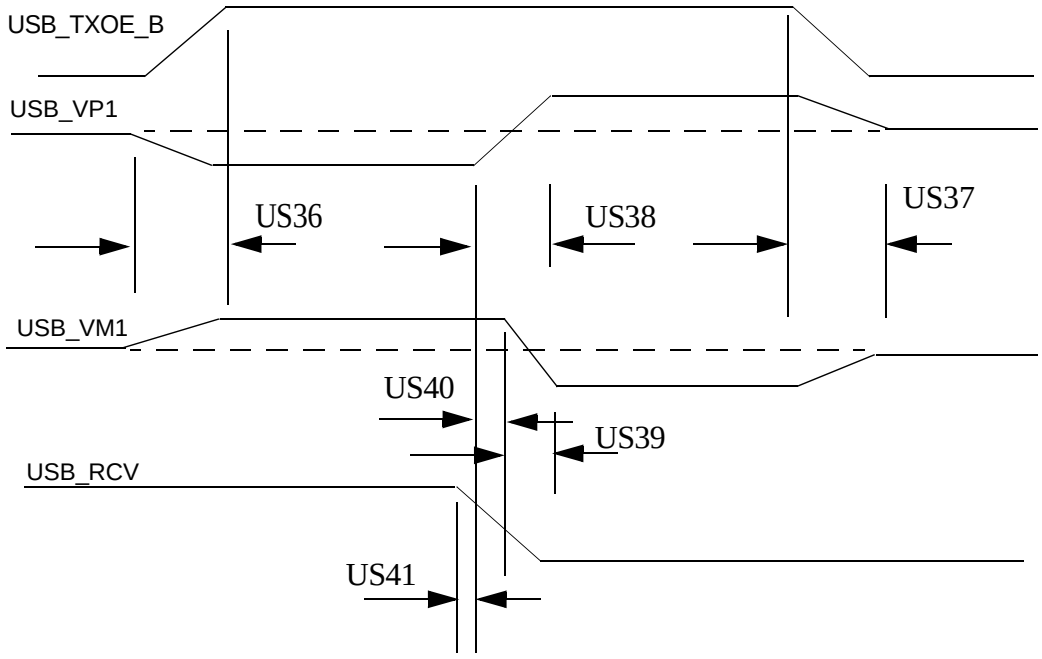

Figure 96. USB Receive Waveform in VP_VM Unidirectional Mode

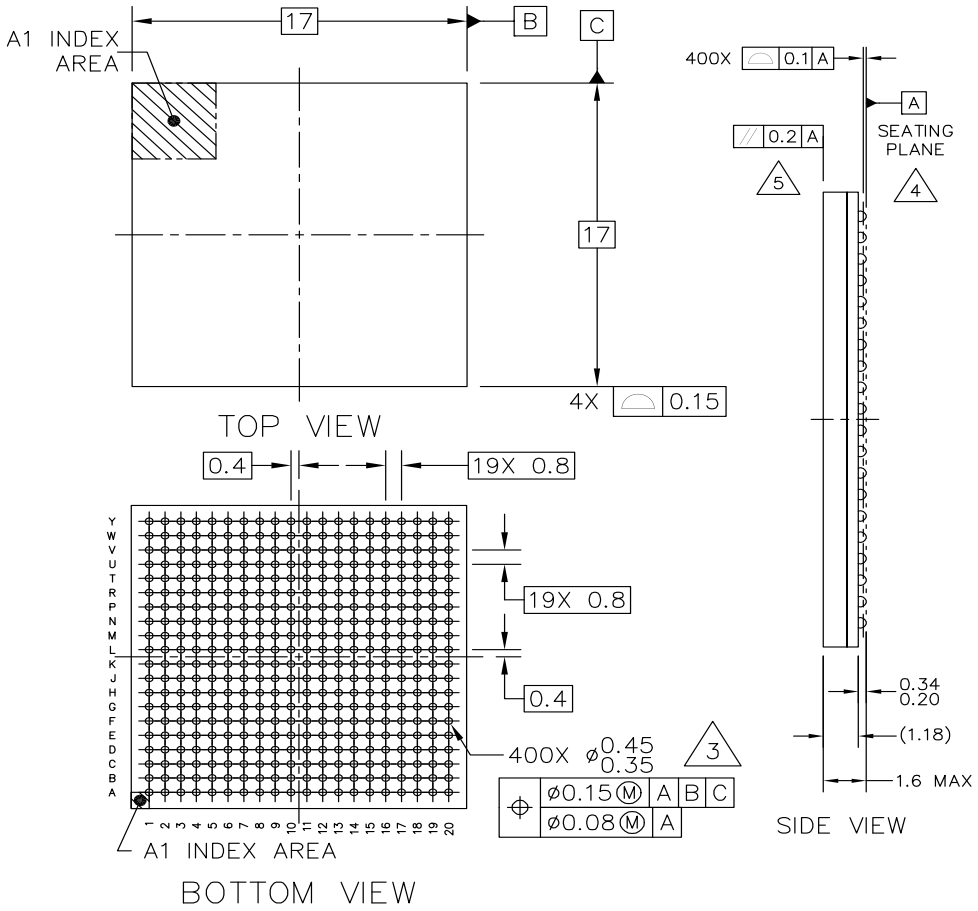

Figure 98. 17×17 i.MX25 Production Package

4.2 Ground, Power, Sense, and Reference Contact Assignments Case 17x17 mm, 0.8 mm Pitch

Table 100 shows the 17×17 mm package ground, power, sense, and reference contact assignments.

Table 100. 17×17 mm Package Ground, Power Sense, and Reference Contact Assignments

Contact Name	Contact Assignment
BATT_VDD	P10
FUSE_VDD	T17
MPLL_GND	U17
MPLL_VDD	U18
NGND_ADC	Y13
NVCC_ADC	W13
NVCC_CRM	N14
NVCC_CSI	J13, J14

Table 101. 17×17 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
I2C1_CLK	F17	CSI	GPIO	INPUT	100 KΩ Pull-Up
I2C1_DAT	G17	CSI	GPIO	INPUT	100 KΩ Pull-Up
CSPI1_MOSI	T4	MISC	GPIO	INPUT	100 KΩ Pull-Up
CSPI1_MISO	W1	MISC	GPIO	OUTPUT	Low
CSPI1_SS0	R4	MISC	GPIO	INPUT	100 KΩ Pull-Up
CSPI1_SS1	V2	MISC	GPIO	INPUT	100 KΩ Pull-Up
CSPI1_SCLK	U3	MISC	GPIO	INPUT	100 KΩ Pull-Up
CSPI1_RDY	V1	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART1_RXD	U2	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART1_TXD	U1	MISC	GPIO	OUTPUT	High
UART1_RTS	T3	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART1_CTS	T2	MISC	GPIO	OUTPUT	High
UART2_RXD	P4	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART2_TXD	T1	MISC	GPIO	OUTPUT	High
UART2_RTS	R3	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART2_CTS	R2	MISC	GPIO	INPUT	-
SD1_CMD	K20	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_CLK	M20	SDIO	GPIO	OUTPUT	High
SD1_DATA0	L20	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_DATA1	N20	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_DATA2	M19	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_DATA3	J20	SDIO	GPIO	INPUT	47 KΩ Pull-Up
KPP_ROW0	N4	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_ROW1	R1	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_ROW2	P3	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_ROW3	P2	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL0	P1	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL1	N3	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL2	N2	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL3	N1	MISC	GPIO	INPUT	100 KΩ Pull-Up
FEC_MDC	L1	MISC	GPIO	OUTPUT	Low
FEC_MDIO	L2	MISC	GPIO	INPUT	22 KΩ Pull-Up

Table 103. i.MX25 17×17 Package Ball Map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
U	UART1_TXD	UART1_RXD	CSPI1_SCLK	CONTRAST	LSCLK	VSYNC	HSYNC	LD3	SJC_MOD	NVCC_JTAG	INAUX0	INAUX2	XN	WIPER	NC_BGA_U15	NC_BGA_U16	MPLL_GND	MPLL_VDD	POR_B	UPLL_BYPCLK
V	CSPI1_RDY	CSPI1_SS1	OE_ACD	LD14	LD12	LD8	LD5	LD1	TRSTB	TCK	REF	INAUX1	YP	XP	NC_BGA_V15	NC_BGA_V16	NC_BGA_V17	TEST_MODE	BOOT_MODE0	CLKO
W	CSPI1_MISO	PWM	LD15	LD13	LD9	LD6	LD2	DE_B	TDI	RTCK	NVCC_DRYICE	YN	NVCC_ADC	NC_BGA_W14	OSC24M_GND	OSC24M_VDD	USBPHY2_VSS	USBPHY2_VDD	CLK_SEL	BOOT_MODE1
Y	QGND	NC_BGA_Y2	LD11	LD10	LD7	LD4	LD0	TDO	TMS	OSC32K_XTAL	OSC32K_EXTAL	OSC_BYP	NGND_ADC	NC_BGA_Y14	OSC24M_EXTAL	OSC24M_XTAL	NC_BGA_Y17	USBPHY2_DP	USBPHY2_DM	QGND