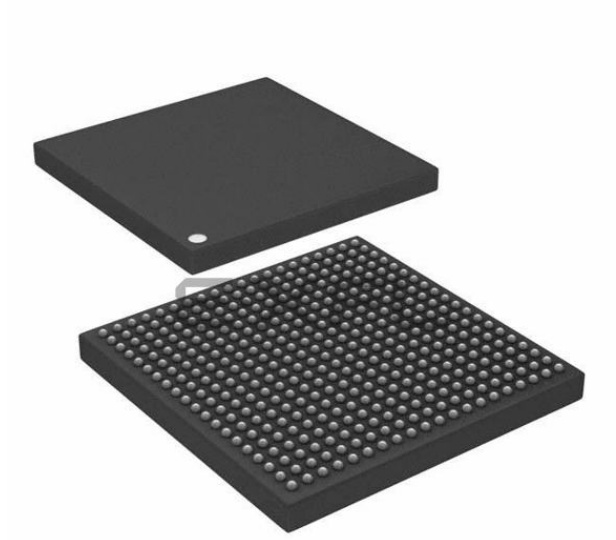


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-20°C ~ 70°C (TA)
Security Features	-
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx253dvm4

Table 3. i.MX25 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SLCD	Smart LCD controller	Multimedia peripherals	The SLCDC module transfers data from the display memory buffer to the external display device.
SPBA	Shared peripheral bus arbiter	System control	The SPBA controls access to the shared peripherals. It supports shared peripheral ownership and access rights to an owned peripheral.
SSI(2)	I2S/SSI/AC97 interface	Connectivity peripherals	The SSI is a full-duplex serial port that allows the processor to communicate with a variety of serial protocols, including the Freescale Semiconductor SPI standard and the inter-IC sound bus standard (I2S). The SSIs interface to the AUDMUX for flexible audio routing.
TSC (and ADC)	Touchscreen controller (and A/D converter)	Multimedia peripherals	The touchscreen controller and associated Analog-to-Digital Converter (ADC) together provide a resistive touchscreen solution. The module implements simultaneous touchscreen control and auxiliary ADC operation for temperature, voltage, and other measurement functions.
UART(5)	UART interface	Connectivity peripherals	Each of the UART modules supports the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, one or two stop bits, programmable parity (even, odd, or none) • Programmable baud rates up to 4 MHz. This is a higher maximum baud rate than the 1.875 MHz specified by the TIA/EIA-232-F standard and previous Freescale UART modules. 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA-1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOTG USBHOST	High-speed USB on-the-go	Connectivity peripherals	The USB module provides high-performance USB On-The-Go (OTG) and host functionality (up to 480 Mbps), compliant with the USB 2.0 specification, the OTG supplement, and the ULPI 1.0 Low Pin Count specification. The module has DMA capabilities for handling data transfer between internal buffers and system memory. An OTG HS PHY and HOST FS PHY are also integrated.

2.1 Special Signal Considerations

Special signal considerations are listed in Table 4. The package contact assignment is found in Section 4, "Package Information and Contact Assignment." Signal descriptions are provided in the reference manual.

Table 4. Signal Considerations

Signal	Description
BAT_VDD	DryIce backup power supply input.
CLK0	Clock-out pin; renders the internal clock visible to users for debugging. The clock source is controllable through CRM registers. This pin can also be configured (through muxing) to work as a normal GPIO.
CLK_SEL	Used to select the ARM clock source from MPLL out or from external EXT_ARMCLK. In normal operation, CLK_SEL should be connected to GND.
EXT_ARMCLK	Primarily for Freescale factory use. There is no internal on-chip pull-up/down on this pin, so it must be externally connected to GND or VDD. Aside from factory use, this pin can also be configured (through muxing) to work as a normal GPIO.

Table 19. DDR2 (SSTL_18) I/O DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Termination voltage[5]	Vtt	—	OVDD/2 – 0.04	OVDD/2	OVDD/2 + 0.04	
Input current[6](no pull-up/down)	IIN	VI = 0 VI = OVDD	—	—	110 60	nA
High-impedance I/O supply current[6]	Icc-ovdd	VI = OVDD or 0	—	—	980	nA
High-impedance core supply current[6]	Icc-vddi	VI = VDD or 0	—	—	1210	nA

1 OVDD = 1.7 V; V_{out} = 1.42 V. (V_{out}-OVDD)/IOH must be less than 21 W for values of V_{out} between OVDD and OVDD-0.28 V.

2 OVDD = 1.7 V; V_{out} = 280 mV. V_{out}/IOL must be less than 21 W for values of V_{out} between 0 V and 280 mV. Simulation circuit for parameters V_{oh} and V_{ol} for I/O cells is below.

3 Vin(dc) specifies the allowable DC excursion of each differential input.

4 Vid(dc) specifies the input differential voltage required for switching. The minimum value is equal to Vih(dc) - Vil(dc).

5 Vtt is expected to track OVDD/2.

6 Minimum condition: BCS model, 1.95 V, and –40 °C. Typical condition: typical model, 1.8 V, and 25 °C. Maximum condition: wcs model, 1.65 V, and 105 °C.

3.5.2 GPIO I/O DC Parameters

Table 20 shows the I/O parameters for GPIO.

Table 20. GPIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
High-level output voltage[1]	Voh	Ioh=–1mA Ioh = Specified Drive	OVDD – 0.15 0.8 × OVDD	—	—	V
Low-level output voltage[1]	Vol	Iol=1mA Iol=Specified Drive	—	—	0.15 0.2 × OVDD	V
High-level output current for slow mode	I Ioh	Voh=0.8 × OVDD Standard Drive High Drive Max. Drive	 –2.0 –4.0 –8.0	—	—	mA
High-level output current for fast mode	I Ioh	Voh=0.8 × OVDD Standard Drive High Drive Max. Drive	 –4.0 –6.0 –8.0	—	—	mA
Low-level output current for slow mode	I Iol	Voh=0.2 × OVDD Standard Drive High Drive Max. Drive	 2.0 4.0 8.0	—	—	mA
Low-level output current for fast mode	I Iol	Voh=0.2 × OVDD Standard Drive High Drive Max. Drive	 4.0 6.0 8.0	—	—	mA
High-level DC input voltage	VIH	—	0.7 × OVDD	—	OVDD	V
Low-level DC input voltage	VIL	—	–0.3 V	—	0.3 × OVDD	V

Table 24. AC Parameters for Mobile DDR I/O (continued)

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Output pad propagation delay[1] (high drive), 40%–60%	tpo	15 pF 35 pF	1.04/1.09 1.63/1.56	1.73/1.83 2.43/2.52	2.69/2.62 3.79/3.62	ns
Output pad propagation delay[1] (standard drive), 40%–60%	tpo	15 pF 35 pF	1.50/1.74 2.73/2.42	2.36/2.41 3.77/3.78	3.67/3.46 5.86/5.37	ns
Output enable to output valid delay[1] (max. drive), 50%–50%	tpv	15 pF 35 pF	1.17/1.01 1.43/1.30	1.93/1.61 2.33/2.00	3.06/2.55 3.69/3.13	ns
Output enable to output valid delay[1] (high drive), 50%–50%	tpv	15 pF 35 pF	1.38/1.28 1.97/1.92	2.25/1.99 3.16/2.86	3.58/3.10 5.01/4.39	ns
Output enable to output valid delay[1] (standard drive), 50%–50%	tpv	15 pF 35 pF	1.92/1.57 3.12/3.16	3.11/2.79 4.97/4.59	4.98/4.13 7.97/6.98	ns
Output enable to output valid delay[1] (max. drive), 40%–60%	tpv	15 pF 35 pF	1.28/1.12 1.49/1.36	2.01/1.70 2.33/2.01	3.09/2.60 3.60/3.06	ns
Output enable to output valid delay[1] (high drive), 40%–60%	tpv	15 pF 35 pF	1.43/1.33 1.90/1.84	2.24/1.99 2.96/2.68	3.47/3.02 4.59/4.03	ns
Output enable to output valid delay[1] (standard drive), 40%–60%	tpv	15 pF 35 pF	1.85/1.78 2.80/2.81	2.91/2.62 4.37/4.53	4.54/3.96 6.88/6.05	ns
Output pad slew rate[2] (max. drive)	tps	25 pF 50 pF	0.80/0.92 0.43/0.50	1.35/1.50 0.72/0.81	2.23/2.27 1.66/1.68	V/ns
Output pad slew rate[2] (high drive)	tps	25 pF 50 pF	0.37/0.43 0.19/0.23	0.62/0.70 0.33/0.37	1.03/1.05 0.75/0.77	V/ns
Output pad slew rate[2] (standard drive)	tps	25 pF 50 pF	0.18/0.22 0.10/0.12	0.31/0.35 0.16/0.18	0.51/0.53 0.38/0.39	V/ns
Output pad dI/dt[3] (max. drive)	tdit	25 pF 50 pF	64 69	171 183	407 432	mA/ns
Output pad dI/dt[3] (high drive)	tdit	25 pF 50 pF	37 39	100 106	232 246	mA/ns
Output pad di/dt[3] (standard drive)	tdit	25 pF 50 pF	18 20	50 52	116 123	mA/ns
Input pad transition times[4]	trfi	1.0 pF	0.07/0.08	0.11/0.13	0.16/0.20	ns
Input pad propagation delay, 50%–50%[4]	tpi	1.0 pF	0.77/1.00	1.22/1.45	1.89/2.21	ns
Input pad propagation delay, 40%–60%[4]	tpi	1.0 pF	1.59/1.82	2.04/2.27	2.69/3.01	ns

1 Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from core is 1 ns (20%–80%).

2 Minimum condition for tps: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

3 Maximum condition for tdit: bcs model, 1.3 V, I/O 1.95 V, and –40 °C.

4 Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.65 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

3.6.3.3 DDR_TYPE = 10 Max Setting I/O AC Parameters and Requirements

Table 29 shows AC parameters for DDR2 I/O.

Table 29. AC Parameters for DDR2 I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	50	60	%
Clock frequency	f	—	—	—	133	MHz
Output pad transition times[1]	tpr	25 pF 50 pF	0.53/0.52 1.01/0.98	0.80/0.72 1.49/1.34	1.19/1.04 2.21/1.90	ns
Output pad propagation delay, 50%–50%[1]	tpo	25 pF 50 pF	0.93/1.25 1.26/1.54	1.56/1.70 2.07/2.19	2.52/2.53 3.29/3.24	ns
Output pad propagation delay, 40%–60%[1]	tpo	25 pF 50 pF	1.01/1.17 1.27/1.53	1.60/1.75 2.00/2.14	2.49/2.52 3.11/3.10	ns
Output enable to output valid delay, 50%–50%[1]	tpv	25 pF 50 pF	1.30/1.19 1.62/1.54	2.17/1.81 2.56/2.29	3.35/2.84 3.35/2.54	ns
Output enable to output valid delay, 40%–60%[1]	tpv	25 pF 50 pF	1.39/1.27 1.64/1.55	2.13/1.86 2.62/2.23	3.38/2.83 4.14/2.38	ns
Output pad slew rate[2]	tps	25 pF 50 pF	0.86/0.98 0.46/054	1.35/1.5 0.72/0.81	2.15/2.19 1.12/1.16	V/ns
Output pad dI/dt[3]	tdit	25 pF 50 pF	65 70	157 167	373 396	mA/ns
Input pad transition times[4]	trfi	1.0 pF	0.07/0.08	0.10/0.12	0.17/0.20	ns
Input pad propagation delay, 50%–50%[4]	tpi	1.0 pF	0.83/0.99	1.23/1.49	1.79/2.04	ns
Input pad propagation delay, 40%–60%[4]	tpi	1.0 pF	1.65/1.81	2.05/2.31	2.60/2.84	ns

1 Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 1. V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.9 V and –40 °C. Input transition time from core is 1 ns (20%–80%).

2 Minimum condition for tps: wcs model, 1.1 V, I/O 1.7 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

3 Maximum condition for tdit: bcs model, 1.3 V, I/O 1.9 V, and –40 °C.

4 Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.7 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.9 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

Table 30 shows AC parameters for DDR2 pbijtov18_33_ddr_clk I/O.

Table 30. AC Parameters for DDR2 pbijtov18_33_ddr_clk I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	50	60	%
Clock frequency	f	—	—	—	133	MHz
Output pad transition times[1]	tpr	25 pF 50 pF	0.53/0.52 1.01/0.98	0.80/0.72 1.49/1.34	1.19/1.04 2.21/1.90	ns
Output pad propagation delay[1], 50%–50% input signals and crossing of output signals	tpo	25 pF 50 pF	1.3/1.21 1.59/1.5	1.97/1.84 2.37/2.24	2.91/2.71 3.48/3.28	ns

Figure 9 and Figure 10 show write 1 and read sequence timing, respectively. Table 34 describes the timing parameters (OW7–OW8) that are shown in the figure.

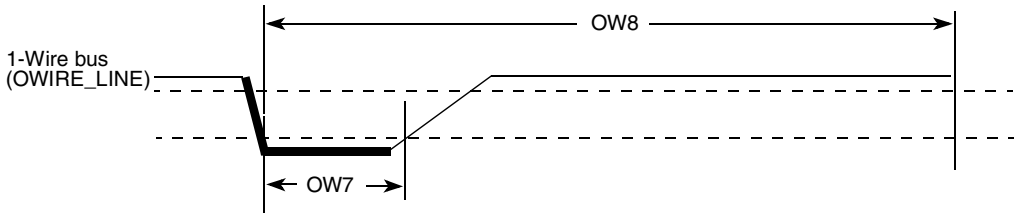


Figure 9. Write 1 Sequence Timing Diagram

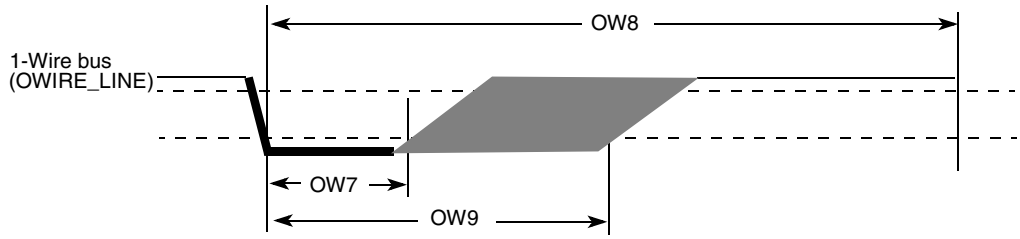


Figure 10. Read Sequence Timing Diagram

Table 34. WR1 /RD Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW7	Write 1 / read low time	t_{LOW1}	1	5	15	µs
OW8	Transmission time slot	t_{SLOT}	60	117	120	µs
OW9	Release time	$t_{RELEASE}$	15	—	45	µs

3.7.2.1 PIO Mode Timing Parameters

Figure 11 shows a timing diagram for PIO read mode.

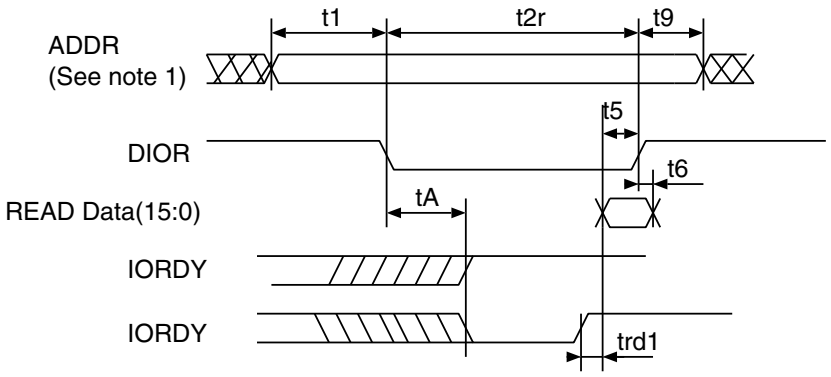


Figure 11. PIO Read Mode Timing

To meet PIO read mode timing requirements, a number of timing parameters must be controlled. Table 36 shows timing parameters and their determining relations, and indicates parameters that can be adjusted to meet required conditions.

Table 36. Timing Parameters for PIO Read Mode

ATA Parameter	PIO Read Mode Timing Parameter[1]	Relation	Adjustable Parameter
t1	t1	t1(min.) = time_1 × T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2r	t2(min.) = time_2r × T – (tskew1 + tskew2 + tskew5)	time_2r
t9	t9	t9(min.) = time_9 × T – (tskew1 + tskew2 + tskew6)	time_9
t5	t5	t5(min.) = tco + tsu + tbuf + tbuf + tcable1 + tcable2	If not met, increase time_2
t6	t6	0	—
tA	tA	tA(min.) = (1.5 + time_ax) × T – (tco + tsui + tcable2 + tcable2 + 2 × tbuf)	time_ax
trd	trd1	trd1(max.) = (–trd) + (tskew3 + tskew4) trd1(min.) = (time_pio_rdx – 0.5) × T – (tsu + thi) (time_pio_rdx – 0.5) × T > tsu + thi + tskew3 + tskew4	time_pio_rdx
t0	—	t0(min.) = (time_1 + time_2 + time_9) × T	time_1, time_2r, time_9

[1] See Figure 11.

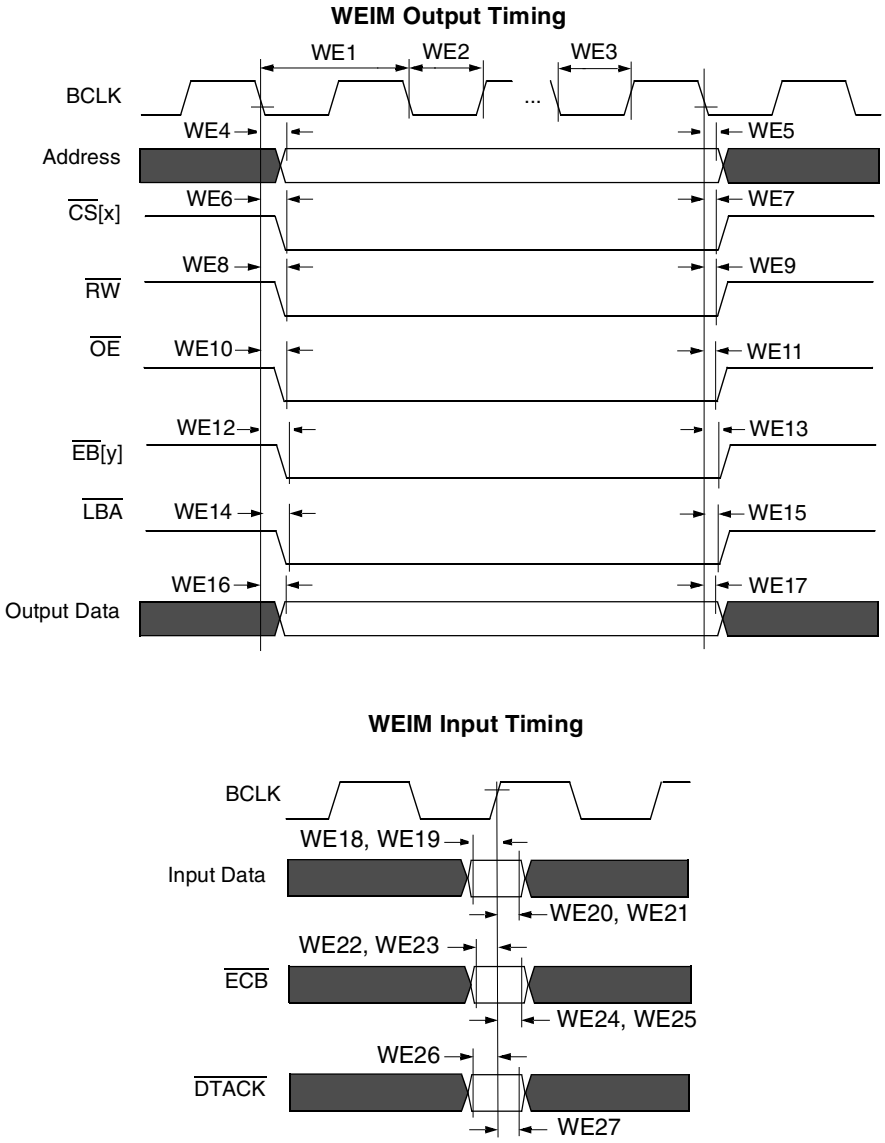


Figure 38. WEIM Bus Timing Diagram

Table 56. WEIM Bus Timing Parameters[1]

ID	Parameter	Min.	Max.	Unit
WE1	BCLK cycle time[2]	14.5	—	ns
WE2	BCLK low-level width[2]	7	—	ns
WE3	BCLK high-level width[2]	7	—	ns
WE4	Clock fall to address valid	15	21	ns
WE5	Clock rise/fall to address invalid	22	25	ns
WE6	Clock rise/fall to $\overline{CS}$[x] valid	15	19	ns
WE7	Clock rise/fall to $\overline{CS}$[x] invalid	3.3	5	ns

Figure 39 through Figure 44 give examples of basic WEIM accesses to external memory devices with the timing parameters described in Table 56 for specific control parameter settings.

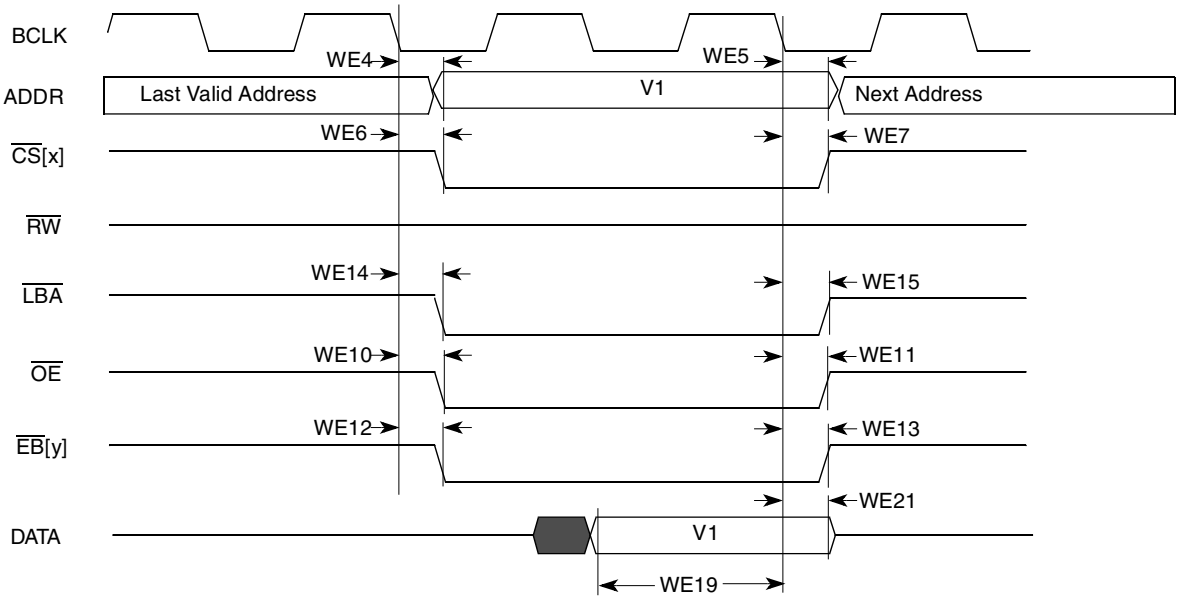


Figure 39. Synchronous Memory Timing Diagram for Read Access—WSC=1

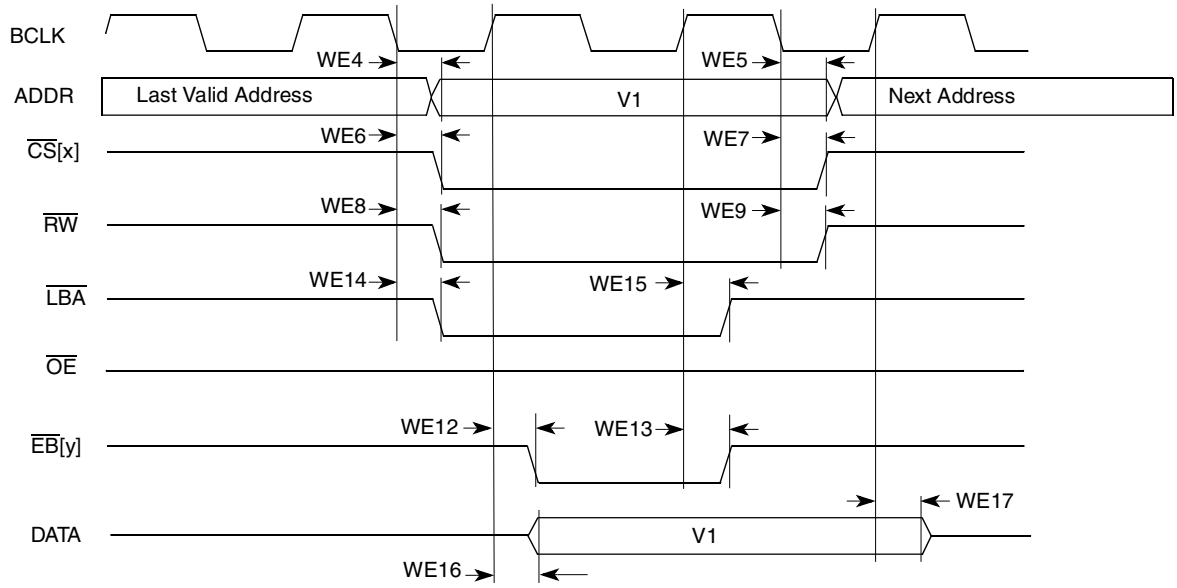


Figure 40. Synchronous Memory Timing Diagram for Write Access—WSC=1, EBWA=1, EBWN=1, LBN=1

Table 60. ESAI General Timing Requirements (continued)

No.	Characteristics[1 2]	Symbol	Expression[3]	Min.	Max.	Condition	Unit
65	SCKR rising edge to FSR out (bl) high	—	—	— —	17.0 7.0	x ck i ck a	ns
66	SCKR rising edge to FSR out (bl) low	—	—	— —	17.0 7.0	x ck i ck a	ns
67	SCKR rising edge to FSR out (wr) high[5]	—	—	— —	19.0 9.0	x ck i ck a	ns
68	SCKR rising edge to FSR out (wr) low[5]	—	—	— —	19.0 9.0	x ck i ck a	ns
69	SCKR rising edge to FSR out (wl) high	—	—	— —	16.0 6.0	x ck i ck a	ns
70	SCKR rising edge to FSR out (wl) low	—	—	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before SCKR (SCK in synchronous mode) falling edge	—	—	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR falling edge	—	—	3.5 9.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR falling edge[5]	—	—	2.0 12.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR falling edge	—	—	2.0 12.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR falling edge	—	—	2.5 8.5	— —	x ck i ck a	ns
76	Flags input setup before SCKR falling edge	—	—	0.0 19.0	— —	x ck i ck s	ns
77	Flags input hold time after SCKR falling edge	—	—	6.0 0.0	— —	x ck i ck s	ns
78	SCKT rising edge to FST out (bl) high	—	—	— —	18.0 8.0	x ck i ck	ns
79	SCKT rising edge to FST out (bl) low	—	—	— —	20.0 10.0	x ck i ck	ns
80	SCKT rising edge to FST out (wr) high[5]	—	—	— —	20.0 10.0	x ck i ck	ns
81	SCKT rising edge to FST out (wr) low[5]	—	—	— —	22.0 12.0	x ck i ck	ns
82	SCKT rising edge to FST out (wl) high	—	—	— —	19.0 9.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	—	—	— —	20.0 10.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	—	—	— —	22.0 17.0	x ck i ck	ns
85	SCKT rising edge to transmitter #0 drive enable assertion	—	—	— —	17.0 11.0	x ck i ck	ns

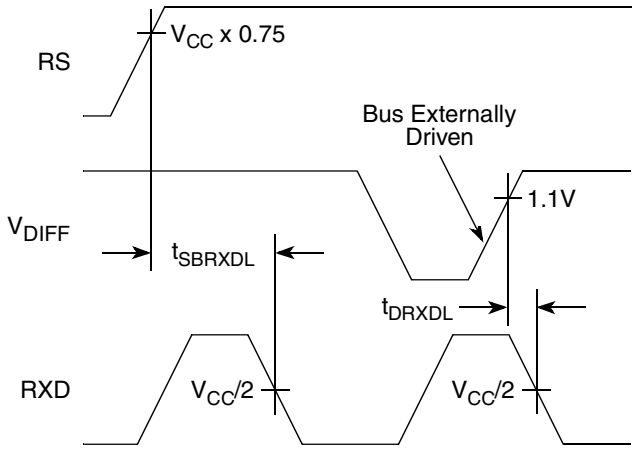


Figure 61. Timing Diagram for FlexCAN Standby Signal

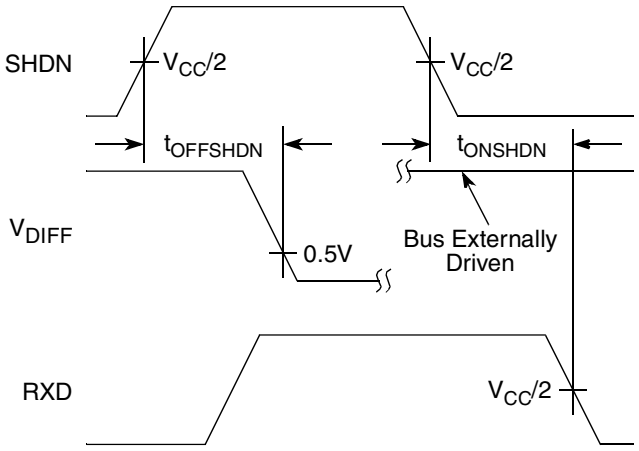


Figure 62. Timing Diagram for FlexCAN Shutdown Signal

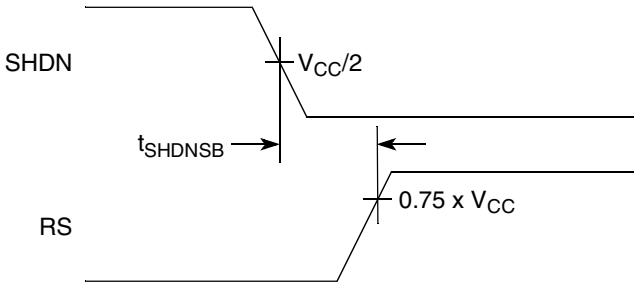


Figure 63. Timing Diagram for FlexCAN Shutdown-to-Standby Signal

Because integer multiples are not possible, taking into account the range of frequencies at which the SoC has to operate, DPLLs work in FOL mode only.

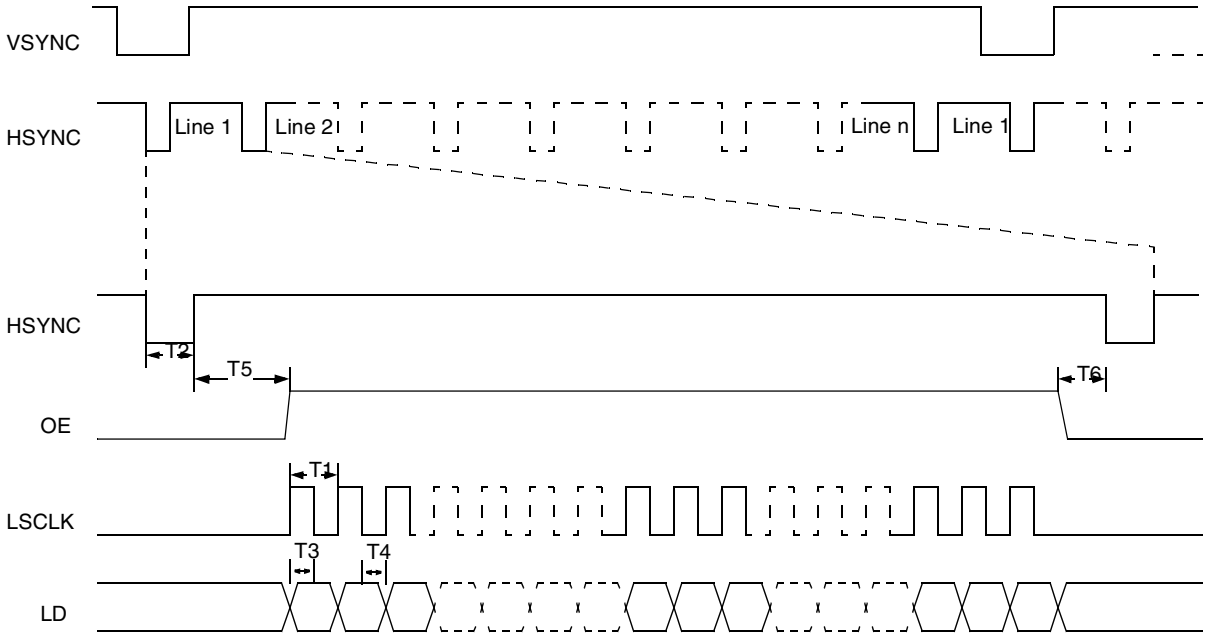


Figure 66. LCDC TFT Mode Timing Diagram

Table 72. LCDC TFT Mode Timing Parameters

ID	Description	Min.	Ma	Unit
T1	Pixel clock period	22.5	1000	ns
T2	HSYNC width	1	—	T[1]
T3	LD setup time	5	—	ns
T4	LD hold time	5	—	ns
T5	Delay from the end of HSYNC to the beginning of the OE pulse	3	—	T[1]
T6	Delay from end of OE to the beginning of the HSYNC pulse	1	—	T[1]

1 T is pixel clock period

3.7.13 Pulse Width Modulator (PWM) Timing Parameters

Figure 67 depicts the timing of the PWM, and Table 73 lists the PWM timing characteristics.

The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse width modulator output (PWMO) external pin.

Table 80. SLCDC Parallel Interface Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{cyc}	Parallel clock cycle time	78 (±) t_{prop}	—	4923	ns
t_{ds}	Data setup time	(t_{cyc} / 2) (±) t_{prop}	—	—	—
t_{dh}	Data hold time	(t_{cyc} / 2) (±) t_{prop}	—	—	—
t_{rss}	Register select setup time	(t_{cyc} / 2) (±) t_{prop}	—	—	—
t_{rsh}	Register select hold time	(t_{cyc} / 2) (±) t_{prop}	—	—	—

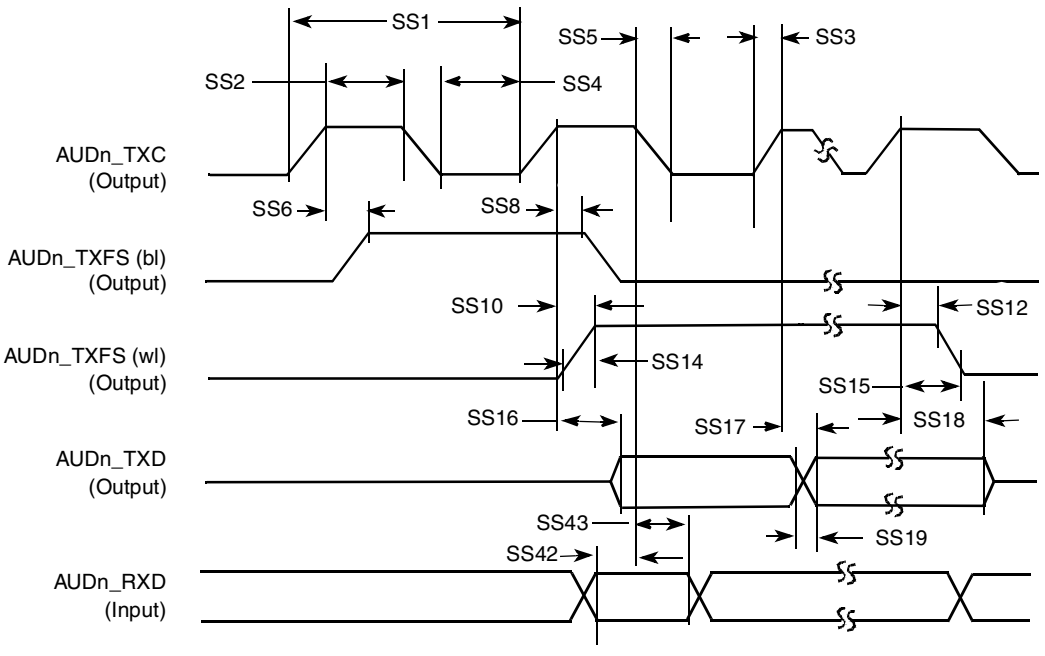
3.7.17 Synchronous Serial Interface (SSI) Timing

The following subsections describe SSI timing in four cases:

- Transmitter with external clock
- Receiver with external clock
- Transmitter with internal clock
- Receiver with internal clock

3.7.17.1 SSI Transmitter Timing with Internal Clock

Figure 78 shows the timing for SSI transmitter with internal clock, and Table 81 describes the timing parameters (SS1–SS52).



Note: SRXD Input in Synchronous mode only

Figure 78. SSI Transmitter with Internal Clock Timing Diagram

3.7.17.4 SSI Receiver Timing with External Clock

Figure 81 shows the timing for SSI receiver with external clock. Table 84 describes the timing parameters (SS22–SS41) used in the figure.

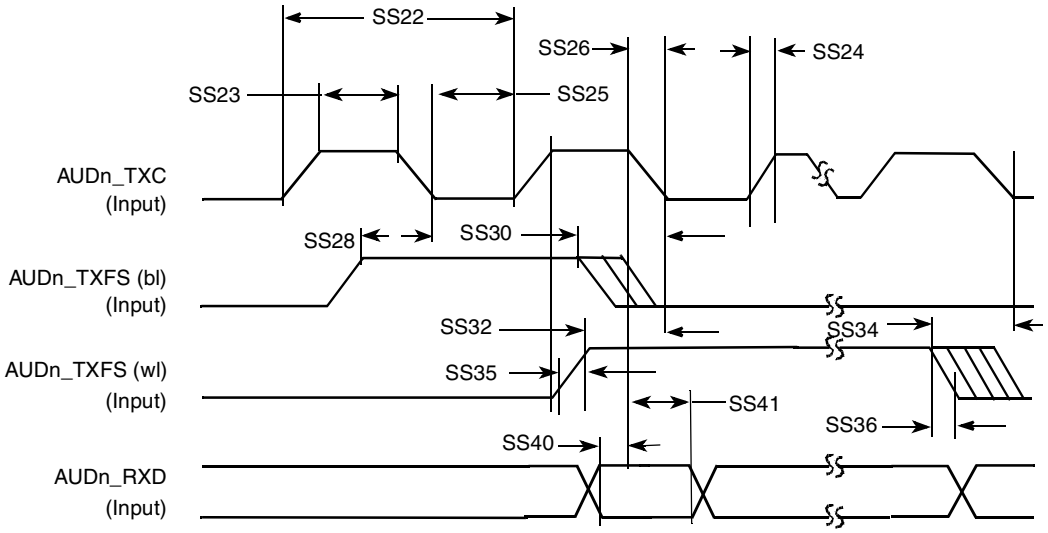


Figure 81. SSI Receiver with External Clock Timing Diagram

Table 84. SSI Receiver Timing with External Clock

ID	Parameter	Min.	Max.	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	FS (bl) low/high setup before (Tx) CK falling	–10.0	15.0	ns
SS30	FS (bl) low/high setup before (Tx) CK falling	10.0	—	ns
SS32	FS (wl) low/high setup before (Tx) CK falling	–10.0	15.0	ns
SS34	FS (wl) low/high setup before (Tx) CK falling	10.0	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10.0	—	ns
SS41	SRXD hold time after (Rx) CK low	2.0	—	ns

Note:

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on pads when SSI is being used for data transfer.

Table 85. Touchscreen ADC Electrical Specifications (continued)

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power-down current NVCC_ADC QV_{DD}	—	—	—	1 10	uA uA
Touchscreen Interface					
Expected plate resistance	—	100	—	1500	Ω
Switch drivers on resistance	GND and VDD switches	—	—	10	Ω
Conversion Characteristics[3]					
DNL[4]	fin = 1 kHz	—	+/–0.75	—	LSB
INL[4]	fin = 1 kHz	—	+/–2.0	—	LSB
Gain + Offset Error	—	—	—	+/–2	%FS

1 This comprises only the required initial dummy conversion cycle. Additional power-up time depends on the *enadc*, *reset* and *soc* signals applied to the touchscreen controller.

2 This value only includes the ADC and the driver switches, but it does not take into account the current consumption in the touchscreen plate. For example, if the plate resistance is 100 W, the total current consumption is about 33 mA.

3 At avdd = 3.3 V, dvdd = 1.2 V, Tjunction = 50 °C, fclk = 1.75 MHz, any process corner, unless otherwise noted.

4 Value measured with a –0.5 dBFS sinusoidal input signal and computed with the code density test.

3.7.18.2 ADC Timing Diagrams

Figure 82 represents the synchronization between the signals *clk*, *soc*, *eoc*, and the output bits in the usage of the internal ADC. After a conversion cycle *eoc* is asserted, a new conversion begins only when the

Figure 90 shows the USB receive waveform in DAT_SE0 bidirectional mode diagram.

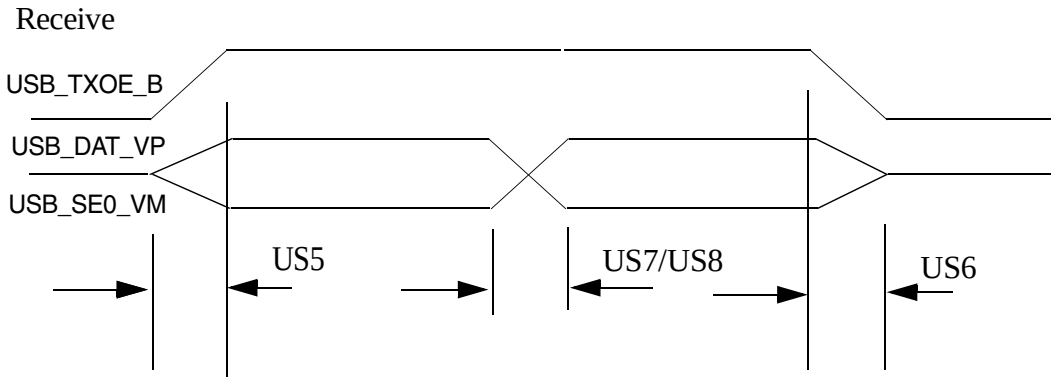


Figure 90. USB Receive Waveform in DAT_SE0 Bidirectional Mode

Table 91 shows the OTG port timing specification in DAT_SE0 bidirectional mode.

Table 91. OTG Port Timing Specification in DAT_SE0 Bidirectional Mode

No.	Parameter	Signal Name	Direction	Min.	Max.	Unit	Conditions/ Reference Signal
US1	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US2	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US3	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US4	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US5	Enable Delay	USB_DAT_VP USB_SE0_VM	In	—	8.0	ns	USB_TXOE_B
US6	Disable Delay	USB_DAT_VP USB_SE0_VM	In	—	10.0	ns	USB_TXOE_B
US7	Rx rise/fall time	USB_DAT_VP	In	—	3.0	ns	35 pF
US8	Rx rise/fall time	USB_SE0_VM	In	—	3.0	ns	35 pF

3.7.20.1.2 DAT_SE0 Unidirectional Mode Timing

Table 92 defines the DAT_SE0 unidirectional mode signals.

Table 92. Signal Definitions—DAT_SE0 Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	Tx data when USB_TXOE_B is low
USB_SE0_VM	Out	SE0 drive when USB_TXOE_B is low
USB_VP1	In	Buffered data on DP when USB_TXOE_B is high
USB_VM1	In	Buffered data on DM when USB_TXOE_B is high
USB_RCV	In	Differential Rx data when USB_TXOE_B is high

3.7.20.1.3 VP_VM Bidirectional Mode Timing

Table 94 defines the VP_VM bidirectional mode signals.

Table 94. Signal Definitions—VP_VM Bidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	• Transmit enable, active low
USB_DAT_VP	Out (Tx) In (Rx)	• Tx VP data when USB_TXOE_B is low • Rx VP data when USB_TXOE_B is high
USB_SE0_VM	Out (Tx) In (Rx)	• Tx VM data when USB_TXOE_B low • Rx VM data when USB_TXOE_B high
USB_RCV	In	• Differential Rx data

Figure 93 shows the USB transmit waveform in VP_VM bidirectional mode diagram.

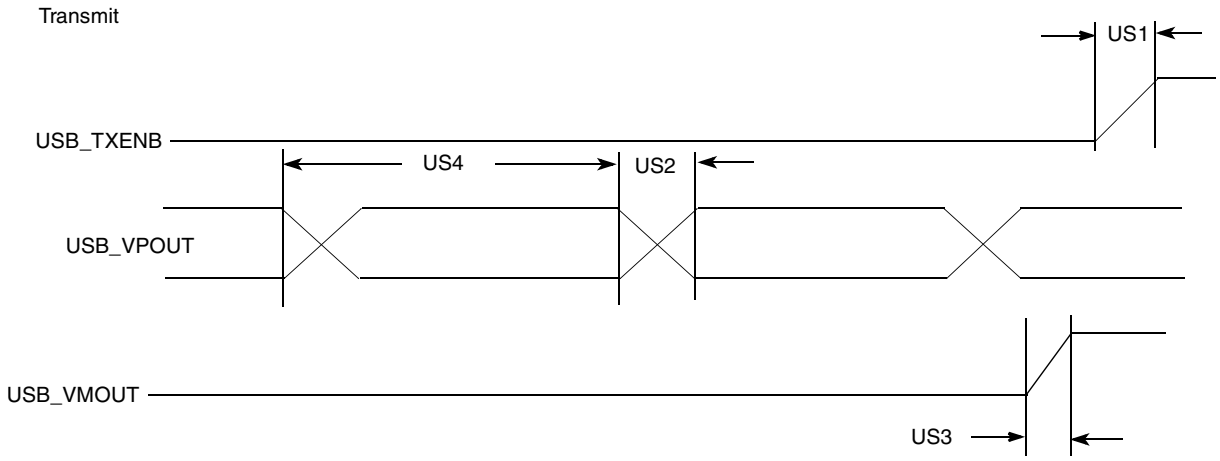


Figure 93. USB Transmit Waveform in VP_VM Bidirectional Mode

Figure 94 shows the USB receive waveform in VP_VM bidirectional mode diagram.

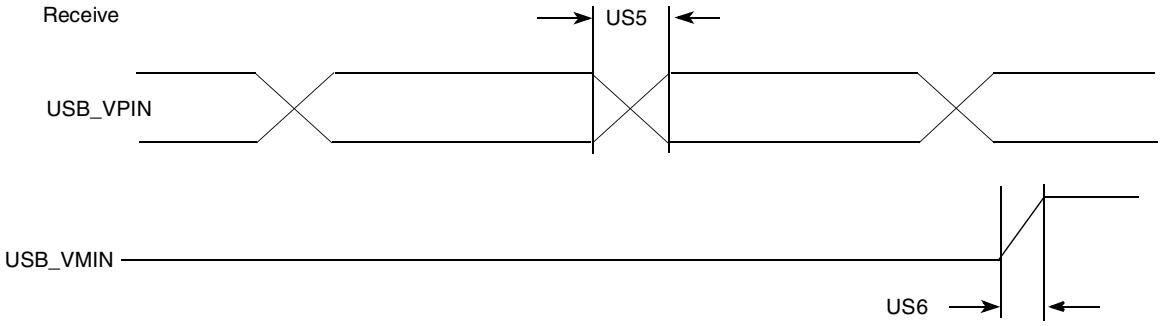


Figure 94. USB Receive Waveform in VP_VM Bidirectional Mode

Figure 97 shows the USB parallel mode transmit/receive waveform. Table 99 describes the timing parameters (USB15–USB17) shown in the figure.

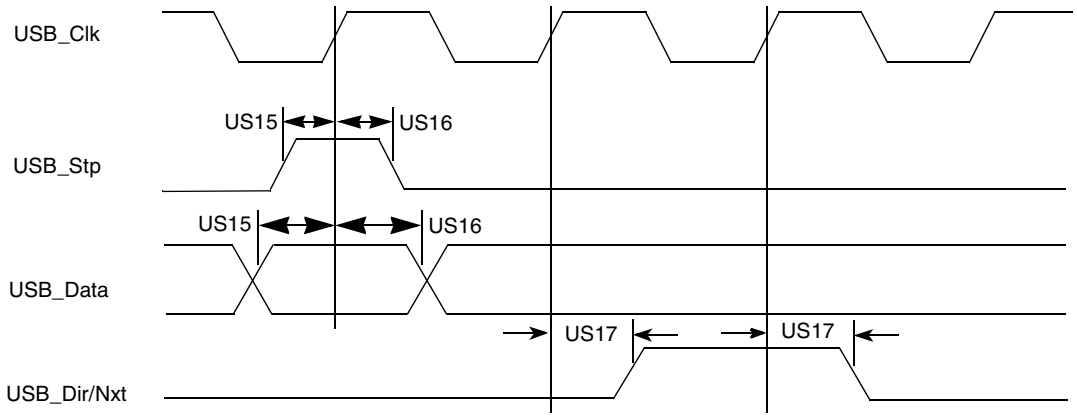


Figure 97. USB Parallel Mode Transmit/Receive Waveform

Table 99. USB Timing Specification in Parallel Mode

ID	Parameter	Min.	Max.	Unit	Conditions/Reference Signal
US15	Setup time (Dir&Nxt in, Data in)	6.0	—	ns	10 pF
US16	Hold time (Dir&Nxt in, Data in)	0.0	—	ns	10 pF
US17	Output delay time (Stp out, Data out	—	9.0	ns	10 pF

4 Package Information and Contact Assignment

4.1 400 MAPBGA—Case 17x17 mm, 0.8 mm Pitch

Figure 98 shows the 17×17 mm i.MX25 production package. The following notes apply to Figure 98:

- All dimensions in millimeters.
- Dimensioning and tolerancing per ASME Y14.5M-1994.
- Maximum solder bump diameter measured parallel to datum A.
- Datum A, the seating plane, is determined by the spherical crowns of the solder bumps.
- Parallelism measurement shall exclude any effect of mark on top surface of package.

4.4 i.MX25 17x17 Package Ball Map

Table 103 shows the i.MX25 17×17 package ball map.

Table 103. i.MX25 17×17 Package Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	QGND	A10	A14	A19	A22	A23	A25	SD15	SD13	SD7	QGND	SD0	SD5	SDCLK_B	SDWE	SDBA1	CS3	A0	A5	QGND
B	LBA	ECB	EB0	A15	A17	A20	A24	SDQS1	SD8	SD10	QGND	SDQS0	SD2	SDCLK	SDBA0	CS2	A1	A3	A7	NC_BGA_B20
C	NFRE_B	NFRB	CS0	RW	EB1	A16	A21	DQM1	SD12	SD11	QGND	DQM0	SD1	RAS	SDCKE1	CAS	A2	A9	A6	A4
D	D9	NF_CE0	CS1	CS5	CS4	OE	A18	BCLK	SD14	SD9	QGND	SD6	SD4	SD3	SDCKE0	MA10	A12	A8	A13	A11
E	D2	D8	D0	NFCLE	QGND	QGND	QGND	QGND	QGND	QGND	QGND	QGND	QGND	QGND	QGND	QGND	NC_BGA_E17	CSI_D7	CSI_D3	CSI_D6
F	D11	D10	D1	NFALE	QGND	QGND	QGND	QGND	QGND	QGND	QGND	QGND	QGND	QGND	QGND	QGND	I2C1_CLK	CSI_D2	CSI_D4	CSI_D9
G	D5	D4	D3	NFWE_B	QGND	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	QGND	QVDD	NVCC_EMI2	NVCC_EMI2	NVCC_EMI2	NVCC_EMI2	QGND	I2C1_DAT	CSI_D5	CSI_D8	CSI_VSYNC
H	D6	D13	D12	NFWP_B	QGND	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	QGND	QGND	QGND	NVCC_EMI2	NVCC_EMI2	NVCC_EMI2	QGND	QGND	NC_BGA_H17	CSI_MCLK	CSI_HSYNC	CSI_PIXCLK
J	D14	D15	D7	FEC_TDATA1	QGND	NVCC_EMI1	NVCC_EMI1	QVDD	QGND	QGND	QGND	QVDD	NVCC_CSI	NVCC_CSI	QGND	QGND	USBPHY1_VSSA_BIAS	USBPHY1_UID	NC_BGA_J19	SD1_DATA3

Table 103. i.MX25 17×17 Package Ball Map (continued)

	T	R	P	N	M	L	K
1	UART2_TXD	KPP_ROW1	KPP_COL0	KPP_COL3	FEC_RDATA0	FEC_MDC	QGND
2	UART1_CTS	UART2_CTS	KPP_ROW3	KPP_COL2	FEC_TX_EN	FEC_MDIO	QGND
3	UART1_RTS	UART2_RTS	KPP_ROW2	KPP_COL1	FEC_RX_DV	FEC_TDATA0	QGND
4	CSPI1_MOSI	CSPI1_SS0	UART2_RXD	KPP_ROW0	FEC_RDATA1	FEC_TX_CLK	QGND
5	QGND	QGND	QGND	NVCC_MISC	QVDD	QGND	QGND
6	QGND	NVCC_LCDC	NVCC_LCDC	NVCC_MISC	QVDD	NVCC_NFC	QVDD
7	QGND	NVCC_LCDC	NVCC_LCDC	NVCC_MISC	QVDD	NVCC_NFC	QVDD
8	QGND	QGND	QVDD	QVDD	QGND	NVCC_NFC	QGND
9	QGND	QGND	QVDD	QGND	QGND	QGND	QGND
10	QGND	QGND	BAT_VDD	TAMPER_A	QGND	QGND	QGND
11	QGND	QGND	MESH_C	TAMPER_B	QGND	QGND	QGND
12	QGND	QGND	MESH_D	QGND	QGND	QGND	QVDD
13	QGND	QGND	QGND	QGND	QGND	QGND	QGND
14	QGND	QGND	QGND	NVCC_CRM	QGND	QGND	QGND
15	QGND	QGND	QGND	QGND	QGND	QGND	QGND
16	QGND	QGND	QGND	QGND	UPLL_GND	UPLL_VDD	USBPHY1_VDDA
17	FUSE_VDD	NVCC_SDIO	GPIO_C	USBPHY1_UPLLVSS	USBPHY1_UPLLVDD	USBPHY1_RREF	USBPHY1_VBUS
18	RESET_B	VSTBY_REQ	GPIO_E	GPIO_B	NC_BGA_M18	USBPHY1_DP	USBPHY1_DM
19	POWER_FAIL	GPIO_F	GPIO_D	GPIO_A	SD1_DATA2	USBPHY1_VSSA	USBPHY1_VDDA_BIAS
20	VSTBY_ACK	EXT_ARMCLK	NC_BGA_P20	SD1_DATA1	SD1_CLK	SD1_DATA0	SD1_CMD

Table 105. 12x12 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
A20	B6	EMI1	DDR	OUTPUT	Low
A21	D7	EMI1	DDR	OUTPUT	Low
A22	A7	EMI1	DDR	OUTPUT	Low
A23	E9	EMI1	DDR	OUTPUT	Low
A24	B7	EMI1	DDR	OUTPUT	Low
A25	D8	EMI1	DDR	OUTPUT	Low
SD0	A13	EMI1	DDR	INPUT	Keeper
SD1	D12	EMI1	DDR	INPUT	Keeper
SD2	B12	EMI1	DDR	INPUT	Keeper
SD3	A14	EMI1	DDR	INPUT	Keeper
SD4	B13	EMI1	DDR	INPUT	Keeper
SD5	A15	EMI1	DDR	INPUT	Keeper
SD6	B11	EMI1	DDR	INPUT	Keeper
SD7	A12	EMI1	DDR	INPUT	Keeper
SD8	D10	EMI1	DDR	INPUT	Keeper
SD9	A10	EMI1	DDR	INPUT	Keeper
SD10	A11	EMI1	DDR	INPUT	Keeper
SD11	B10	EMI1	DDR	INPUT	Keeper
SD12	B9	EMI1	DDR	INPUT	Keeper
SD13	E11	EMI1	DDR	INPUT	Keeper
SD14	B8	EMI1	DDR	INPUT	Keeper
SD15	D9	EMI1	DDR	INPUT	Keeper
SDBA1	D16	EMI2	DDR	OUTPUT	Low
SDBA0	A17	EMI2	DDR	OUTPUT	Low
DQM0	D11	EMI1	DDR	OUTPUT	High
DQM1	A9	EMI1	DDR	OUTPUT	High
RAS	D15	EMI2	DDR	OUTPUT	High
CAS	B16	EMI2	DDR	OUTPUT	High
SDWE	B15	EMI2	DDR	OUTPUT	High
SDCKE0	A16	EMI2	DDR	OUTPUT	High
SDCKE1	F16	EMI2	DDR	OUTPUT	High
SDCLK	D13	EMI2	DDR	OUTPUT	Low