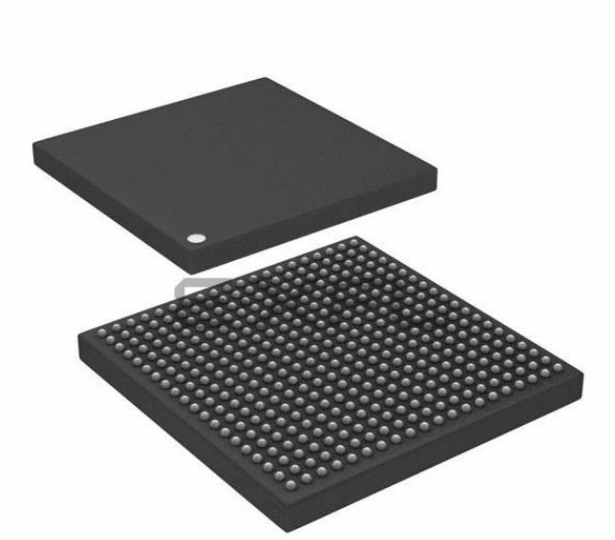

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx257cjm4

Table 2 shows the functional differences between the different parts in the i.MX25 family.

Table 2. i.MX25 Parts Functional Differences

Features	MCIMX253	MCIMX257	MCIMX258
Core	ARM 926EJ-S	ARM 926EJ-S	ARM 926EJ-S
CPU Speed	400 MHz	400 MHz	400 MHz
L1 I/D Cache	16K I/D	16K I/D	16K I/D
On-chip SRAM	128 KB	128 KB	128 KB
PATA/CE-ATA	Yes	Yes	Yes
LCD Controller	Yes	Yes	Yes
Touchscreen	—	Yes	Yes
CSI	—	Yes	Yes
FlexCAN (2)	—	Yes	Yes
ESAI	—	Yes	Yes
SIM (2)	—	Yes	Yes
Security	—	—	Yes
10/100 Ethernet	Yes	Yes	Yes
HS USB 2.0 OTG + PHY	Yes	Yes	Yes
HS USB 2.0 Host + PHY	Yes	Yes	Yes
12-bit ADC	Yes	Yes	Yes
SD/SDIO/MMC (2)	Yes	Yes	Yes
External Memory Controller	Yes	Yes	Yes
I^2C (3)	Yes	Yes	Yes
SSI/I2S (2)	Yes	Yes	Yes
CSPI (2)	Yes	Yes	Yes
UART (5)	Yes	Yes	Yes

Table 3. i.MX25 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SLCD	Smart LCD controller	Multimedia peripherals	The SLCDC module transfers data from the display memory buffer to the external display device.
SPBA	Shared peripheral bus arbiter	System control	The SPBA controls access to the shared peripherals. It supports shared peripheral ownership and access rights to an owned peripheral.
SSI(2)	I2S/SSI/AC97 interface	Connectivity peripherals	The SSI is a full-duplex serial port that allows the processor to communicate with a variety of serial protocols, including the Freescale Semiconductor SPI standard and the inter-IC sound bus standard (I2S). The SSIs interface to the AUDMUX for flexible audio routing.
TSC (and ADC)	Touchscreen controller (and A/D converter)	Multimedia peripherals	The touchscreen controller and associated Analog-to-Digital Converter (ADC) together provide a resistive touchscreen solution. The module implements simultaneous touchscreen control and auxiliary ADC operation for temperature, voltage, and other measurement functions.
UART(5)	UART interface	Connectivity peripherals	Each of the UART modules supports the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, one or two stop bits, programmable parity (even, odd, or none) • Programmable baud rates up to 4 MHz. This is a higher maximum baud rate than the 1.875 MHz specified by the TIA/EIA-232-F standard and previous Freescale UART modules. 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA-1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOTG USBHOST	High-speed USB on-the-go	Connectivity peripherals	The USB module provides high-performance USB On-The-Go (OTG) and host functionality (up to 480 Mbps), compliant with the USB 2.0 specification, the OTG supplement, and the ULPI 1.0 Low Pin Count specification. The module has DMA capabilities for handling data transfer between internal buffers and system memory. An OTG HS PHY and HOST FS PHY are also integrated.

2.1 Special Signal Considerations

Special signal considerations are listed in Table 4. The package contact assignment is found in Section 4, "Package Information and Contact Assignment." Signal descriptions are provided in the reference manual.

Table 4. Signal Considerations

Signal	Description
BAT_VDD	DryIce backup power supply input.
CLK0	Clock-out pin; renders the internal clock visible to users for debugging. The clock source is controllable through CRM registers. This pin can also be configured (through muxing) to work as a normal GPIO.
CLK_SEL	Used to select the ARM clock source from MPLL out or from external EXT_ARMCLK. In normal operation, CLK_SEL should be connected to GND.
EXT_ARMCLK	Primarily for Freescale factory use. There is no internal on-chip pull-up/down on this pin, so it must be externally connected to GND or VDD. Aside from factory use, this pin can also be configured (through muxing) to work as a normal GPIO.

3 Electrical Characteristics

This section provides the device-level and module-level electrical characteristics for the i.MX25.

3.1 i.MX25 Chip-Level Conditions

This section provides the chip-level electrical characteristics for the IC.

3.1.1 DC Absolute Maximum Ratings

Table 5 provides the DC absolute maximum operating conditions.

CAUTION

- Stresses beyond those listed under Table 5 may cause permanent damage to the device.
- Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- Table 5 gives stress ratings only—functional operation of the device is not implied beyond the conditions indicated in Table 6.

Table 5. DC Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply voltage	QV_{DD}	–0.5	1.52	V
Supply voltage (level shift i/o)	$V_{DDIOmax}$	–0.5	3.6	V
ESD damage immunity:	V_{esd}			V
Human body model (HBM)		—	2500	
Charge device model (CDM)		—	400	
Machine model (MM)		—	200	
Input voltage range	V_{Imax}	–0.5	NV_{DD} + 0.3	V
Storage temperature range	$T_{storage}$	–40	105	°C

3.1.2 DC Operating Conditions

Table 6 provides the DC recommended operating conditions.

Table 6. DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Core supply voltage (at 266 MHz)	QV_{DD}	1.15	1.34	1.52	V
Core supply voltage (at 400 MHz)	QV_{DD}	1.38	1.45	1.52	V
Coin battery[1] BAT_VDD	V_{DD_BAT}	1.15	—	1.55	V
I/O supply voltage, GPIO NFC,CSI,SDIO	NV_{DD_GPIO1}	1.75	—	3.6	V

Table 6. DC Operating Conditions (continued)

Parameter	Symbol	Min.	Typ.	Max.	Units
I/O supply voltage, GPIO CRM,LCDC,JTAG,MISC	NV_{DD_GPIO2}	3.0	3.3	3.6	—
I/O supply voltage DDR (Mobile DDR mode) EMI1, EMI2	NV_{DD_MDDR}	1.75	—	1.95	V
I/O supply voltage DDR (DDR2 mode) EMI1,EMI2	NV_{DD_DDR2}	1.75	—	1.9	V
I/O supply voltage DDR (SDRAM mode) EMI1,EMI2	NV_{DD_SDRAM}	1.75	—	3.6	V
Supply of USBPHY1 (HS) USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD,USBPHY1_VDDA	$V_{DD\_usbphy1}$	3.17	3.3	3.43	V
Supply of USBPHY2 (FS) USBPHY2_VDD	$V_{DD\_usbphy2}$	3.0	3.3	3.6	V
Supply of OSC24M OSC24M_VDD	V_{DD_OSC24M}	3.0	3.3	3.6	V
Supply of PLL MPLL_VDD,UPLL_VDD	V_{DD_PLL}	1.4	—	1.65	V
Supply of touchscreen ADC NVCC_ADC	V_{DD_tsc}	3.0	3.3	3.6	V
External reference of touchscreen ADC Ref	Vref	2.5	V_{DD_tsc}	V_{DD_tsc}	V
Fusebox program supply voltage FUSE_VDD[2]	$FUSEV_{DD}$ (program mode)	3.3 ± 5%	—	3.6	V
Supply output[3] NVCC_DRYICE	$V_{DD\_}$	1.0	—	1.55	V
Operating ambient temperature	T_A	–40	—	85	°C

1 V_{DD_BAT} must always be powered by battery in security application. In non-security case, V_{DD_BAT} can be connected to QV_{DD}.

2 The fusebox read supply is connected to supply of the full speed USBPHY2_VDD. FUSE_VDD is only used for programming. It is recommended that FUSE_VDD be connected to ground when not being used for programming. See Table 7 for current parameters.

3 NVCC_DRYICE is a supply output. An external capacitor no less than 4 µF must be connected to it. A 4.7 µF capacitor is recommended.

Table 24. AC Parameters for Mobile DDR I/O (continued)

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Output pad propagation delay[1] (high drive), 40%–60%	tpo	15 pF 35 pF	1.04/1.09 1.63/1.56	1.73/1.83 2.43/2.52	2.69/2.62 3.79/3.62	ns
Output pad propagation delay[1] (standard drive), 40%–60%	tpo	15 pF 35 pF	1.50/1.74 2.73/2.42	2.36/2.41 3.77/3.78	3.67/3.46 5.86/5.37	ns
Output enable to output valid delay[1] (max. drive), 50%–50%	tpv	15 pF 35 pF	1.17/1.01 1.43/1.30	1.93/1.61 2.33/2.00	3.06/2.55 3.69/3.13	ns
Output enable to output valid delay[1] (high drive), 50%–50%	tpv	15 pF 35 pF	1.38/1.28 1.97/1.92	2.25/1.99 3.16/2.86	3.58/3.10 5.01/4.39	ns
Output enable to output valid delay[1] (standard drive), 50%–50%	tpv	15 pF 35 pF	1.92/1.57 3.12/3.16	3.11/2.79 4.97/4.59	4.98/4.13 7.97/6.98	ns
Output enable to output valid delay[1] (max. drive), 40%–60%	tpv	15 pF 35 pF	1.28/1.12 1.49/1.36	2.01/1.70 2.33/2.01	3.09/2.60 3.60/3.06	ns
Output enable to output valid delay[1] (high drive), 40%–60%	tpv	15 pF 35 pF	1.43/1.33 1.90/1.84	2.24/1.99 2.96/2.68	3.47/3.02 4.59/4.03	ns
Output enable to output valid delay[1] (standard drive), 40%–60%	tpv	15 pF 35 pF	1.85/1.78 2.80/2.81	2.91/2.62 4.37/4.53	4.54/3.96 6.88/6.05	ns
Output pad slew rate[2] (max. drive)	tps	25 pF 50 pF	0.80/0.92 0.43/0.50	1.35/1.50 0.72/0.81	2.23/2.27 1.66/1.68	V/ns
Output pad slew rate[2] (high drive)	tps	25 pF 50 pF	0.37/0.43 0.19/0.23	0.62/0.70 0.33/0.37	1.03/1.05 0.75/0.77	V/ns
Output pad slew rate[2] (standard drive)	tps	25 pF 50 pF	0.18/0.22 0.10/0.12	0.31/0.35 0.16/0.18	0.51/0.53 0.38/0.39	V/ns
Output pad dI/dt[3] (max. drive)	tdit	25 pF 50 pF	64 69	171 183	407 432	mA/ns
Output pad dI/dt[3] (high drive)	tdit	25 pF 50 pF	37 39	100 106	232 246	mA/ns
Output pad di/dt[3] (standard drive)	tdit	25 pF 50 pF	18 20	50 52	116 123	mA/ns
Input pad transition times[4]	trfi	1.0 pF	0.07/0.08	0.11/0.13	0.16/0.20	ns
Input pad propagation delay, 50%–50%[4]	tpi	1.0 pF	0.77/1.00	1.22/1.45	1.89/2.21	ns
Input pad propagation delay, 40%–60%[4]	tpi	1.0 pF	1.59/1.82	2.04/2.27	2.69/3.01	ns

1 Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from core is 1 ns (20%–80%).

2 Minimum condition for tps: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

3 Maximum condition for tdit: bcs model, 1.3 V, I/O 1.95 V, and –40 °C.

4 Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.65 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

3.6.3.3 DDR_TYPE = 10 Max Setting I/O AC Parameters and Requirements

Table 29 shows AC parameters for DDR2 I/O.

Table 29. AC Parameters for DDR2 I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	50	60	%
Clock frequency	f	—	—	—	133	MHz
Output pad transition times[1]	tpr	25 pF 50 pF	0.53/0.52 1.01/0.98	0.80/0.72 1.49/1.34	1.19/1.04 2.21/1.90	ns
Output pad propagation delay, 50%–50%[1]	tpo	25 pF 50 pF	0.93/1.25 1.26/1.54	1.56/1.70 2.07/2.19	2.52/2.53 3.29/3.24	ns
Output pad propagation delay, 40%–60%[1]	tpo	25 pF 50 pF	1.01/1.17 1.27/1.53	1.60/1.75 2.00/2.14	2.49/2.52 3.11/3.10	ns
Output enable to output valid delay, 50%–50%[1]	tpv	25 pF 50 pF	1.30/1.19 1.62/1.54	2.17/1.81 2.56/2.29	3.35/2.84 3.35/2.54	ns
Output enable to output valid delay, 40%–60%[1]	tpv	25 pF 50 pF	1.39/1.27 1.64/1.55	2.13/1.86 2.62/2.23	3.38/2.83 4.14/2.38	ns
Output pad slew rate[2]	tps	25 pF 50 pF	0.86/0.98 0.46/054	1.35/1.5 0.72/0.81	2.15/2.19 1.12/1.16	V/ns
Output pad dI/dt[3]	tdit	25 pF 50 pF	65 70	157 167	373 396	mA/ns
Input pad transition times[4]	trfi	1.0 pF	0.07/0.08	0.10/0.12	0.17/0.20	ns
Input pad propagation delay, 50%–50%[4]	tpi	1.0 pF	0.83/0.99	1.23/1.49	1.79/2.04	ns
Input pad propagation delay, 40%–60%[4]	tpi	1.0 pF	1.65/1.81	2.05/2.31	2.60/2.84	ns

1 Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 1. V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.9 V and –40 °C. Input transition time from core is 1 ns (20%–80%).

2 Minimum condition for tps: wcs model, 1.1 V, I/O 1.7 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

3 Maximum condition for tdit: bcs model, 1.3 V, I/O 1.9 V, and –40 °C.

4 Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.7 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.9 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

Table 30 shows AC parameters for DDR2 pbijtov18_33_ddr_clk I/O.

Table 30. AC Parameters for DDR2 pbijtov18_33_ddr_clk I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	50	60	%
Clock frequency	f	—	—	—	133	MHz
Output pad transition times[1]	tpr	25 pF 50 pF	0.53/0.52 1.01/0.98	0.80/0.72 1.49/1.34	1.19/1.04 2.21/1.90	ns
Output pad propagation delay[1], 50%–50% input signals and crossing of output signals	tpo	25 pF 50 pF	1.3/1.21 1.59/1.5	1.97/1.84 2.37/2.24	2.91/2.71 3.48/3.28	ns

3.7 Module Timing and Electrical Parameters

This section contains the timing and electrical parameters for i.MX25 modules.

3.7.1 1-Wire Timing Parameters

Figure 7 shows the reset and presence pulses (RPP) timing for 1-Wire.

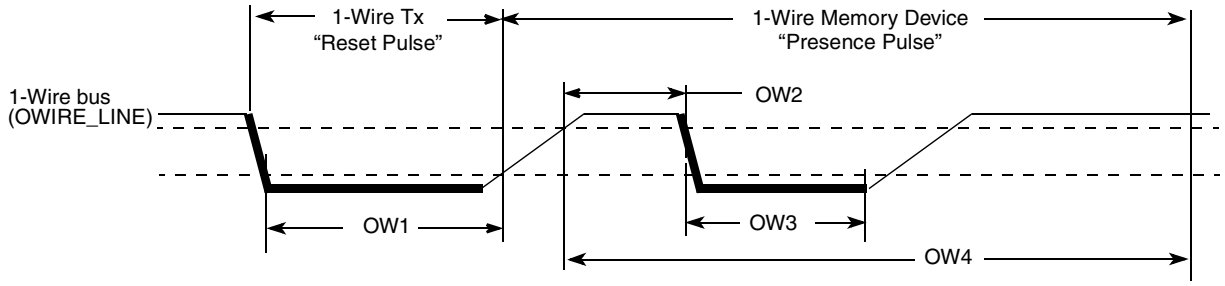

Figure 7. 1-Wire RPP Timing Diagram

Table 32 lists the RPP timing parameters.

Table 32. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min.	Typ.	Max.	Units
OW1	Reset Time Low	t_{RSTL}	480	511	—	µs
OW2	Presence Detect High	t_{PDH}	15	—	60	µs
OW3	Presence Detect Low	t_{PDL}	60	—	240	µs
OW4	Reset Time High	t_{RSTH}	480	512	—	µs

Figure 8 shows write 0 sequence timing, and Table 33 describes the timing parameters (OW5–OW6) that are shown in the figure.

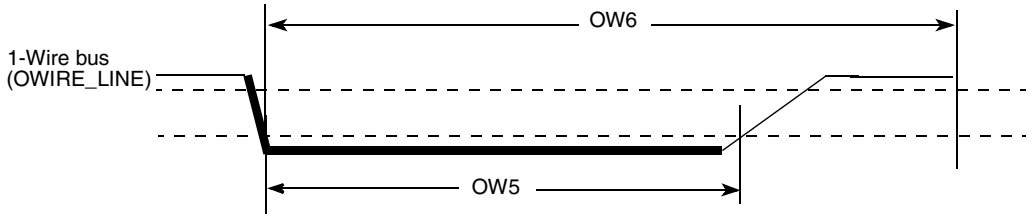

Figure 8. Write 0 Sequence Timing Diagram

Table 33. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW5	Write 0 Low Time	t_{WR0_low}	60	100	120	µs
OW6	Transmission Time Slot	t_{SLOT}	OW5	117	120	µs

3.7.2.1 PIO Mode Timing Parameters

Figure 11 shows a timing diagram for PIO read mode.

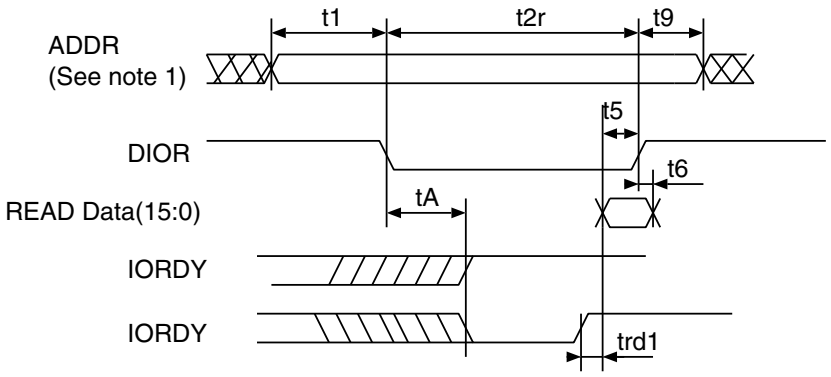

Figure 11. PIO Read Mode Timing

To meet PIO read mode timing requirements, a number of timing parameters must be controlled. Table 36 shows timing parameters and their determining relations, and indicates parameters that can be adjusted to meet required conditions.

Table 36. Timing Parameters for PIO Read Mode

ATA Parameter	PIO Read Mode Timing Parameter[1]	Relation	Adjustable Parameter
t1	t1	t1(min.) = time_1 × T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2r	t2(min.) = time_2r × T – (tskew1 + tskew2 + tskew5)	time_2r
t9	t9	t9(min.) = time_9 × T – (tskew1 + tskew2 + tskew6)	time_9
t5	t5	t5(min.) = tco + tsu + tbuf + tbuf + tcable1 + tcable2	If not met, increase time_2
t6	t6	0	—
tA	tA	tA(min.) = (1.5 + time_ax) × T – (tco + tsui + tcable2 + tcable2 + 2 × tbuf)	time_ax
trd	trd1	trd1(max.) = (–trd) + (tskew3 + tskew4) trd1(min.) = (time_pio_rdx – 0.5) × T – (tsu + thi) (time_pio_rdx – 0.5) × T > tsu + thi + tskew3 + tskew4	time_pio_rdx
t0	—	t0(min.) = (time_1 + time_2 + time_9) × T	time_1, time_2r, time_9

[1] See Figure 11.

To meet timing requirements, a number of timing parameters must be controlled. See Table 38 for details on timing parameters for MDMA read and write modes.

Table 38. Timing Parameters for MDMA Read and Write Modes

ATA Parameter	MDMA Read[1] and Write[2] Timing Parameters	Relation	Adjustable Parameter(s)
tm, ti	tm	tm(min.) = ti(min.) = time_m × T – (tskew1 + tskew2 + tskew5)	time_m
td	td, td1	td1(min.) = td(min.) = time_d × T – (tskew1 + tskew2 + tskew6)	time_d
tk	tk	tk(min.) = time_k × T – (tskew1 + tskew2 + tskew6)	time_k
t0	—	t0(min.) = (time_d + time_k) × T	time_d, time_k
tg(read)	tgr	tgr(min.–read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 tgr(min.–drive) = td – te(drive)	time_d
tf(read)	tfr	tfr(min.–drive) =0 k	—
tg(write)	—	tg(min.–write) = time_d × T –(tskew1 + tskew2 + tskew5)	time_d
tf(write)	—	tf(min.–write) = time_k × T – (tskew1 + tskew2 + tskew6)	time_k
tL	—	tL(max.) = (time_d + time_k–2) × T – (tsu + tco + 2 × tbuf + 2 × tcable2)	time_d, time_k[3]
tn, tj	tkjn	tn= tj= tkjn = (max.(time_k,. time_jn) × T – (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

1 See Figure 13.

2 See Figure 14.

3 tk1 in the UDMA figures equals (tk –2 × T).

3.7.2.3 Ultra DMA (UDMA) Mode Timing

UDMA mode timing is more complicated than PIO mode or MDMA mode. In this section, timing diagrams for UDMA in- and out-transfers are provided.

3.7.4.1 Gated Clock Mode Timing

Figure 20 and Figure 21 shows the gated clock mode timings for CSI, and Table 41 describes the timing parameters (P1–P7) shown in the figures. A frame starts with a rising/falling edge on VSYNC, then HSYNC is asserted and holds for the entire line. The pixel clock is valid as long as HSYNC is asserted.

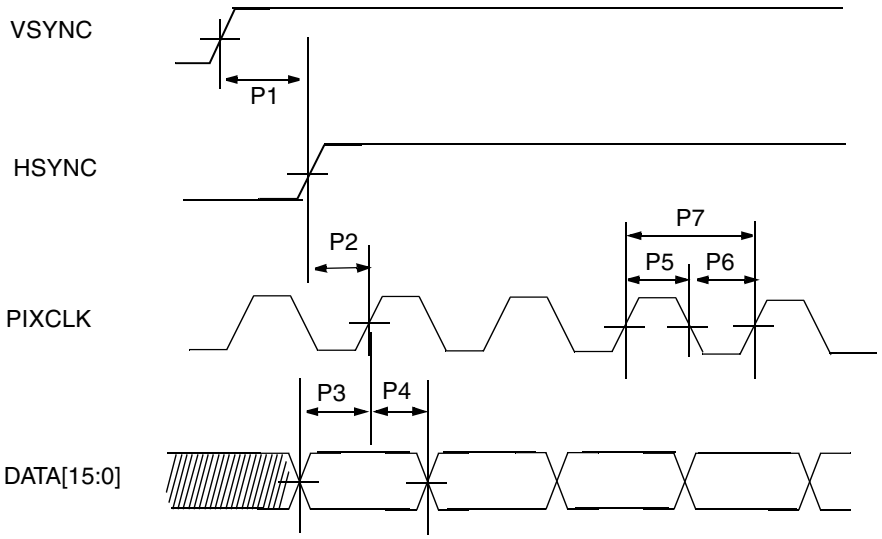

Figure 20. CSI Gated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

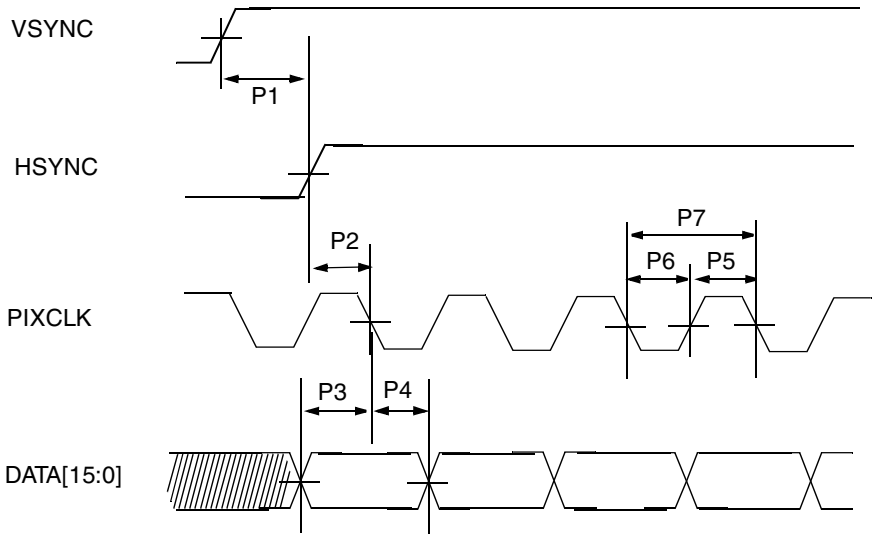

Figure 21. CSI Gated Clock Mode—Sensor Data at Rising Edge, Latch Data at Falling Edge

3.7.6.1 ESDCTL Electrical Specifications

3.7.6.1.1 SDRAM Memory Controller

The following diagrams and tables specify the timings related to the SDRAMC module which interfaces SDRAM.

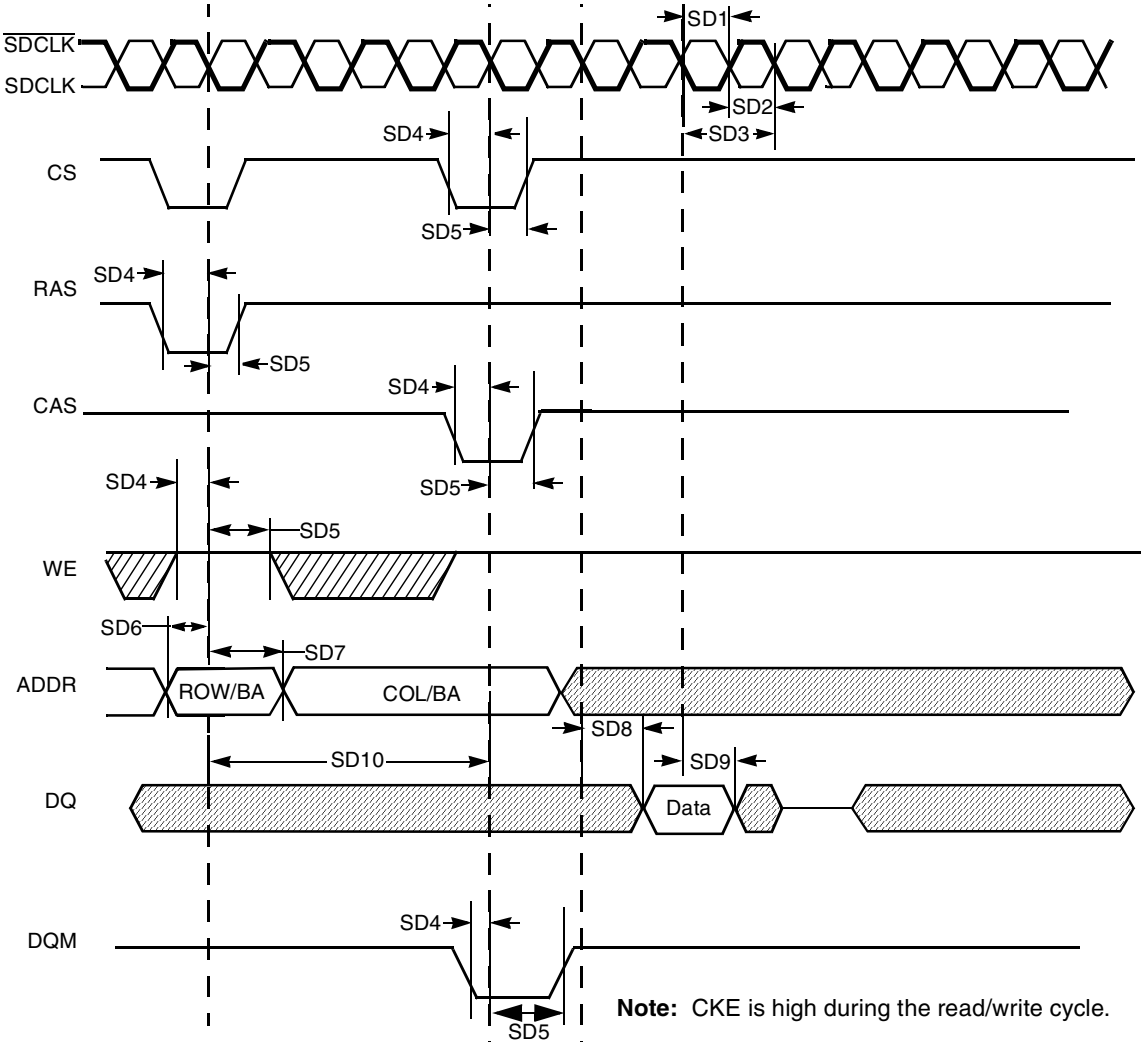

Figure 25. SDRAM Read Cycle Timing Diagram

Table 44. DDR/SDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width[1]	tCH	3.4	4.1	ns
SD2	SDRAM clock low-level width[1]	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD4	CS, RAS, CAS, WE, DQM, CKE setup time	tCMS	2.0	—	ns
SD5	CS, RAS, CAS, WE, DQM, CKE hold time	tCMH	1.8	—	ns

Table 47. SDRAM Self-Refresh Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD16	CKE output delay time	tCKS	1.8	—	ns

3.7.6.1.2 Mobile DDR SDRAM–Specific Parameters

The following diagrams and tables specify the timings related to the SDRAMC module which interfaces with the mobile DDR SDRAM.

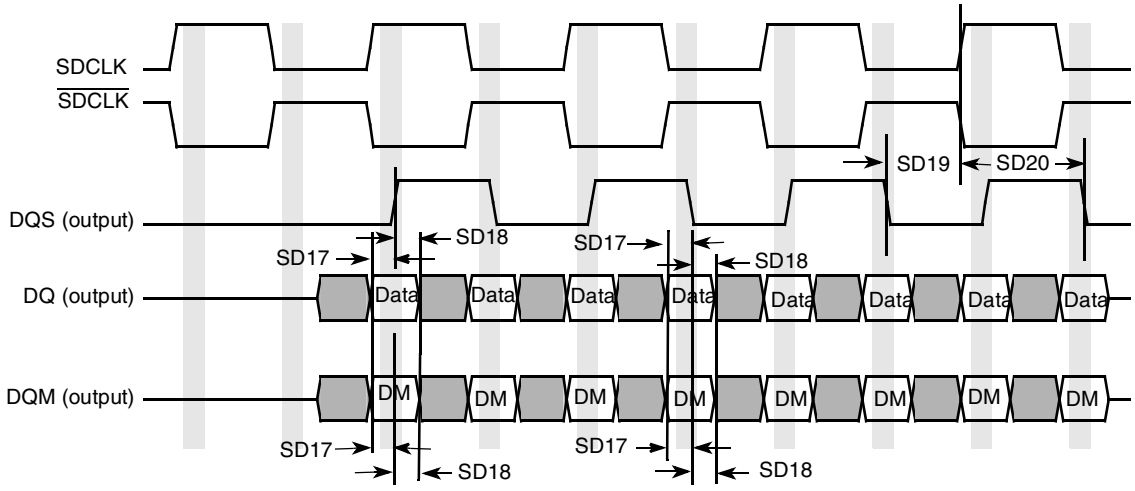

Figure 29. Mobile DDR SDRAM Write Cycle Timing Diagram

Table 48. Mobile DDR SDRAM Write Cycle Timing Parameters[1]

ID	Parameter	Symbol	Min.	Max.	Unit
SD17	DQ and DQM setup time to DQS	tDS	0.95	—	ns
SD18	DQ and DQM hold time to DQS	tDH	0.95	—	ns
SD19	Write cycle DQS falling edge to SDCLK output delay time	tDSS	1.8	—	ns
SD20	Write cycle DQS falling edge to SDCLK output hold time	tDSH	1.8	—	ns

[1] Test condition: Measured using delay line 5 programmed as follows: ESDCDLY5[15:0] = 0x0703.

3.7.6.1.3 DDR2 SDRAM–Specific Parameters

The following diagrams and tables specify timing related to the SDRAMC module, which interfaces with DDR2 SDRAM.

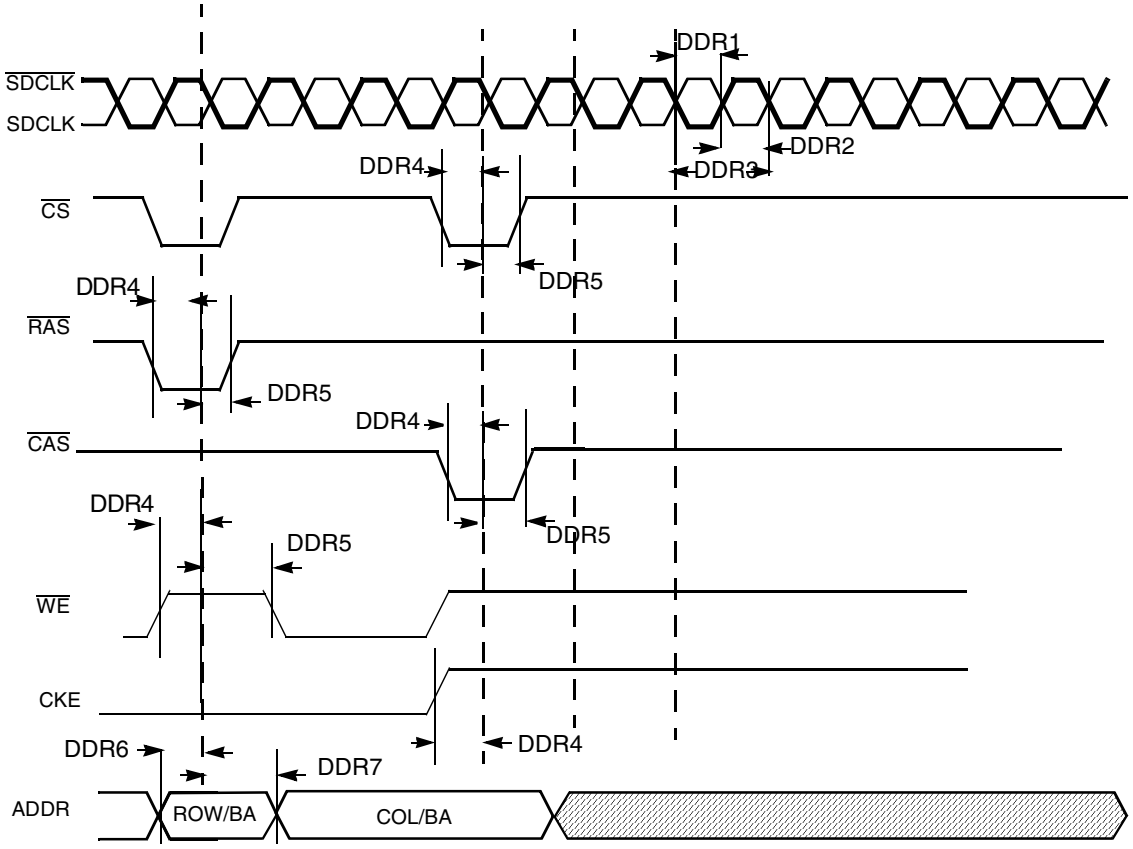

Figure 31. DDR2 SDRAM Basic Timing Parameters

Table 50 provides values for a command/address slew rate of 1 V/ns and an SDCLK, SDCLK_B differential slew rate of 2 V/ns. For additional values, use Table 51, “tlS, tlH Derating Values for DDR2-400, DDR2-533.”

Table 50. DDR2 SDRAM Timing Parameter Table

ID	Parameter	Symbol	DDR2-400		Unit
			Min.	Max.	
DDR1	SDRAM clock high-level width	t_{CH}	0.45	0.55	t_{CK}
DDR2	SDRAM clock low-level width	t_{CL}	0.45	0.55	t_{CK}
DDR3	SDRAM clock cycle time	t_{CK}	7.5	8	ns

3.7.9.1.5 MII Transmit Signal Timing (FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER, and FEC_TX_CLK)

The transmitter functions correctly up to an FEC_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the FEC_TX_CLK frequency.

Figure 56 shows MII transmit signal timings. Table 63 describes the timing parameters (M5–M8) shown in the figure.

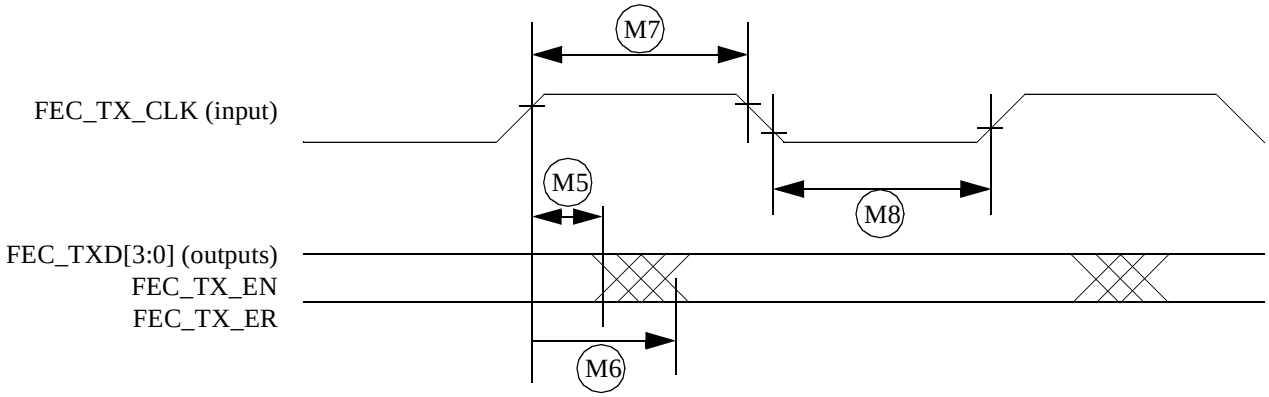

Figure 56. MII Transmit Signal Timing Diagram

Table 63. MII Transmit Signal Timing

ID	Characteristic[1]	Min.	Max.	Unit
M5	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER invalid	5	—	ns
M6	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER valid	—	20	ns
M7	FEC_TX_CLK pulse width high	35%	65%	FEC_TX_CLK period
M8	FEC_TX_CLK pulse width low	35%	65%	FEC_TX_CLK period

[1] FEC_TX_EN, FEC_TX_CLK, and FEC_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

3.7.9.1.6 MII Asynchronous Inputs Signal Timing (FEC_CRS and FEC_COL)

Figure 57 shows MII asynchronous input timings. Table 64 describes the timing parameter (M9) shown in the figure.

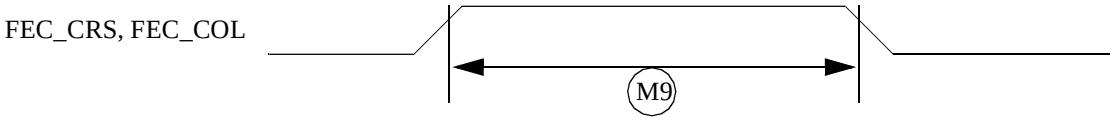

Figure 57. MII Async Inputs Timing Diagram

Table 64. MII Asynchronous Inputs Signal Timing

ID	Characteristic	Min.	Max.	Unit
M9[1]	FEC_CRS to FEC_COL minimum pulse width	1.5	—	FEC_TX_CLK period

[1] FEC_COL has the same timing in 10-Mbit 7-wire interface mode.

3.7.9.2 MII Serial Management Channel Timing (FEC_MDIO and FEC_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to comply with the IEEE 802.3 standard MII specification. However the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Figure 58 shows MII asynchronous input timings. Table 65 describes the timing parameters (M10—M15) shown in the figure.

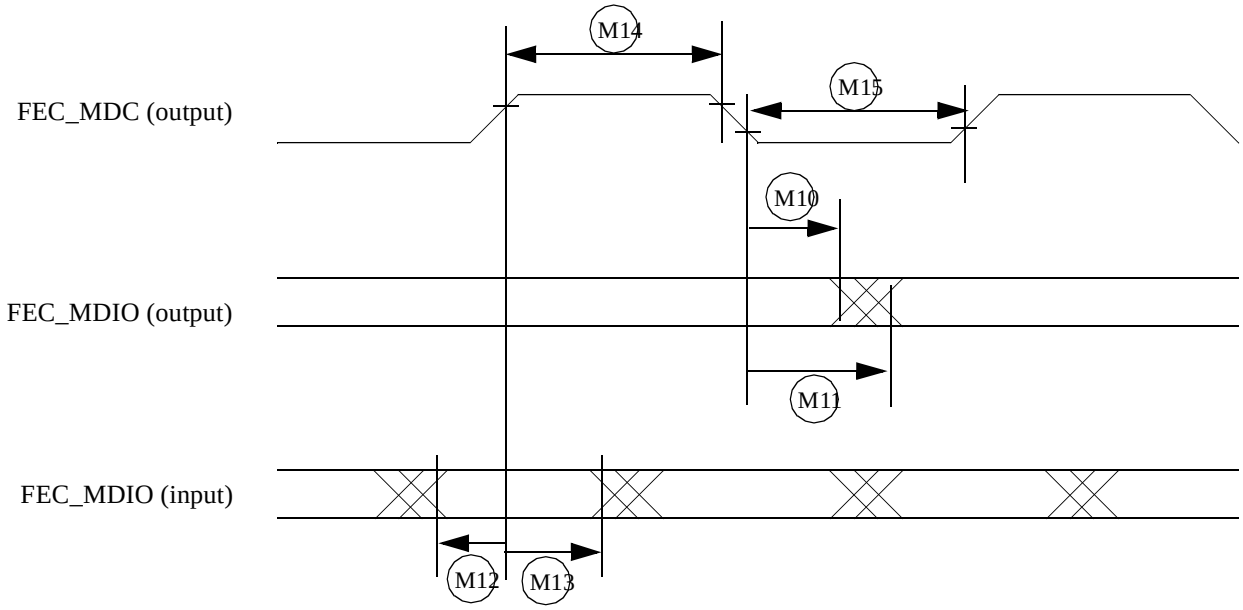

Figure 58. MII Serial Management Channel Timing Diagram

Table 65. MII Serial Management Channel Timing

ID	Characteristic	Min.	Max.	Unit
M10	FEC_MDC falling edge to FEC_MDIO output invalid (min. propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max. propagation delay)	—	5	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	18	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

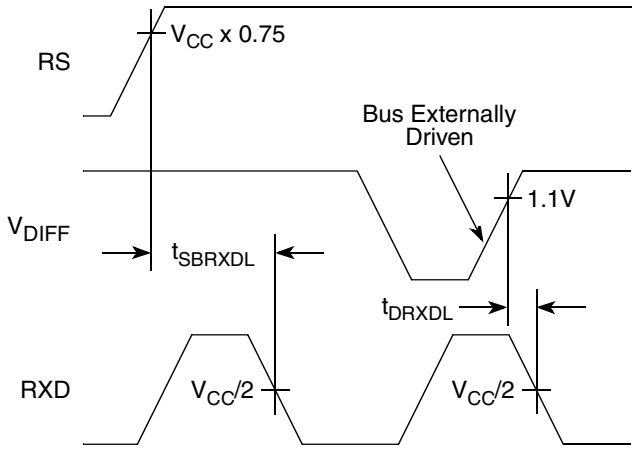

Figure 61. Timing Diagram for FlexCAN Standby Signal

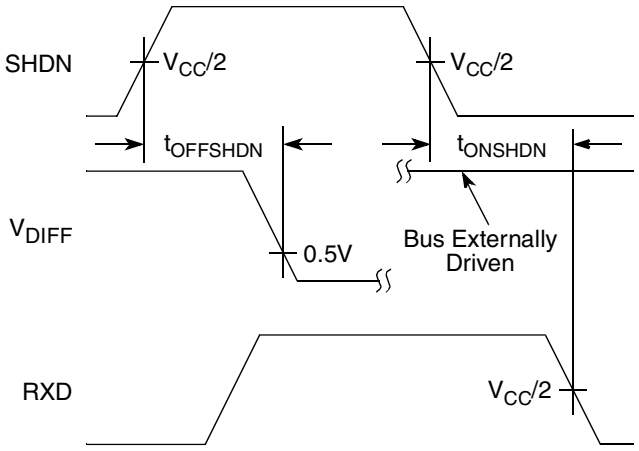

Figure 62. Timing Diagram for FlexCAN Shutdown Signal

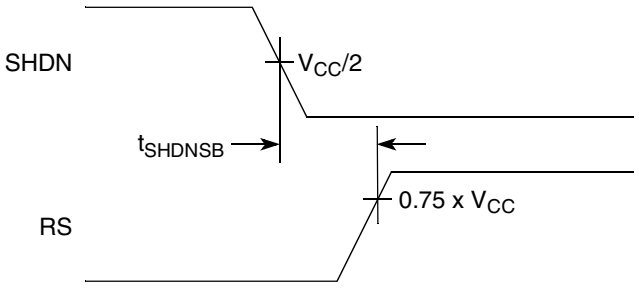

Figure 63. Timing Diagram for FlexCAN Shutdown-to-Standby Signal

Because integer multiples are not possible, taking into account the range of frequencies at which the SoC has to operate, DPLLs work in FOL mode only.

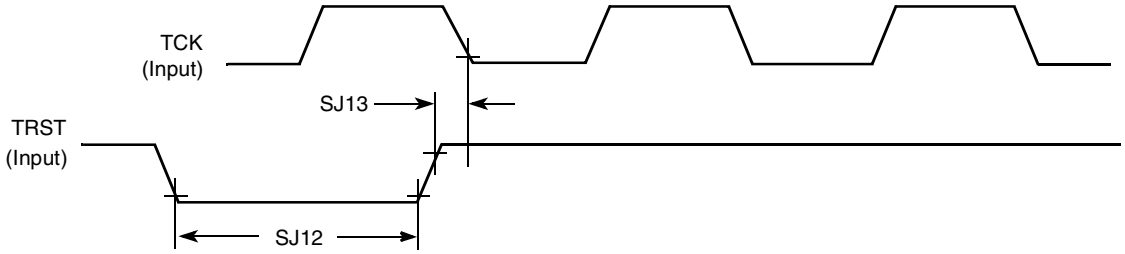

Figure 75. $\overline{\text{TRST}}$ Timing Diagram

Table 78. SJC Timing Parameters

ID	Parameter	All Frequencies		Unit
		Min.	Max.	
SJ1	TCK cycle time	100[1]	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	40	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	10	—	ns
SJ5	Boundary scan input data hold time	50	—	ns
SJ6	TCK low to output data valid	—	50	ns
SJ7	TCK low to output high impedance	—	50	ns
SJ8	TMS, TDI data set-up time	10	—	ns
SJ9	TMS, TDI data hold time	50	—	ns
SJ10	TCK low to TDO data valid	—	44	ns
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

1 In cases where SDMA TAP is put in the chain, the maximum TCK frequency is limited by the maximum ratio of 1:8 of SDMA core frequency to TCK. This implies a maximum frequency of 8.25 MHz (or 121.2 ns) for a 66 MHz IPG clock.

2 $V_{M\ -}$ mid point voltage

Table 97 shows the timing specifications for USB in VP_VM unidirectional mode.

Table 97. USB Timing Specifications in VP_VM Unidirectional Mode

No.	Parameter	Signal	Direction	Min.	Max.	Unit	Conditions/ Reference Signal
US30	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US31	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US32	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US33	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US34	Tx high overlap	USB_SE0_VM	Out	0.0	—	ns	USB_DAT_VP
US35	Tx low overlap	USB_SE0_VM	Out	—	0.0	ns	USB_DAT_VP
US36	Enable delay	USB_DAT_VP USB_SE0_VM	In	—	8.0	ns	USB_TXOE_B
US37	Disable delay	USB_DAT_VP USB_SE0_VM	In	—	10.0	ns	USB_TXOE_B
US38	Rx rise/fall time	USB_VP1	In	—	3.0	ns	35 pF
US39	Rx rise/fall time	USB_VM1	In	—	3.0	ns	35 pF
US40	Rx skew	USB_VP1	Out	–4.0	+4.0	ns	USB_SE0_VM
US41	Rx skew	USB_RCV	Out	–6.0	+2.0	ns	USB_DAT_VP

3.7.20.2 USB Parallel Interface Timing

Table 98 defines the USB parallel interface signals.

Table 98. Signal Definitions for USB Parallel Interface

Name	Direction	Signal Description
USB_Clk	In	Interface clock—All interface signals are synchronous to USB_Clk
USB_Data[7:0]	I/O	Bidirectional data bus, driven low by the link during idle—Bus ownership is determined by the direction
USB_Dir	In	Direction—Control the direction of the data bus
USB_Stp	Out	Stop—The link asserts this signal for one clock cycle to stop the data stream currently on the bus
USB_Nxt	In	Next—The PHY asserts this signal to throttle the data

Table 103. i.MX25 17×17 Package Ball Map (continued)

	T	R	P	N	M	L	K
1	UART2_TXD	KPP_ROW1	KPP_COL0	KPP_COL3	FEC_RDATA0	FEC_MDC	QGND
2	UART1_CTS	UART2_CTS	KPP_ROW3	KPP_COL2	FEC_TX_EN	FEC_MDIO	QGND
3	UART1_RTS	UART2_RTS	KPP_ROW2	KPP_COL1	FEC_RX_DV	FEC_TDATA0	QGND
4	CSPI1_MOSI	CSPI1_SS0	UART2_RXD	KPP_ROW0	FEC_RDATA1	FEC_TX_CLK	QGND
5	QGND	QGND	QGND	NVCC_MISC	QVDD	QGND	QGND
6	QGND	NVCC_LCDC	NVCC_LCDC	NVCC_MISC	QVDD	NVCC_NFC	QVDD
7	QGND	NVCC_LCDC	NVCC_LCDC	NVCC_MISC	QVDD	NVCC_NFC	QVDD
8	QGND	QGND	QVDD	QVDD	QGND	NVCC_NFC	QGND
9	QGND	QGND	QVDD	QGND	QGND	QGND	QGND
10	QGND	QGND	BAT_VDD	TAMPER_A	QGND	QGND	QGND
11	QGND	QGND	MESH_C	TAMPER_B	QGND	QGND	QGND
12	QGND	QGND	MESH_D	QGND	QGND	QGND	QVDD
13	QGND	QGND	QGND	QGND	QGND	QGND	QGND
14	QGND	QGND	QGND	NVCC_CRM	QGND	QGND	QGND
15	QGND	QGND	QGND	QGND	QGND	QGND	QGND
16	QGND	QGND	QGND	QGND	UPLL_GND	UPLL_VDD	USBPHY1_VDDA
17	FUSE_VDD	NVCC_SDIO	GPIO_C	USBPHY1_UPLLVSS	USBPHY1_UPLLVDD	USBPHY1_RREF	USBPHY1_VBUS
18	RESET_B	VSTBY_REQ	GPIO_E	GPIO_B	NC_BGA_M18	USBPHY1_DP	USBPHY1_DM
19	POWER_FAIL	GPIO_F	GPIO_D	GPIO_A	SD1_DATA2	USBPHY1_VSSA	USBPHY1_VDDA_BIAS
20	VSTBY_ACK	EXT_ARMCLK	NC_BGA_P20	SD1_DATA1	SD1_CLK	SD1_DATA0	SD1_CMD

Table 105. 12x12 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
WIPER	AA17	ADC	ANALOG	ANALOG	-
INAUX0	AA15	ADC	ANALOG	ANALOG	-
INAUX1	W14	ADC	ANALOG	ANALOG	-
INAUX2	AB16	ADC	ANALOG	ANALOG	-

1 The state immediately after reset and before ROM firmware or software has executed.

2 During power-on reset this port acts as input for fuse override signal.

3 During power-on reset this port acts as output for diagnostic signal.

Table 106 lists the 12×12 mm package i.MX25 no connect contact assignments.

Table 106. 12×12 mm Package i.MX25 No Connect Contact Assignments

Signal Name	Contact Assignment
NC_BGA_E4	E4
NC_BGA_L4	L4

4.8 i.MX25 12x12 Package Ball Map

Table 107 shows the i.MX25 12×12 package ball map.

Table 107. i.MX25 12×12 Package Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	QGND	EB0	OE	A14	A16	A18	A22	BCLK	DQM1	SD9	SD10	SD7	SD0	SD3	SD5	SDCKE0	SDBA0	CS3	A1	A0	A4	QGND
B	ECB	QGND	LBA	EB1	A10	A20	A24	SD14	SD12	SD11	SD6	SD2	SD4	QGND	SDWE	CAS	CS2	A2	A5	A7	QGND	A12
C	NFRE_B	CS0																			A11	CS1_D2
D	NFCLE	CS5		CS1	RW	A15	A21	A25	SD15	SD8	DQM0	SD1	SDCLK	SDCLK_B	RAS	SDBA1	A3	A6	A9		A13	CSI_D6
E	NFWE_B	NFALE		NC_BGA_E4	CS4	A17	A19		A23		SD13	SDQS1		SDQS0	NVCC_EMI2		MA10	QGND	A8		CSI_D4	CSI_D8
F	D1	D0		NF_CE0									QGND	QGND	NVCC_EMI2	SDCKE1		QGND	CSI_D3		CSI_D7	CSI_MCLK