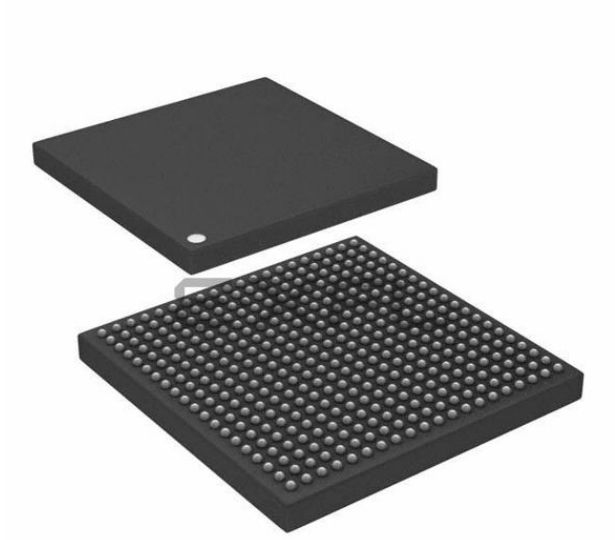

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx257cjm4a

1.2 Block Diagram

Figure 1 shows the simplified interface block diagram.

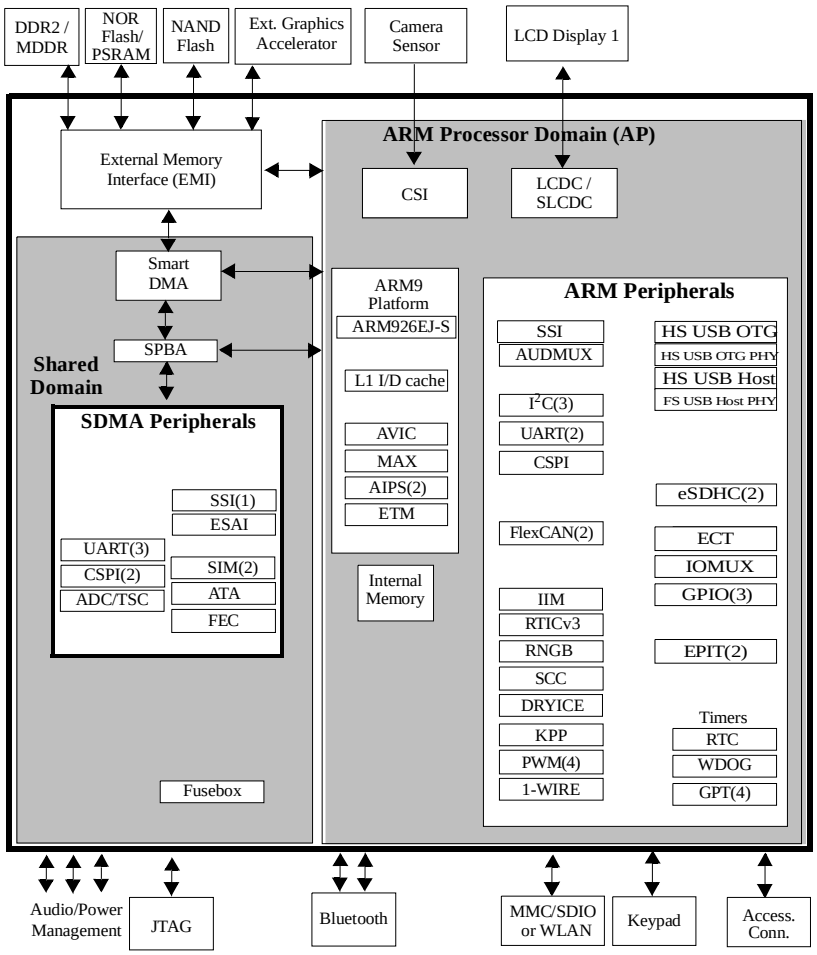

Figure 1. i.MX25 Simplified Interface Block Diagram

Table 3. i.MX25 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
EPIT(2)	Enhanced periodic interrupt timer	Timer peripherals	Each Enhanced Periodic Interrupt Timer (EPIT) is a 32-bit set-and-forget timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler to adjust the input clock frequency to the required time setting for the interrupts, and the counter value can be programmed on the fly.
ESAI	Enhanced serial audio interface	Connectivity peripherals	ESAI provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other DSPs. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator.
eSDHC(2)	Enhanced multimedia card/ secure digital host controller	Connectivity peripherals	The features of the eSDHC module, when serving as host, include the following: • Conforms to the SD host controller standard specification version 2.0 • Compatible with the JEDEC MMC system specification version 4.2 • Compatible with the SD memory card specification version 2.0 • Compatible with the SDIO specification version 1.2 • Designed to work with SD memory, miniSD memory, SDIO, miniSDIO, SD combo, MMC and MMC RS cards • Configurable to work in one of the following modes: —SD/SDIO 1-bit, 4-bit —MMC 1-bit, 4-bit, 8-bit • Full-/high-speed mode • Host clock frequency variable between 32 kHz and 52 MHz • Up to 200-Mbps data transfer for SD/SDIO cards using four parallel data lines • Up to 416-Mbps data transfer for MMC cards using eight parallel data lines
FEC	Fast ethernet controller	Connectivity peripherals	The Ethernet Media Access Controller (MAC) is designed to support both 10- and 100-Mbps Ethernet networks compliant with IEEE 802.3® standard. An external transceiver interface and transceiver function are required to complete the interface to the media
FlexCAN(2)	Controller area network module	Connectivity peripherals	The Controller Area Network (CAN) protocol is primarily designed to be used as a vehicle serial data bus running at 1 MBps.
GPIO(4)	General purpose I/O modules	System control peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPT(4)	General purpose timers	Timer peripherals	Each GPT is a 32-bit free-running or set-and-forget mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in set-and-forget mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.

Table 4. Signal Considerations (continued)

Signal	Description
MESH_C, MESH_D	Wire-mesh tamper detect pins that can be routed at the PCB board to detect attempted tampering of a protected wire. When security measures are implemented, MESH_C should be pulled-up or connected to NVCC_DRYICE and triggers a tamper event when floating or when connected to MESH_D. MESH_D should be pulled-down or connected to GND and triggers an event when floating or connected to MESH_C. These pins can be left unconnected if the DryIce security features are not being used.
NVCC_DRYICE	This is the DryIce power supply output. The supply source is QVDD when the i.MX25 is in run mode. When i.MX25 is in reduced power mode, the DryIce supply source is the BATT_VDD supply. This pin can be used to power external DryIce components (external tamper detect, wire-mesh tamper detect). In order to guarantee the power-loss protection feature which guarantees that RTC and/or secure keys be maintained after power-off an external capacitor no less than 4 µF must be connected to this supply output pin. A 4.7 µF capacitor is recommended.
OSC_BYP	The 32 kHz oscillator bypass-control pin. If this signal is pulled down, then OSC32K_EXTAL and OSC32K_XTAL analog pins should be tied to the external 32.768 kHz crystal circuit. If on the other hand the signal is pulled up, then the external 32 kHz oscillator output clock must be connected to OSC32K_EXTAL analog pin, and OSC32K_XTAL can be no connect (NC).
OSC32K_EXTAL OSC32K_XTAL	These analog pins are connected to an external 32 kHz CLK circuit depending on the state of OSC_BYP pin (see the description of OSC_BYP under the preceding bullet). The 32 kHz reference CLK is required for normal operation.
POWER_FAIL	An interrupt from PMIC, which should be connected to a low-battery detection circuit. This signal is internally connected to an on-chip 100 kΩ pull-down device. If there is no low-battery detection, then users can tie this pin to GND through a pull-down resistor, or leave the signal as NC. This pin can also be configured to work as a normal GPIO.
REF	External ADC reference voltage. REF may be tied to GND if the user plans to only use the internally generated 2.5 V reference supply.
SJC_MOD	Must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed, but the value should be much smaller than the on-chip 100 kΩ pull-up.
TAMPER_A, TAMPER _B	DryIce external tamper detect pins, active high. If TAMPER_A or TAMPER_B is connected to NVCC_DRYICE, then external tampering is detected. These pins can be left unconnected if the DryIce security features are not being used.
TEST_MODE	For Freescale factory use only. This signal is internally connected to an on-chip pull-down device. Users must either float this signal or tie it to GND.
UPLL_BYPCLK	Primarily for Freescale factory use. There is no internal on-chip pull-up/down on this pin, so it must be externally connected to GND or VDD. Aside from factory use, this pin can also be configured (through muxing) to work as a normal GPIO.
USBPHY1_RREF	Determines the reference current for the USB PHY1 bandgap reference. An external 10 kΩ 1% resistor to GND is required.
USBPHY2_DM USBPHY2_DP	The output impedance of these signals is expected at 10 Ω. It is recommended to also have on-board 33 Ω series resistors (close to the pins).

[1] Sleep mode differs from stop mode in that the core voltage is reduced to 1 V.

Table 13 shows typical current consumption for the various power supplies under the various power modes.

Table 13. i.MX25 Power Mode Current Consumption

Power Group	Power Supplies	Voltage Setting	Current Consumption for Power Modes[1]			
			Doze	Wait	Stop	Sleep
NVCC_EMI	NVCC_EMI1 NVCC_EMI2	3.0 V	5 µA	3.15 µA	3.51 µA	3.61 µA
NVCC_CRM	NVCC_CRM	3.0 V	1.15 µA	4.31 µA	0.267 µA	0.32 µA
NVCC_ OTHER	NVCC_SDIO NVCC_CSI NVCC_NFC NVCC_JTAG NVCC_LCDC NVCC_MISC	3.0 V	31.2 µA	29.5 µA	31.7 µA	32.1 µA
NVCC_ADC	NVCC_ADC	3.0 V	163 µA	3.25 µA	1.14 µA	0.871 µA
OSC24M	OSC24M_ VDD	3.0 V	906 µA	903 µA	10.2 µA mA	10.5 µA
PLL_VDD	MPLL_VDD UPLL_VDD	1.4 V	6.83 mA	6.83 mA	38.9 µA	39.1 µA
QVDD	QVDD	1.15 V	8.79 mA	11.28 mA	842 µA	665 µA
USBPHY1_ VDDA	USBPHY1_ VDDA	3.17 V	240 µA	240 µA	241 µA	242 µA
USBPHY1_ VDDA_VBIAS	USBPHY1_ VDDA_VBIAS	3.17 V	0.6 µA	1.46 µA	0.328 µA	0.231 µA
USBPHY1_ UPLL_VDD	USBPHY1_ UPLL_VDD	3.17 V	201 µA	201 µA	191 µA	191 µA
USBPHY2	USBPHY2_ VDD	3.0 V	158 µA	0158 µA	164 µA	164 µA

[1] Values are typical, under typical use conditions.

In the reduced power mode, shown in Table 14, the i.MX25 is powered down, while the RTC clock and the secure keys (in secure-use case), remain operational. BAT_VDD is tied to a battery while all other supplies are turned off.

NOTE

In this low-power mode, i.MX25 cannot be woken up with an interrupt; it must be powered back up before it can detect any events.

NOTE

This is to guarantee that POR is stable already at NVCC_CRM/QVDD power domain interface before QVDD is turned on, and POR instantly propagates to QVDD domain after QVDD is turned on.

4. Turn on other NVCCx digital I/O power supplies for not less than 1 ms and not more than 32 ms, after QVDD reaches 90% of 1.2 V.
5. Turn on all other analog power supplies, including USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD, USBPHY1_VDDA, USBPHY2_VDD, NVCC_ADC, OSC24M_VDD, MPPLL_VDD, UPLL_VDD, and FUSEVDD (FUSEVDD is tied to GND if fuses are not programmed) for not less than 1 ms and not more than 32 ms, after NVCCx reaches 90% of 3.3 V.

NOTE

This is to guarantee that analog peripherals can get properly initialized (reset) values from QVDD domain and NVCCx domain.

6. Negate the POR signal for at least 90 µs after all previous steps.

NOTE

- This is to guarantee that both POR logic and clocks are stable inside the i.MX25 chip, before POR is removed.
- The dV/dT should be no faster than 0.25 V/us for all power supplies, to avoid triggering ESD circuit.

In addition, the following power-down sequence is recommended:

1. Turn off power for analog parts, including USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD, USBPHY1_VDDA, USBPHY2_VDD, NVCC_ADC, and FUSEVDD (FUSEVDD is tied to GND if fuses are not programmed).
2. Turn off QVDD.
3. Turn off NVCCx, PLL, OSC, and other powers.

NOTE

The power-down steps can be executed simultaneously, or very shortly one after another.

3.3 Power Characteristics

Table 15 shows values representing maximum current numbers for the i.MX25 under worst case voltage and temperature conditions. These values are derived from the i.MX25 with core clock speed up to 400 MHz. Additionally, no power saving techniques such as clock gating were implemented when measuring these values. Common supplies are bundled according to the i.MX25 power-up sequence requirements. Peak numbers are provided for system designers so that the i.MX25 power supply requirements are satisfied during startup and transient conditions. Freescale recommends that system

Figure 12 gives timing waveforms for PIO write mode.

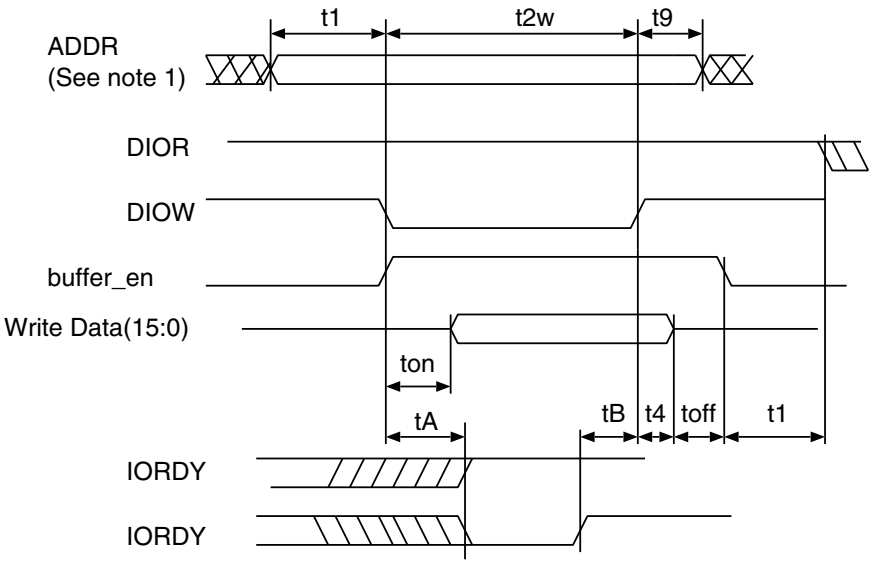

Figure 12. PIO Write Mode Timing

To meet PIO write mode timing requirements, a number of timing parameters must be controlled. Table 37 shows timing parameters and their determining relations, and indicates parameters that can be adjusted to meet required conditions.

Table 37. Timing Parameters for PIO Write Mode

ATA Parameter	PIO Write Mode Timing Parameter[1]	Relation	Adjustable Parameter(s)
t1	t1	t1(min.) = time_1 × T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2w	t2(min.) = time_2w × T – (tskew1 + tskew2 + tskew5)	time_2w
t9	t9	t9(min.) = time_9 × T – (tskew1 + tskew2 + tskew6)	time_9
t3	—	t3(min.) = (time_2w – time_on) × T – (tskew1 + tskew2 +tskew5)	if not met, increase time_2w
t4	t4	t4(min.) = time_4 × T – tskew1	time_4
tA	tA	tA = (1.5 + time_ax) × T – (tco + tsui + tcable2 + tcable2 + 2 × tbuf)	time_ax
t0	—	t0(min.) = (time_1 + time_2 + time_9) × T	time_1, time_2r, time_9
—	—	Avoid bus contention when switching buffer on by making ton long enough	—
—	—	Avoid bus contention when switching buffer off by making toff long enough	—

[1] See Figure 12.

Figure 17 shows timing for device-terminated UDMA in-transfer.

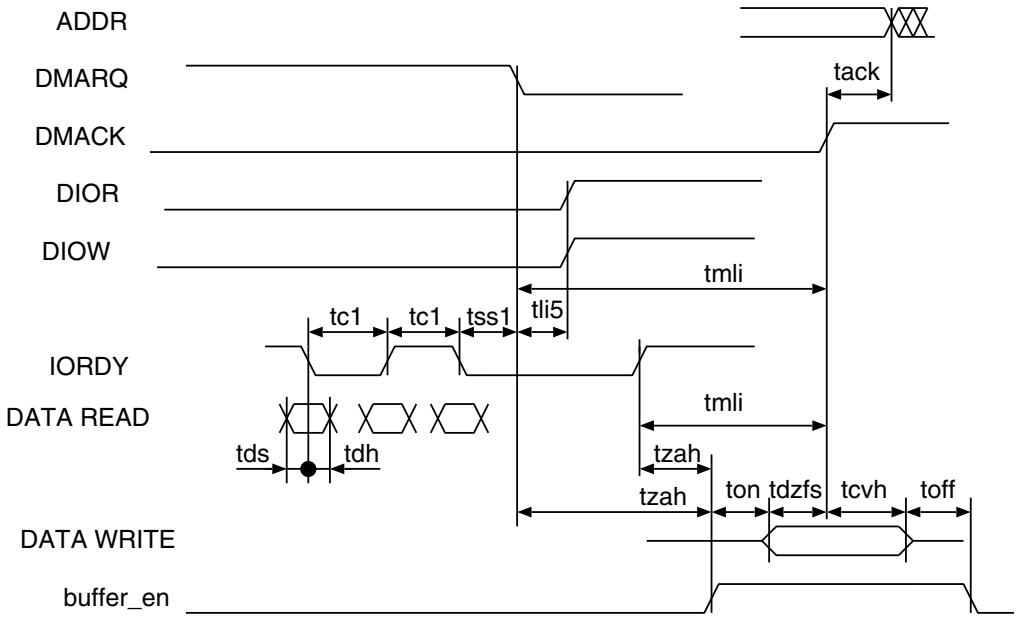

Figure 17. Timing for Device-Terminated UDMA Transfer

Timing parameters for UDMA in-burst are listed in Table 39.

Table 39. Timing Parameters for UDMA In-Burst

ATA Parameter	Spec. Parameter	Value	Required Conditions
tack	tack	tack(min.) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv(min.) = (time_env × T) – (tskew1 + tskew2) tenv(max.) = (time_env × T) + (tskew1 + tskew2)	time_env
tds	tds1	tds – (tskew3) – ti_ds > 0	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	tdh – (tskew3) –ti_dh > 0	
tcyc	tc1	(tcyc – tskew) > T	T big enough
trp	trp	trp(min.) = time_rp × T – (tskew1 + tskew2 + tskew6)	time_rp
—	tx1[1]	(time_rp × T) – (tco + tsu + 3T + 2 × tbuf + 2 × tcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1(min.) = (time_mlix + 0.4) × T	time_mlix
tzah	tzah	tzah(min.) = (time_zah + 0.4) × T	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs × T) – (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh × T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

[1] There is a special timing requirement in the ATA host that requires the internal DIOW to go only high three clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

Make t_{on} and t_{off} big enough to avoid bus contention.

3.7.6.1 ESDCTL Electrical Specifications

3.7.6.1.1 SDRAM Memory Controller

The following diagrams and tables specify the timings related to the SDRAMC module which interfaces SDRAM.

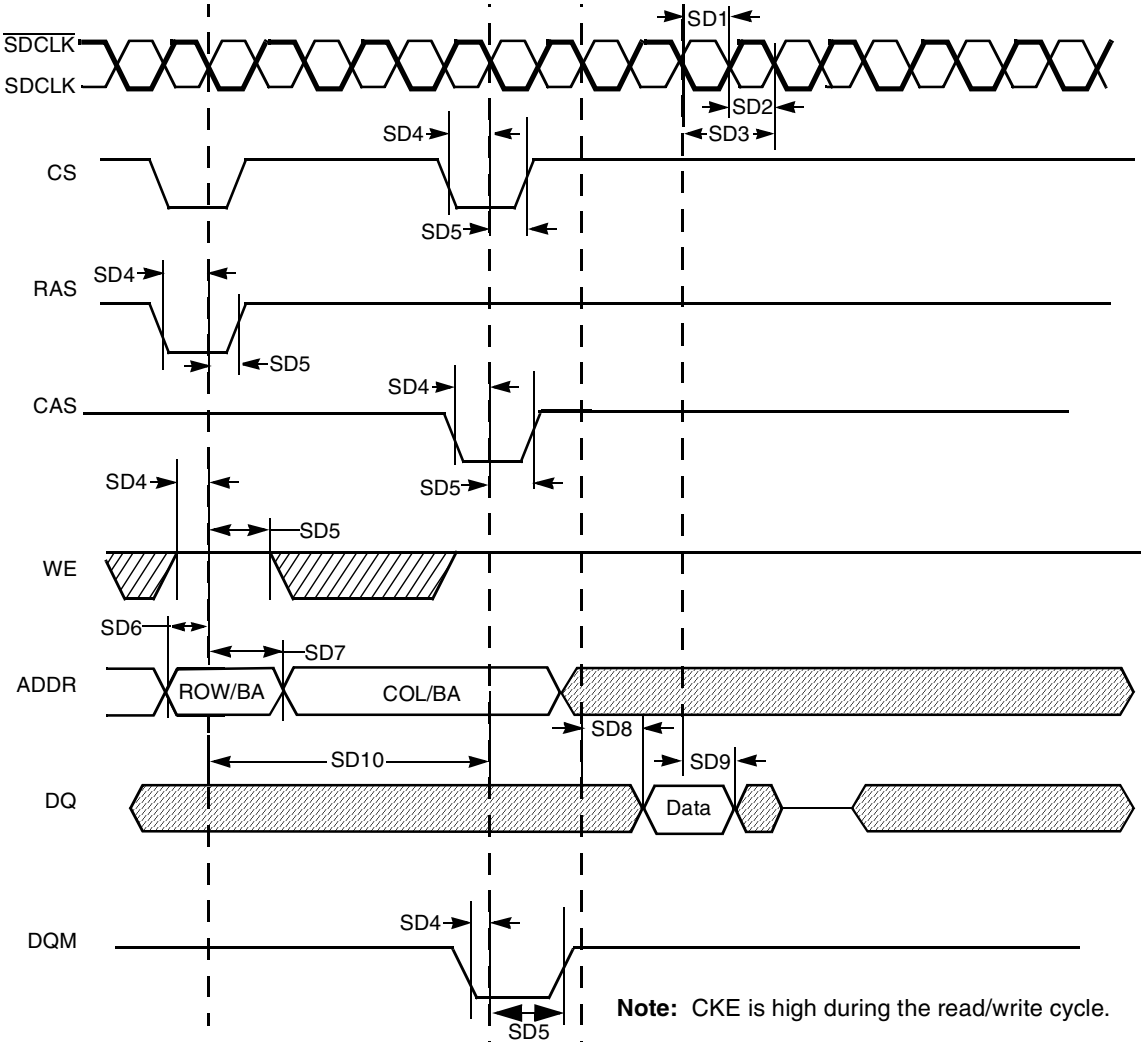

Figure 25. SDRAM Read Cycle Timing Diagram

Table 44. DDR/SDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width[1]	tCH	3.4	4.1	ns
SD2	SDRAM clock low-level width[1]	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD4	CS, RAS, CAS, WE, DQM, CKE setup time	tCMS	2.0	—	ns
SD5	CS, RAS, CAS, WE, DQM, CKE hold time	tCMH	1.8	—	ns

Table 50. DDR2 SDRAM Timing Parameter Table (continued)

ID	Parameter	Symbol	DDR2-400		Unit
			Min.	Max.	
DDR4	CS, RAS, CAS, CKE, WE setup time	t_{IS}	1.2	—	ns
DDR5	CS, RAS, CAS, CKE, WE hold time	t_{IH}	1.2	—	ns
DDR6	Address output setup time	t_{IS}	1.2	—	ns
DDR7	Address output hold time	t_{IH}	0.475	—	ns

Table 50 shows values for a command/address slew rate of 1 V/ns and an SDCLK, SDCLK_B differential slew rate of 2 V/ns. Table 51 shows additional values for DDR2-400 and DDR2-533.

Table 51. tIS, tIH Derating Values for DDR2-400, DDR2-533

Command/ Address Slew Rate (V/Ns)	CK, CK Differential Slew Rate						Units
	2.0 V/ns		1.5 V/ns		1.0 V/ns		
	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	
4.0	+187	+94	+217	+124	+247	+154	ps
3.5	+179	+89	+209	+119	+239	+149	ps
3.0	+167	+83	+197	+113	+227	+143	ps
2.5	+150	+75	+180	+105	+210	+135	ps
2.0	+125	+45	+155	+75	+185	+105	ps
1.5	+83	+21	+113	+51	+143	+81	ps
1.0	0	0	+30	+30	+60	+60	ps
0.9	–11	–14	+19	+16	+49	+46	ps
0.8	–25	–31	+5	–1	+35	+29	ps
0.7	–43	–54	–13	–24	+17	+6	ps
0.6	–67	–83	–37	–53	–7	–23	ps
0.5	–110	–125	–80	–95	–50	–65	ps
0.4	–175	–188	–145	–158	–115	–128	ps
0.3	–285	–292	–255	–262	–225	–232	ps
0.25	–350	–375	–320	–345	–290	–315	ps
0.2	–525	–500	–495	–470	–465	–440	ps
0.15	–800	–708	–770	–678	–740	–648	ps
0.1	–1450	–1125	–1420	–1095	–1390	–1065	ps

Table 53. ΔtDS1, ΔtDH1 Derating Values for DDR2-400, DDR2-533[1,2,3] (continued)

		DQS Single-Ended Slew Rate																	
DQ Slew Rate V/ns	2.0	188	188	167	146	125	63	—	—	—	—	—	—	—	—	—	—	—	—
	1.5	146	167	125	125	83	42	81	43	—	—	—	—	—	—	—	—	—	—
	1.0	63	125	42	83	0	0	–2	1	–7	–13	—	—	—	—	—	—	—	—
	0.9	—	—	31	69	–11	–14	–13	–13	–18	–27	–29	–45	—	—	—	—	—	—
	0.8	—	—	—	—	–25	–31	–27	–30	–32	–44	–43	–62	–60	–86	—	—	—	—
	0.7	—	—	—	—	—	—	–45	–53	–50	–67	–61	–85	–78	–109	–108	–152	—	—
	0.6	—	—	—	—	—	—	—	—	–74	–96	–85	–114	–102	–138	–132	–181	–183	–246
	0.5	—	—	—	—	—	—	—	—	—	—	–128	–156	–145	–180	–175	–223	–226	–288
	0.4	—	—	—	—	—	—	—	—	—	—	—	—	–210	–243	–240	–286	–291	–351

1 All units in 'ps'.

2 Test conditions are at capacitance=15pF for DDR PADS. Recommended drive strengths are medium for SDCLK and high for address and controls.

3 SDRAM CLK and DQS related parameters are measured from the 50% point. That is, high is defined as 50% of the signal value, and low is defined as 50% of the signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and SDCLK (inverted clock).

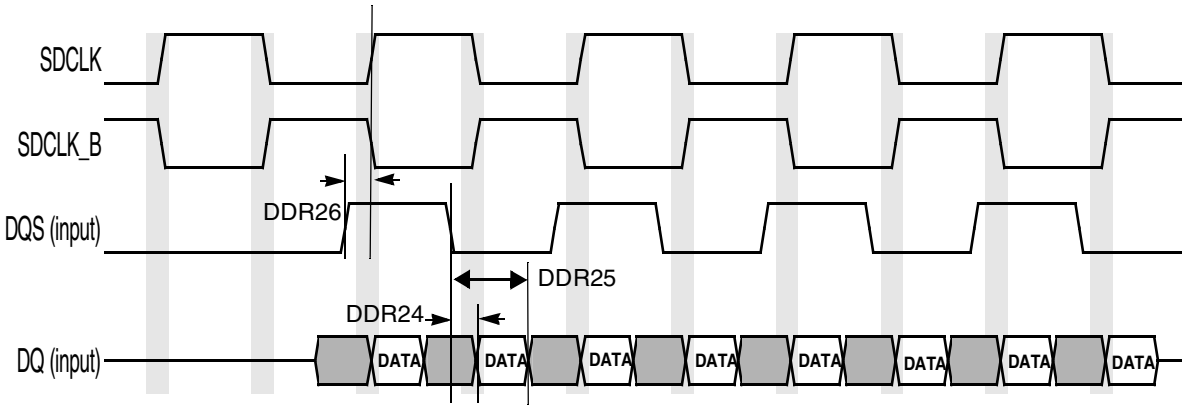

Figure 33. DDR2 SDRAM DQ vs. DQS and SDCLK READ Cycle Timing Diagram

Table 54. DDR2 SDRAM Read Cycle Parameter Table[1,2]

ID	Parameter	Symbol	DDR2-400		Unit
			Min.	Max.	
DDR24	DQS - DQ Skew (defines the Data valid window in read cycles related to DQS)	t_{DQSQ}	—	0.6	ns
DDR25	DQS DQ in HOLD time from DQS[3]	t_{QH}	2.5	—	ns
DDR26	DQS output access time from SDCLK posedge	t_{DQSCK}	–0.5	0.5	ns

1 Test conditions are at capacitance=15 pF for DDR PADS. Recommended drive strengths are medium for SDCLK and high for address and controls.

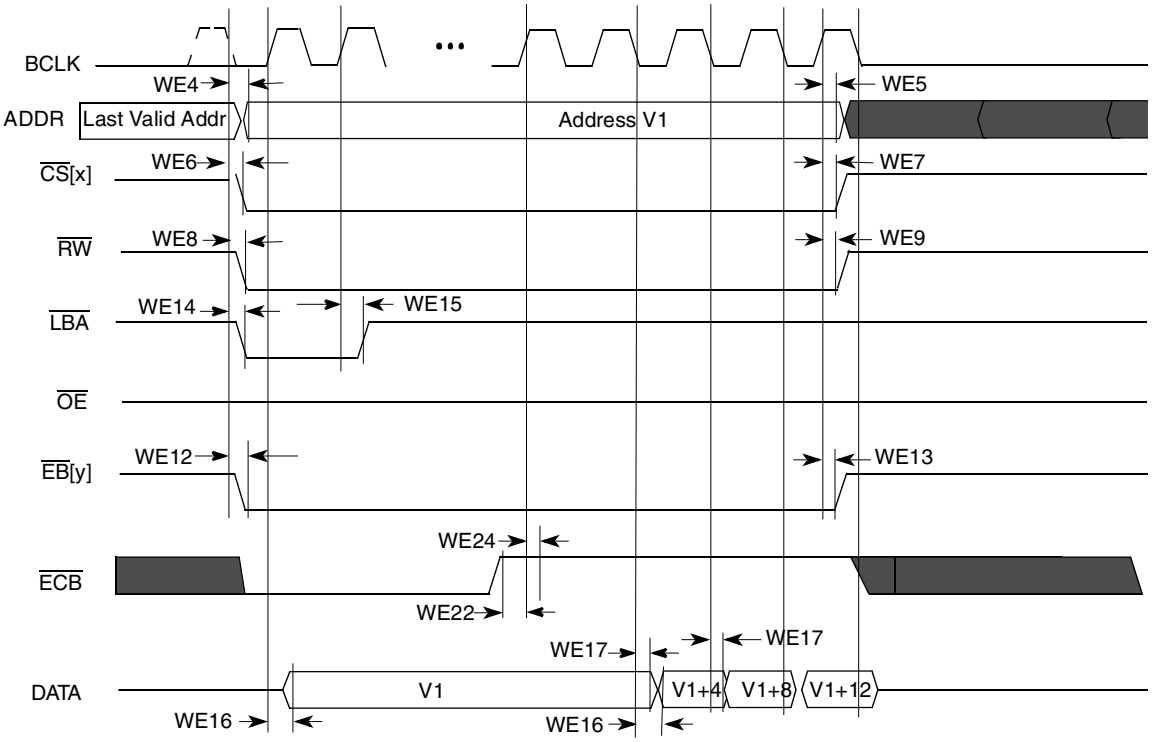

Figure 42. Synchronous Memory TIming Diagram for Burst Write Access—BCS=1, WSC=4, SYNC=1, DOL=0, PSR=1

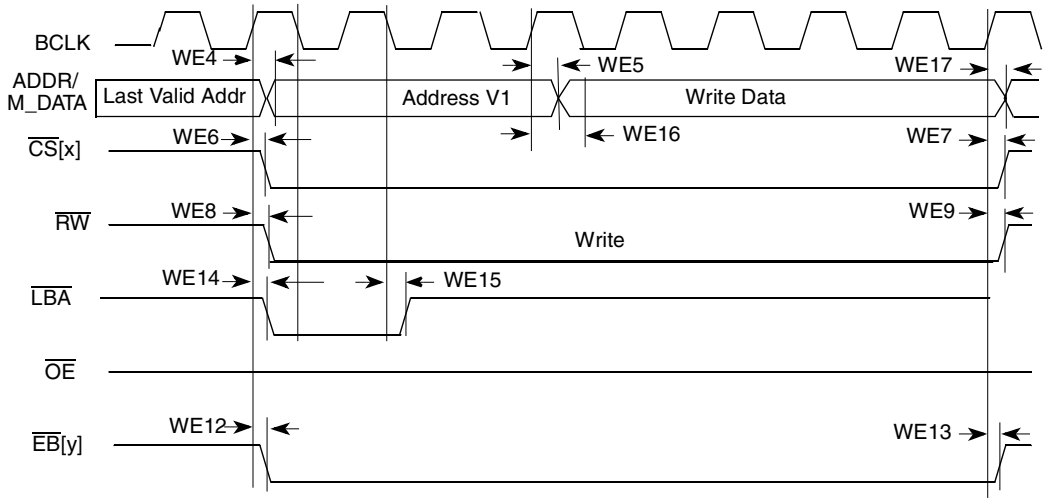

Figure 43. Muxed A/D Mode Timing Diagram for Synchronous Write Access—WSC=7, LBA=1, LBN=1, LAH=1

Figure 53 shows the ESAI HCKR timing diagram.

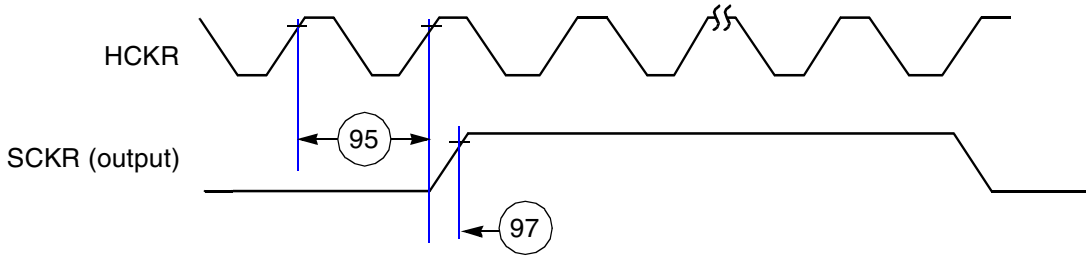

Figure 53. ESAI HCKR Timing

Table 60 describes the general timing requirements for the ESAI module. Table 58 and Table 59 describe respectively the conditions and signals cited in Table 60.

Table 58. ESAI Timing Conditions

Symbol	Significance	Comments
i ck	Internal clock	In the i.MX25, the internal clock frequency is equal to the IP bus frequency (133 MHz)
x ck	External clock	The external clock may be derived from the CRM module or other external clock sources
i ck a	Internal clock, asynchronous mode	In asynchronous mode, SCKT and SCKR are different clocks
i ck s	Internal clock, synchronous mode	In synchronous mode, SCKT and SCKR are the same clock

Table 59. ESAI Signals

Signal Name	Significance
SCKT	Transmit clock
SCKR	Receive clock
FST	Transmit frame sync
HCKT	Transmit high-frequency clock
HCKR	Receive high-frequency clock

Table 60. ESAI General Timing Requirements

No.	Characteristics[1 2]	Symbol	Expression[3]	Min.	Max.	Condition	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_c$ $4 \times T_c$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period For internal clock For external clock	— — —	— $2 \times T_c - 9.0$ $2 \times T_c$	— 6 15	— — —	— — —	ns
64	Clock low period For internal clock For external clock	 — —	 $2 \times T_c - 9.0$ $2 \times T_c$	 6 15	 — —	— —	ns

3.7.11 Inter IC Communication (I^2C) Timing

The I^2C communication protocol consists of the following seven elements:

- Start
- Data source/recipient
- Data direction
- Slave acknowledge
- Data
- Data acknowledge
- Stop

Figure 64 shows the timing of the I^2C module. Table 69 and Table 70 describe the I^2C module timing parameters (IC1–IC6) shown in the figure.

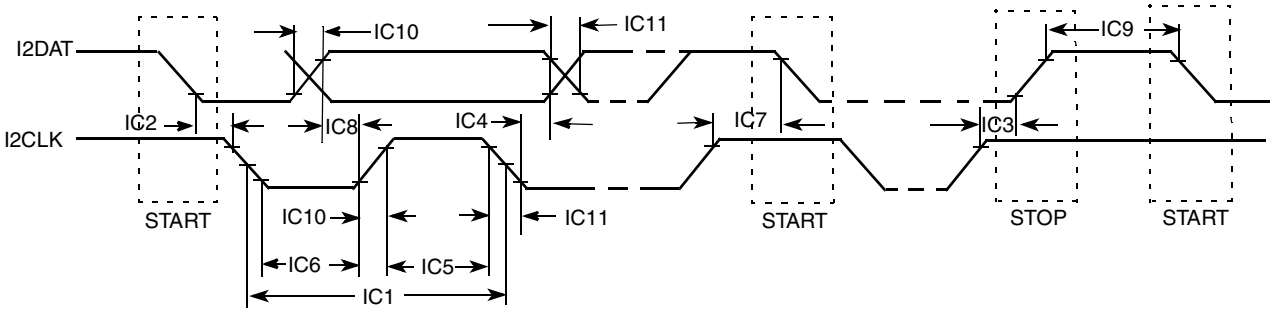

Figure 64. I^2C Module Timing Diagram

Table 69. I2C Module Timing Parameters: 3.0 V +/–0.30 V

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
IC1	I2CLK cycle time	10	-	2.5		µs
IC2	Hold time (repeated) START condition	4.0	-	0.6	-	µs
IC3	Set-up time for STOP condition	4.0	-	0.6	-	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	-	0.6	-	µs
IC6	LOW Period of the I2CLK Clock	4.7	-	1.3	-	µs
IC7	Set-up time for a repeated START condition	4.7	-	0.6	-	µs
IC8	Data set-up time	250	-	100[3]	-	ns
IC9	Bus free time between a STOP and START condition	4.7	-	1.3	-	µs
IC10	Rise time of both I2DAT and I2CLK signals	-	1000	$20+0.1C_b$[4]	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	-	300	$20+0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	-	400	-	400	pF

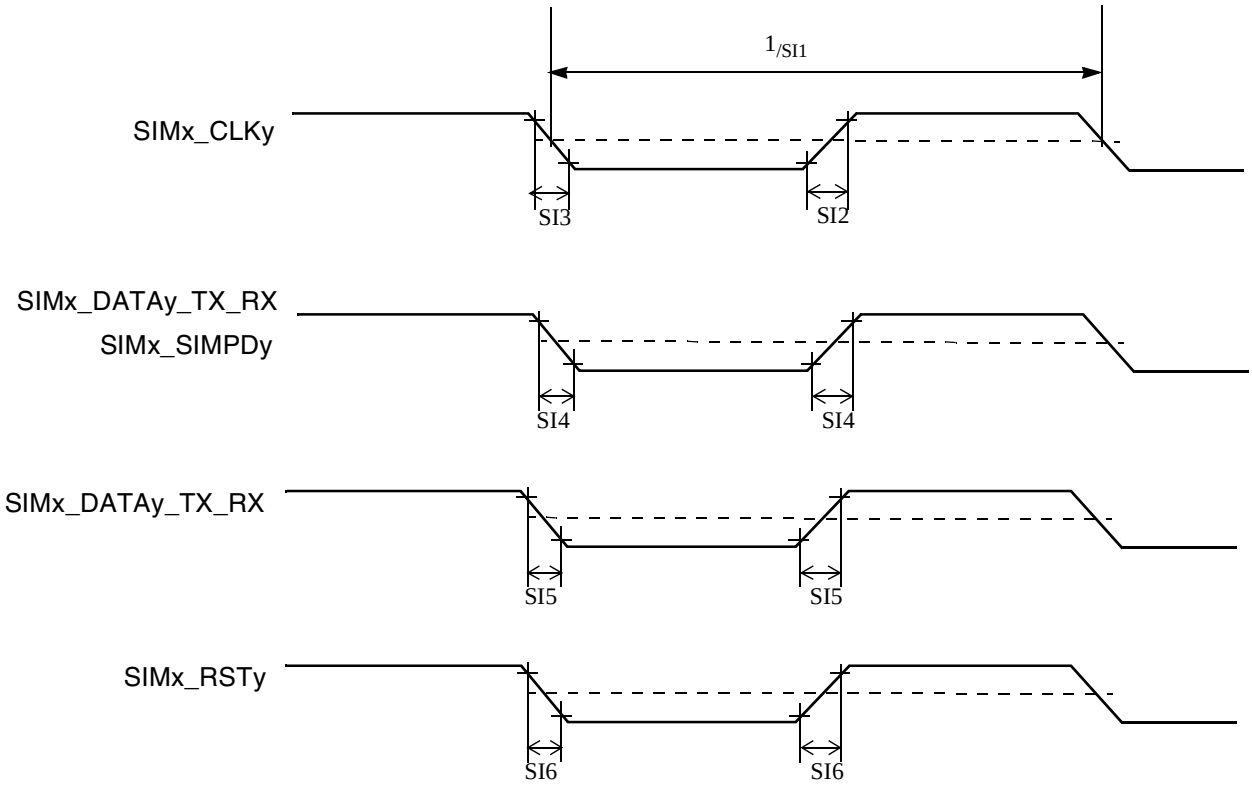

Figure 68. SIM Clock Timing Diagram

Table 74 defines the general timing requirements for the SIM interface.

Table 74. Timing Specifications, High Drive Strength

ID	Parameter	Symbol	Min.	Max.	Unit
SI1	SIM clock frequency (SIMx_CLKy)[1]	S_{freq}	0.01	25	MHz
SI2	SIM clock rise time (SIMx_CLKy)[2]	S_{rise}	—	$0.09 \times (1/S_{freq})$	ns
SI3	SIM clock fall time (SIMx_CLKy)[3]	S_{fall}	—	$0.09 \times (1/S_{freq})$	ns
SI4	SIM input transition time (SIMx_DATAy_RX_TX, SIMx_SIMPDy)	S_{trans}	10	25	ns
SI5	SIM I/O rise time / fall time (SIMx_DATAy_RX_TX)[4]	Tr/Tf	—	1	µs
SI6	SIM RST rise time / fall time (SIMx_RSTy)[5]	Tr/Tf	—	1	µs

1 50% duty cycle clock,
2 With C = 50 pF
3 With C = 50 pF
4 With Cin = 30 pF, Cout = 30 pF,
5 With Cin = 30 pF,

Table 83. SSI Transmitter Timing with External Clock

ID	Parameter	Min.	Max.	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	FS (bl) low/ high setup before (Tx) CK falling	–10.0	15.0	ns
SS29	FS (bl) low/ high setup before (Tx) CK falling	10.0	—	ns
SS31	FS (wl) low/ high setup before (Tx) CK falling	–10.0	15.0	ns
SS33	FS (wl) low/ high setup before (Tx) CK falling	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

Note:

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables figures.
- All timings are on pads when SSI is being used for data transfer.
- ”Tx” and “Rx” refer, respectively, to the transmit and receive sections of the SSI.
- For internal frame sync operation using external clock, the FS timing is the same as that of Tx data (for example, during AC97 mode of operation).

Figure 97 shows the USB parallel mode transmit/receive waveform. Table 99 describes the timing parameters (USB15–USB17) shown in the figure.

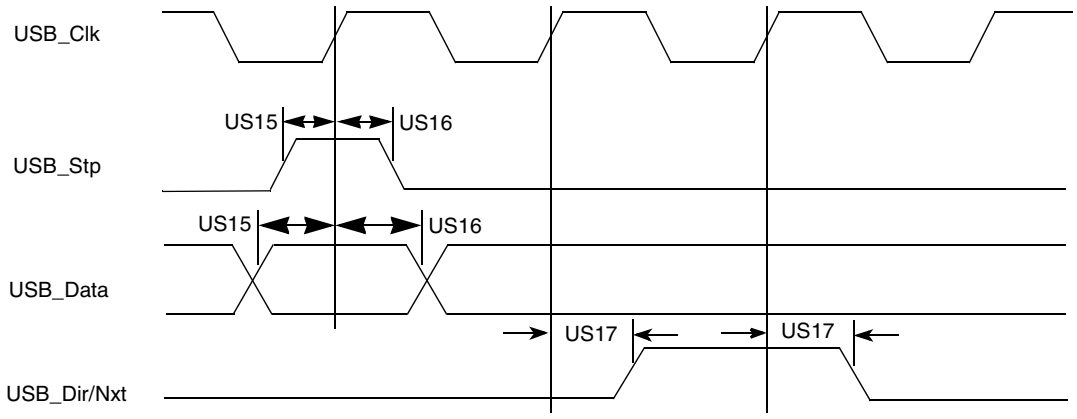

Figure 97. USB Parallel Mode Transmit/Receive Waveform

Table 99. USB Timing Specification in Parallel Mode

ID	Parameter	Min.	Max.	Unit	Conditions/Reference Signal
US15	Setup time (Dir&Nxt in, Data in)	6.0	—	ns	10 pF
US16	Hold time (Dir&Nxt in, Data in)	0.0	—	ns	10 pF
US17	Output delay time (Stp out, Data out	—	9.0	ns	10 pF

4 Package Information and Contact Assignment

4.1 400 MAPBGA—Case 17x17 mm, 0.8 mm Pitch

Figure 98 shows the 17×17 mm i.MX25 production package. The following notes apply to Figure 98:

- All dimensions in millimeters.
- Dimensioning and tolerancing per ASME Y14.5M-1994.
- Maximum solder bump diameter measured parallel to datum A.
- Datum A, the seating plane, is determined by the spherical crowns of the solder bumps.
- Parallelism measurement shall exclude any effect of mark on top surface of package.

Table 100. 17×17 mm Package Ground, Power Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
NVCC_DRYICE[1]	W11
NVCC_EMI1	G6, G7, G8, G9, H6, H7, H8, J6, J7
NVCC_EMI2	G12, G13, G14, G15, H12, H13, H14
NVCC_JTAG	U10
NVCC_LCDC	P6, P7, R6, R7
NVCC_MISC	N5, N6, N7
NVCC_NFC	L6, L7, L8
NVCC_SDIO	R17
OSC24M_GND	W15
OSC24M_VDD	W16
QGND	A1, A11, A20, B11, C11, D11, E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, E15, E16, F5, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, F16, G5, G10, G16, H5, H9, H10, H11, H15, H16, J5, J9, J10, J11, J15, J16, K1, K2, K3, K4, K5, K8, K9, K10, K11, K13, K14, K15, L5, L9, L10, L11, L12, L13, L14, L15, M8, M9, M10, M11, M12, M13, M14, M15, N9, N12, N13, N15, N16, P5, P13, P14, P15, P16, R5, R8, R9, R10, R11, R12, R13, R14, R15, R16, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, Y1, Y20
QVDD	G11, J8, J12, K6, K7, K12, M5, M6, M7, N8, P8, P9
REF	V11
UPLL_GND	M16
UPLL_VDD	L16
USBPHY1_UPLLVDD	M17
USBPHY1_UPLLVSS	N17
USBPHY1_VDDA	K16
USBPHY1_VDDA_BIAS	K19
USBPHY1_VSSA	L19
USBPHY1_VSSA_BIAS	J17
USBPHY2_VDD	W18
USBPHY2_VSS	W17

[1] NVCC_DRYICE is a supply output. An external capacitor no less than 4 µF must be connected to it. A 4.7 µF capacitor is recommended.

Table 105. 12x12 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
UART2_RTS	T2	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART2_CTS	P5	MISC	GPIO	INPUT	-
SD1_CMD	N22	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_CLK	N21	SDIO	GPIO	OUTPUT	High
SD1_DATA0	P22	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_DATA1	R22	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_DATA2	M22	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_DATA3	M21	SDIO	GPIO	INPUT	47 KΩ Pull-Up
KPP_ROW0	R2	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_ROW1	R4	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_ROW2	U1	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_ROW3	P4	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL0	T1	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL1	N5	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL2	P2	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL3	N4	MISC	GPIO	INPUT	100 KΩ Pull-Up
FEC_MDC	P1	MISC	GPIO	OUTPUT	Low
FEC_MDIO	M2	MISC	GPIO	INPUT	22 KΩ Pull-Up
FEC_TDATA0	L2	MISC	GPIO	OUTPUT	High
FEC_TDATA1	M1	MISC	GPIO	OUTPUT	High
FEC_TX_EN	R1	MISC	GPIO	OUTPUT	Low

Table 105. 12x12 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
GPIO_E	R21	CRM	GPIO	INPUT	100 KΩ Pull-Up
GPIO_F	R19	CRM	GPIO	INPUT	-
EXT_ARMCLK	V22	CRM	GPIO	INPUT	-
UPLL_BYPCLK	U21	CRM	GPIO	INPUT	-
VSTBY_REQ	T21	CRM	GPIO	OUTPUT	Low
VSTBY_ACK[3]	W22	CRM	GPIO	OUTPUT	Low
POWER_FAIL	T19	CRM	GPIO	INPUT	100 KΩ Pull-Down
RESET_B	U19	CRM	GPIO	INPUT	100 KΩ Pull-Up
POR_B	V21	CRM	GPIO	INPUT	100 KΩ Pull-Up
CLKO	Y22	CRM	GPIO	OUTPUT	Low
BOOT_MODE0[2]	AA22	CRM	GPIO	INPUT	100 KΩ Pull-Down
BOOT_MODE1[2]	W21	CRM	GPIO	INPUT	100 KΩ Pull-Down
CLK_SEL	AA20	CRM	GPIO	INPUT	100 KΩ Pull-Down
TEST_MODE	AA19	CRM	GPIO	INPUT	100 KΩ Pull-Down
OSC24M_EXTAL	AB19	OSC24M	ANALOG	ANALOG	-
OSC24M_XTAL	AB20	OSC24M	ANALOG	ANALOG	-
OSC32K_EXTAL	AB13	DRYICE	ANALOG	ANALOG	-
OSC32K_XTAL	AB12	DRYICE	ANALOG	ANALOG	-
TAMPER_A	V11	DRYICE	ANALOG	ANALOG	-
TAMPER_B	V13	DRYICE	ANALOG	ANALOG	-
MESH_C	T13	DRYICE	ANALOG	ANALOG	-
MESH_D	R13	DRYICE	ANALOG	ANALOG	-
OSC_BYP	AB15	DRYICE	ANALOG	ANALOG	-
XP	AA18	ADC	ANALOG	ANALOG	-
XN	AA16	ADC	ANALOG	ANALOG	-
YP	AB17	ADC	ANALOG	ANALOG	-
YN	W15	ADC	ANALOG	ANALOG	-

Table 107. i.MX25 12×12 Package Ball Map (continued)

	AB	AA	Y	W	V	U	T	R	
1	QGND	CSPI1_MOSI	CSPI1_SCLK	UART1_RTS	UART2_RXD	KPP_ROW2	KPP_COL0	FEC_TX_EN	1
2	LSCLK	QGND	CONTRAST	QGND	CSPI1_SS0	UART1_RXD	UART2_RTS	KPP_ROW0	2
3	LD14	OE_ACD							3
4	LD12	HSYNC		PWM	CSPI1_MISO	CSPI1_SS1	UART2_TXD	KPP_ROW1	4
5	LD10	LD15		VSYNC		CSPI1_RDY	QGND	UART1_CTS	5
6	LD8	LD9		LD13	UART1_TXD		QGND		6
7	LD6	LD7		LD11			NVCC_MISC	NVCC_MISC	7
8	LD4	LD5		LD1			NVCC_LCDC	NVCC_LCDC	8
9	LD2	LD3		QGND			QVDD	NVCC_LCDC	9
10	LD0	BAT_VDD		NVCC_JTAG	QVDD		QVDD	QVDD	10
11	SJC_MOD	TDO		DE_B	TAMPER_A		QGND	QGND	11
12	OSC32K_XTAL	TMS		TDI			QGND	QGND	12
13	OSC32K_EXTAL	TCK		RTCK	TAMPER_B		MESH_C	MESH_D	13
14	TRSTB	REF		INAUX1				NVCC_DRYICE	14
15	OSC_BYP	INAUX0		YN	OSC24M_VDD		OSC24M_GND	QVDD	15
16	INAUX2	XN		USBPHY2_VSS			USBPHY2_VDD	QVDD	16
17	YP	WIPER		USBPHY2_DP	MPLL_GND				17
18	QGND	XP		USBPHY2_DM	QGND		QGND	QGND	18
19	OSC24M_EXTAL	TEST_MODE		MPLL_VDD	QGND	RESET_B	POWER_FAIL	GPIO_F	19
20	OSC24M_XTAL	CLK_SEL							20
21	QGND	QGND	QGND	BOOT_MODE1	POR_B	UPLL_BYPCLK	VSTBY_REQ	GPIO_E	21
22	QGND	BOOT_MODE0	CLKO	VSTBY_ACK	EXT_ARMCLK	GPIO_C	GPIO_A	SD1_DATA1	22