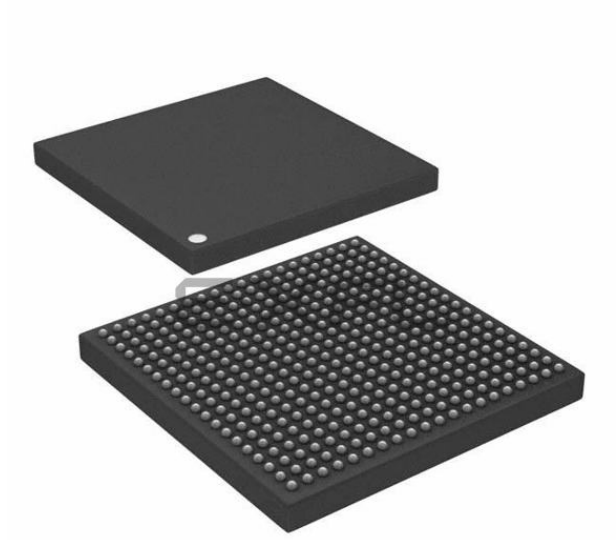

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx257cjm4ar2

Table 4. Signal Considerations (continued)

Signal	Description
MESH_C, MESH_D	Wire-mesh tamper detect pins that can be routed at the PCB board to detect attempted tampering of a protected wire. When security measures are implemented, MESH_C should be pulled-up or connected to NVCC_DRYICE and triggers a tamper event when floating or when connected to MESH_D. MESH_D should be pulled-down or connected to GND and triggers an event when floating or connected to MESH_C. These pins can be left unconnected if the DryIce security features are not being used.
NVCC_DRYICE	This is the DryIce power supply output. The supply source is QVDD when the i.MX25 is in run mode. When i.MX25 is in reduced power mode, the DryIce supply source is the BATT_VDD supply. This pin can be used to power external DryIce components (external tamper detect, wire-mesh tamper detect). In order to guarantee the power-loss protection feature which guarantees that RTC and/or secure keys be maintained after power-off an external capacitor no less than 4 µF must be connected to this supply output pin. A 4.7 µF capacitor is recommended.
OSC_BYP	The 32 kHz oscillator bypass-control pin. If this signal is pulled down, then OSC32K_EXTAL and OSC32K_XTAL analog pins should be tied to the external 32.768 kHz crystal circuit. If on the other hand the signal is pulled up, then the external 32 kHz oscillator output clock must be connected to OSC32K_EXTAL analog pin, and OSC32K_XTAL can be no connect (NC).
OSC32K_EXTAL OSC32K_XTAL	These analog pins are connected to an external 32 kHz CLK circuit depending on the state of OSC_BYP pin (see the description of OSC_BYP under the preceding bullet). The 32 kHz reference CLK is required for normal operation.
POWER_FAIL	An interrupt from PMIC, which should be connected to a low-battery detection circuit. This signal is internally connected to an on-chip 100 kΩ pull-down device. If there is no low-battery detection, then users can tie this pin to GND through a pull-down resistor, or leave the signal as NC. This pin can also be configured to work as a normal GPIO.
REF	External ADC reference voltage. REF may be tied to GND if the user plans to only use the internally generated 2.5 V reference supply.
SJC_MOD	Must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed, but the value should be much smaller than the on-chip 100 kΩ pull-up.
TAMPER_A, TAMPER _B	DryIce external tamper detect pins, active high. If TAMPER_A or TAMPER_B is connected to NVCC_DRYICE, then external tampering is detected. These pins can be left unconnected if the DryIce security features are not being used.
TEST_MODE	For Freescale factory use only. This signal is internally connected to an on-chip pull-down device. Users must either float this signal or tie it to GND.
UPLL_BYPCLK	Primarily for Freescale factory use. There is no internal on-chip pull-up/down on this pin, so it must be externally connected to GND or VDD. Aside from factory use, this pin can also be configured (through muxing) to work as a normal GPIO.
USBPHY1_RREF	Determines the reference current for the USB PHY1 bandgap reference. An external 10 kΩ 1% resistor to GND is required.
USBPHY2_DM USBPHY2_DP	The output impedance of these signals is expected at 10 Ω. It is recommended to also have on-board 33 Ω series resistors (close to the pins).

Table 21. Slow I/O AC Parameters (continued)

Parameter	Symbol	Test Voltage	Test Capacitance	Min. Rise/Fall	Typ. Rise/Fall	Max. Rise/Fall	Units
Output pad dI/dt[3] (max. drive)	tdit	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	15 16 7 7	36 38 21 22	76 80 56 58	mA /ns
Output pad dI/dt[3] (high drive)	tdit	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	8 9 5 5	20 21 14 15	45 47 38 40	
Output pad dI/dt[3] (standard drive)	tdit	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	4 4 2 2	10 10 7 7	22 23 18 19	
Input pad propagation delay without hysteresis, 50%–50%[4]	tpi	—	1.6 pF	0.82/0.47 0.74/1	1.1/0.76 1.1/1.5	1.6/1.04 1.75/2.16	ns
Input pad propagation delay with hysteresis, 50%–50%[4]	tpi	—	1.6 pF	1.1/1.3 1.75/1.63	1.43/1.6 2.67/2.22	2/2 2.92/3	
Input pad propagation delay without hysteresis, 40%–60%[4]	tpi	—	1.6 pF	1.62/1.28 1.82/1.55	1.9/1.56 2.28/1.87	2.38/1.82 2.95/2.54	
Input pad propagation delay with hysteresis, 40%–60%[4]	tpi	—	1.6 pF	1.88/2.1 2.4/2.6	2.2/2.4 3/3.07	2.7/2.75 3.77/3.71	
Input pad transition times without hysteresis[4]	trfi	—	1.6 pF	0.16/0.12	0.23/0.18	0.33/0.29	
Input pad transition times with hysteresis[4]	trfi		1.6 pF	0.16/0.13	0.22/0.18	0.33/0.29	
Maximum input transition times[5]	trm	—	—	—	—	25	ns

1 Maximum condition for tpr, tpo, and tpv: wcs model, 1.1 V, I/O 3.0 V (3.0–3.6 V range) or 1.65 V (1.65–1.95 V range), and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 3.6 V (3.0–3.6 V range) or 1.95 V (1.65–1.95 V range), and –40 °C. Input transition time from core is 1 ns (20%–80%).

2 Minimum condition for tps: wcs model, 1.1 V, I/O 3.0 V (3.0–3.6 V range) or 1.65 V (1.65–1.95 V range), and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

3 Maximum condition for tdit: bcs model, 1.3 V, I/O 3.6 V (3.0–3.6 V range) or 1.95 V (1.65–1.95 V range), and –40 °C.

4 Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 3.0 V (3.0–3.6 V range) or 1.65 V (1.65–1.95 V range), and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 3.6 V or 1.95 V (1.65–1.95 V range), and –40 °C. Input transition time from pad is 5 ns (20%–80%).

5 Hysteresis mode is recommended for input with transition time greater than 25 ns.

Table 23. Fast I/O AC Parameters for OVDD = 3.0–3.6 V (continued)

Output Pad Propagation Delay[1] (High Drive), 50%–50%	tpo	25 pF 50 pF	1.35/1.42 1.98/2.04	1.95/1.91 2.81/2.68	2.96/2.76 4.16/3.78	ns
Output Pad Propagation Delay[1] (Standard Drive), 50%–50%	tpo	25 pF 50 pF	1.77/1.85 2.70/2.78	2.54/2.48 3.82/3.62	3.80/3.60 5.62/5.10	ns
Output Pad Propagation Delay[1] (Max Drive), 40%–60%	tpo	25 pF 50 pF	1.37/1.50 1.74/1.88	1.94/2.05 2.46/2.55	2.95/3.07 3.71/3.75	ns
Output Pad Propagation Delay[1] (High Drive), 40%–60%	tpo	25 pF 50 pF	1.48/1.61 1.98/2.10	2.11/2.19 2.78/2.81	3.19/3.26 4.14/4.09	ns
Output Pad Propagation Delay[1] (Standard Drive), 40%–60%	tpo	25 pF 50 pF	1.84/1.97 2.58/2.71	2.61/2.67 3.62/3.58	3.95/3.95 5.36/5.15	ns
Output Enable to Output Valid Delay[1] (Max Drive), 50%–50%	tpv	25 pF 50 pF	1.34/1.32 1.81/1.79	1.91/1.81 2.56/2.40	2.92/2.67 3.83/3.47	ns
Output Enable to Output Valid Delay[1] (High Drive), 50%–50%	tpv	25 pF 50 pF	1.48/1.47 2.12/2.1	2.12/2.00 2.98/2.76	3.21/2.92 4.41/3.94	ns
Output Enable to Output Valid Delay[1] (Standard Drive), 50%–50%	tpv	25 pF 50 pF	1.90/1.90 2.85/2.83	2.70/2.60 4.00/3.70	4.07/3.74 5.86/5.24	ns
Output Enable to Output Valid Delay[1] (Max Drive), 40%–60%	tpv	25 pF 50 pF	1.55/1.42 1.93/1.81	2.25/2.08 2.77/2.58	3.50/3.31 4.24/3.99	ns
Output Enable to Output Valid Delay[1] (High Drive), 40%–60%	tpv	25 pF 50 pF	1.67/1.54 2.16/2.03	2.41/2.23 3.08/2.86	3.74/3.51 4.66/4.34	ns
Output Enable to Output Valid Delay[1] (Standard Drive), 40%–60%	tpv	25 pF 50 pF	2.02/1.90 2.76/2.63	2.91/2.71 3.91/3.62	4.48/4.21 5.85/5.39	ns
Output Pad Slew Rate[2] (Max Drive)	tps	25 pF 50 pF	0.96/1.40 0.54/0.83	1.54/2.10 0.85/1.24	2.30/3.00 1.26/1.70	V/ns
Output Pad Slew Rate[2] (High Drive)	tps	25 pF 50 pF	0.76/1.10 0.41/0.64	1.19/1.71 0.63/0.95	1.78/2.39 0.95/1.30	V/ns
Output Pad Slew Rate[2] (Standard Drive)	tps	25 pF 50 pF	0.52/0.78 0.28/0.44	0.80/1.19 0.43/0.64	1.20/1.60 0.63/0.87	V/ns
Output Pad di/dt[3] (Max Drive)	didt	25 pF 50 pF	46 49	108 113	250 262	mA/ns
Output Pad di/dt[3] (High Drive)	didt	25 pF 50 pF	35 37	82 86	197 207	mA/ns
Output Pad di/dt[3] (Standard Drive)	didt	25 pF 50 pF	22 23	52 55	116 121	mA/ns
Input Pad Propagation Delay without Hysteresis, 50%–50%[4]	tpi	1.6pF	0.729/0.458	0.97/0.0649	1.404/0.97	ns
Input Pad Propagation Delay with Hysteresis, 50%–50%[4]	tpi	1.6pF	1.203/0.938	1.172/1.187	1.713/1.535	ns
Input Pad Propagation Delay without Hysteresis, 40%–60%[4]	tpi	1.6pF	0.879/0.977	1.434/1.12	1.854/1.427	ns

3.7.2.3.1 UDMA In-Transfer Timing

Figure 15 shows the timing for UDMA in-transfer start.

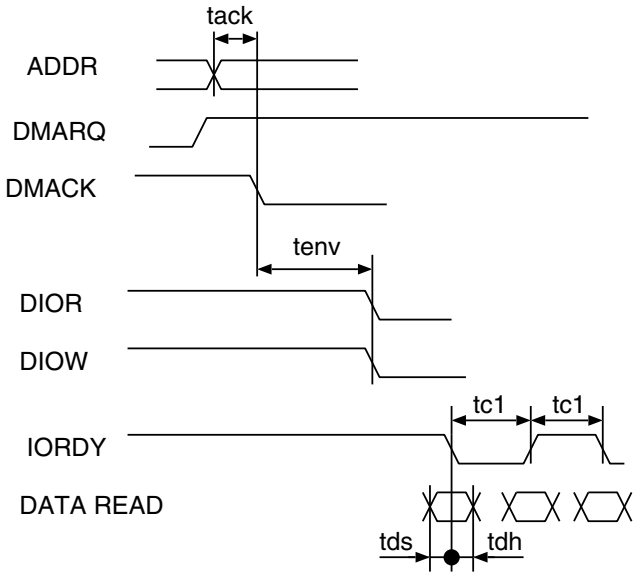

Figure 15. Timing for UDMA In-Transfer Start

Figure 16 shows the timing for host-terminated UDMA in-transfer.

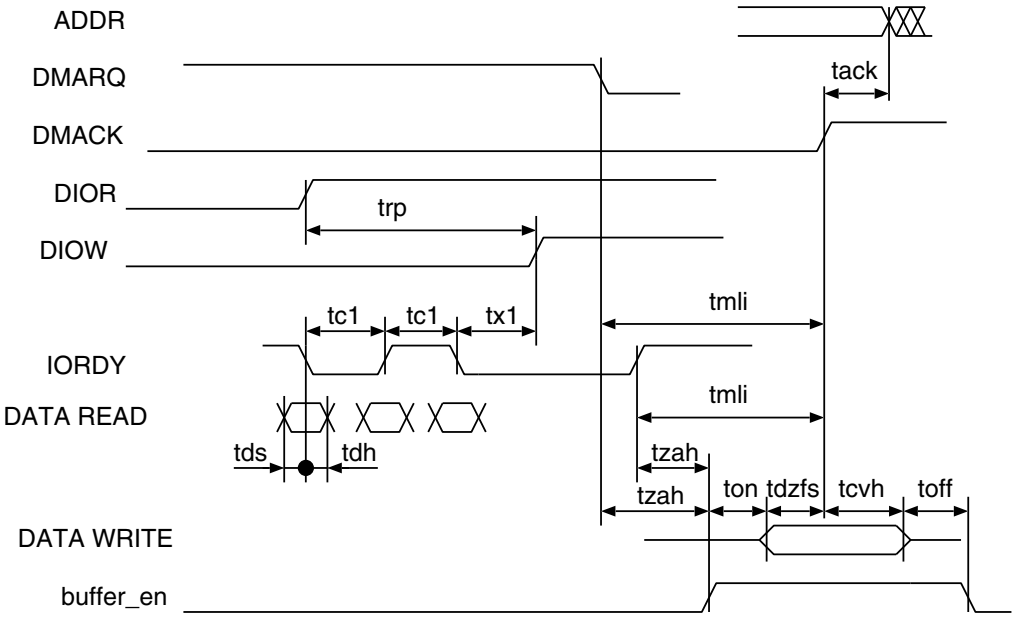

Figure 16. Timing for Host-Terminated UDMA In-Transfer

Timing parameters for UDMA out-bursts are listed in Table 40.

Table 40. Timing Parameters UDMA Out-Bursts

ATA Parameter	Spec Parameter	Value	How to Meet?
tack	tack	tack(min.) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv(min.) = (time_env × T) – (tskew1 + tskew2) tenv(max.) = (time_env × T) + (tskew1 + tskew2)	time_env
tdvs	tdvs	tdvs = (time_dvs × T) – (tskew1 + tskew2)	time_dvs
tdvh	tdvh	tdvs = (time_dvh × T) – (tskew1 + tskew2)	time_dvh
tcyc	tcyc	tcyc = time_cyc × T – (tskew1 + tskew2)	time_cyc
t2cyc	—	t2cyc = time_cyc × 2 × T	time_cyc
trfs1	trfs	trfs = 1.6 × T + tsui + tco + tbuf + tbuf	—
—	tdzfs	tdzfs = time_dzfs × T – (tskew1)	time_dzfs
tss	tss	tss = time_ss × T – (tskew1 + tskew2)	time_ss
tmli	tdzfs_mli	tdzfs_mli =max.(time_dzfs, time_mli) × T – (tskew1 + tskew2)	—
tli	tli1	tli1 > 0	—
tli	tli2	tli2 > 0	—
tli	tli3	tli3 > 0	—
tcvh	tcvh	tcvh = (time_cvh × T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

3.7.3 Digital Audio Mux (AUDMUX) Timing

The AUDMUX provides a programmable interconnect logic for voice, audio, and data routing between internal serial interfaces (SSI and SAP) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI modules. For more information, see Section 3.7.17, “Synchronous Serial Interface (SSI) Timing.”

3.7.4 CMOS Sensor Interface (CSI) Timing

The CSI enables the chip to connect directly to external CMOS image sensors, which are classified as dumb or smart as follows:

- Dumb sensors only support traditional sensor timing (vertical sync (VSYNC) and horizontal sync (HSYNC)) and output-only Bayer and statistics data.
- Smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats).

The following subsections describe the CSI timing in gated and ungated clock modes.

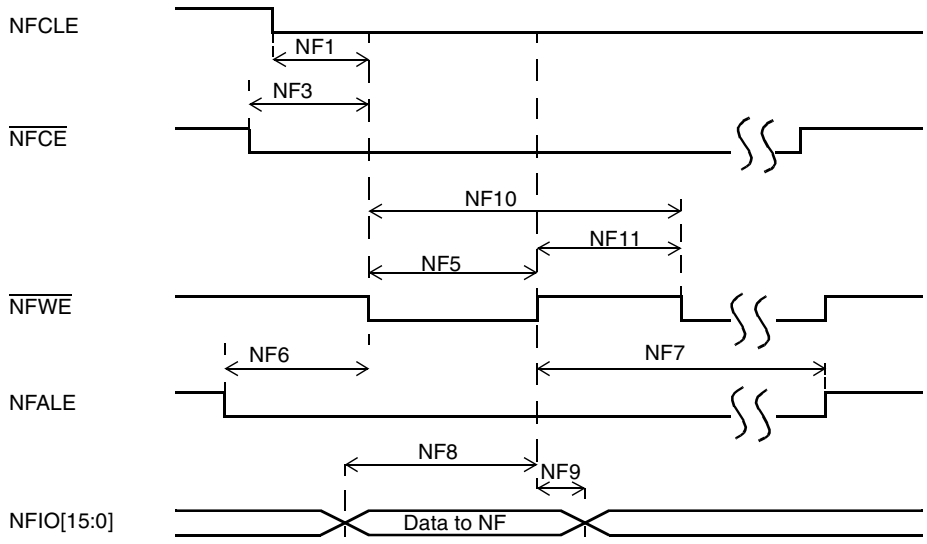

Figure 36. Write Data Latch Cycle Timing Diagram

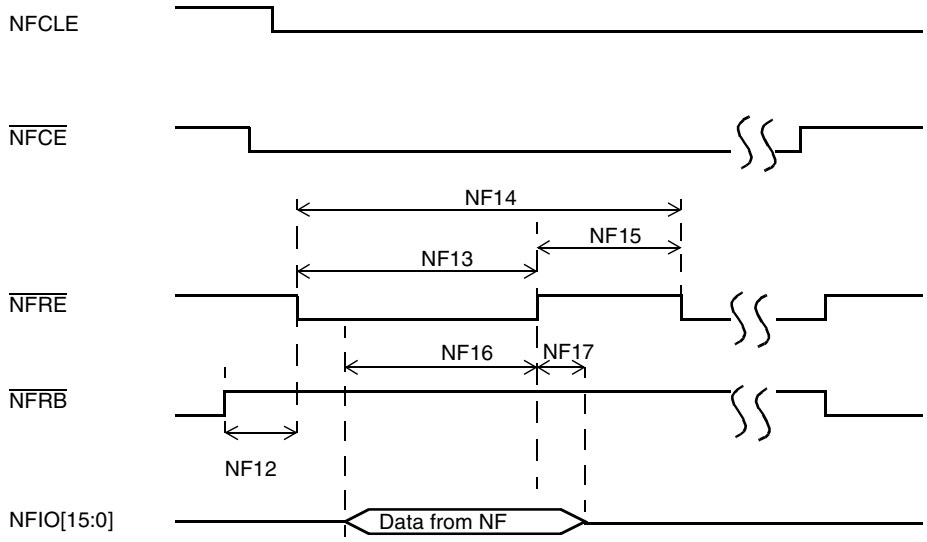

Figure 37. Read Data Latch Cycle Timing Diagram

Table 55. NFC Timing Parameters[1]

ID	Parameter	Symbol	Timing T = NFC Clock Cycle		Example Timing for NFC Clock ≈ 33 MHz T = 30 ns		Unit
			Min.	Max.	Min.	Max.	
NF1	NFCLE setup time	tCLS	T–1.0 ns	—	29	—	ns
NF2	NFCLE hold time	tCLH	T–2.0 ns	—	28	—	ns
NF3	$\overline{\text{NFCE}}$ setup time	tCS	2T–5.0 ns	—	55	—	ns
NF4	$\overline{\text{NFCE}}$ hold time	tCH	7T–5.0 ns	—	205	—	ns

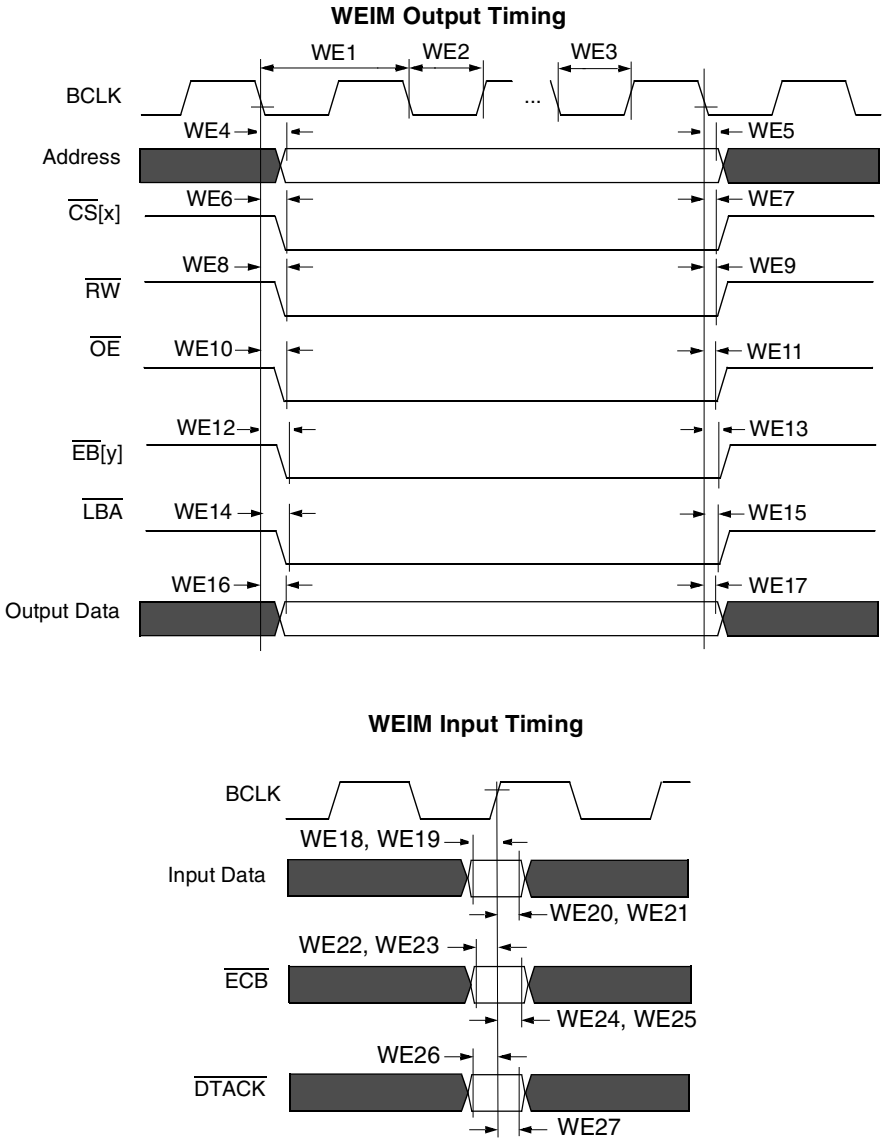

Figure 38. WEIM Bus Timing Diagram

Table 56. WEIM Bus Timing Parameters[1]

ID	Parameter	Min.	Max.	Unit
WE1	BCLK cycle time[2]	14.5	—	ns
WE2	BCLK low-level width[2]	7	—	ns
WE3	BCLK high-level width[2]	7	—	ns
WE4	Clock fall to address valid	15	21	ns
WE5	Clock rise/fall to address invalid	22	25	ns
WE6	Clock rise/fall to $\overline{CS}$[x] valid	15	19	ns
WE7	Clock rise/fall to $\overline{CS}$[x] invalid	3.3	5	ns

Figure 39 through Figure 44 give examples of basic WEIM accesses to external memory devices with the timing parameters described in Table 56 for specific control parameter settings.

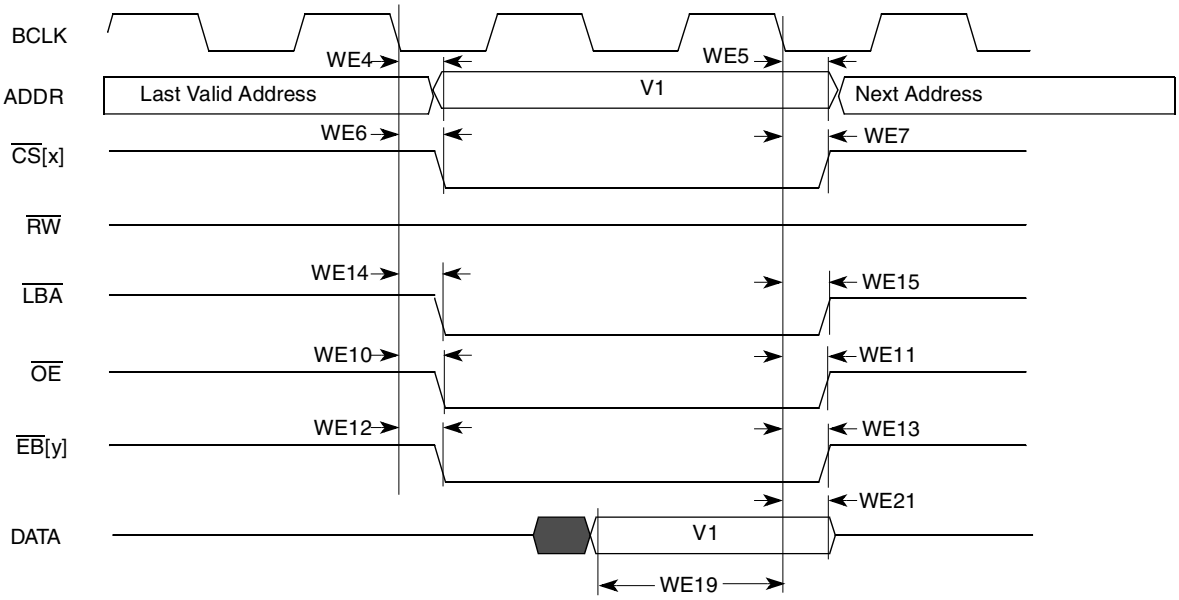

Figure 39. Synchronous Memory Timing Diagram for Read Access—WSC=1

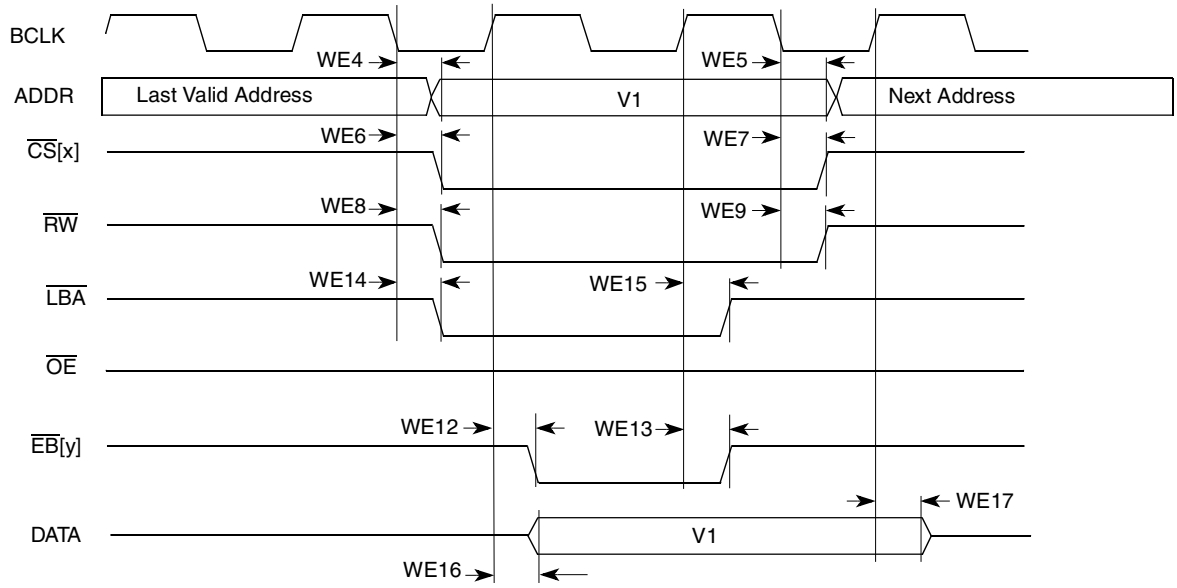

Figure 40. Synchronous Memory Timing Diagram for Write Access—WSC=1, EBWA=1, EBWN=1, LBN=1

Table 57. WEIM Asynchronous Timing Parameters Relative to Chip Select Table (continued)

Ref No.	Parameter	Determination By Synchronous Measured Parameters[1]	Min	Max (If 133 MHz is supported by SoC)	Unit
WE32A(muxed A/D	$\overline{CS}$[x] valid to Address Invalid	WE4 – WE7 + (LBN + LBA + 1 – CSA[2])	–3 + (LBN + LBA + 1 – CSA)	—	ns
WE33	$\overline{CS}$[x] Valid to $\overline{RW}$ Valid	WE8 – WE6 + (RWA – CSA)	—	3 + (RWA – CSA)	ns
WE34	$\overline{RW}$ Invalid to $\overline{CS}$[x] Invalid	WE7 – WE9 + (RWN – CSN)	—	3 – (RWN_CSN)	ns
WE35	$\overline{CS}$[x] Valid to $\overline{OE}$ Valid	WE10 – WE6 + (OEA – CSA)	—	3 + (OEA – CSA)	ns
WE35A (muxed A/D)	$\overline{CS}$[x] Valid to $\overline{OE}$ Valid	WE10 – WE6 + (OEA + LBN + LBA + LAH + 1 – CSA)	–3 + (OEA + LBN + LBA + LAH + 1 – CSA)	3 + (OEA + LBN + LBA + LAH + 1 – CSA)	ns
WE36	$\overline{OE}$ Invalid to $\overline{CS}$[x] Invalid	WE7 – WE11 + (OEN – CSN)	—	3 – (OEN – CSN)	ns
WE37	$\overline{CS}$[x] Valid to $\overline{EB}$[y] Valid (Read access)	WE12 – WE6 + (EBRA – CSA)	—	3 + (EBRA[4] – CSA)	ns
WE38	$\overline{EB}$[y] Invalid to $\overline{CS}$[x] Invalid (Read access)	WE7 – WE13 + (EBRN – CSN)	—	3 – (EBRN[5] – CSN)	ns
WE39	$\overline{CS}$[x] Valid to $\overline{LBA}$ Valid	WE14 – WE6 + (LBA – CSA)	—	3 + (LBA – CSA)	ns
WE40	$\overline{LBA}$ Invalid to $\overline{CS}$[x] Invalid	WE7 – WE15 – CSN	—	3 – CSN	ns
WE40A (muxed A/D)	$\overline{CS}$[x] Valid to $\overline{LBA}$ Invalid	WE14 – WE6 + (LBN + LBA + 1 – CSA)	–3 + (LBN + LBA + 1 – CSA)	3 + (LBN + LBA + 1 – CSA)	ns
WE41	$\overline{CS}$[x] Valid to Output Data Valid	WE16 – WE6 – CSA	—	3 – CSA	ns
WE41A (muxed A/D)	$\overline{CS}$[x] Valid to Output Data Valid	WE16 – WE6 + (LBN + LBA + LAH + 1 – CSA)	—	3 + (LBN + LBA + LAH + 1 – CSA)	ns
WE42	Output Data Invalid to $\overline{CS}$[x] Invalid	WE17 – WE7 – CSN	—	3 – CSN	ns
WE43	Input Data Valid to $\overline{CS}$[x] Invalid	MAXCO – MAXCSO + MAXDI	MAXCO[6] – MAXCSO[7] + MAXDI[8]	—	ns
WE44	$\overline{CS}$[x] Invalid to Input Data invalid	0	0	—	ns
WE45	$\overline{CS}$[x] Valid to $\overline{EB}$[y] Valid (Write access)	WE12 – WE6 + (EBWA – CSA)	—	3 + (EBWA – CSA)	ns
WE46	$\overline{EB}$[y] Invalid to $\overline{CS}$[x] Invalid (Write access)	WE7 – WE13 + (EBWN – CSN)	—	–3 + (EBWN – CSN)	ns
WE47	$\overline{DTACK}$ Valid to $\overline{CS}$[x] Invalid	MAXCO – MAXCSO + MAXDTI	MAXCO[6] – MAXCSO[7] + MAXDTI[9]	—	ns
WE48	$\overline{CS}$[x] Invalid to $\overline{DTACK}$ invalid	0	0	—	ns

3.7.10 Controller Area Network (FlexCAN) Transceiver Parameters and Timing

Table 67 and Table 68 show voltage requirements for the FlexCAN transceiver Tx and Rx pins.

Table 67. Tx Pin Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
High-level output voltage	V_{OH}	2	—	Vcc[1] + 0.3	V
Low-level output voltage	V_{OL}	—	0.8	—	V

1 Vcc = +3.3 V ± 5%

Table 68. Rx Pin Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
High-level input voltage	V_{IH}	0.8 × Vcc[1]	—	Vcc[1]	V
Low-level input voltage	V_{IL}	—	0.4	—	V

1 Vcc = +3.3 V ± 5%

Figure 60 through Figure 63 show the FlexCAN timing, including timing of the standby and shutdown signals.

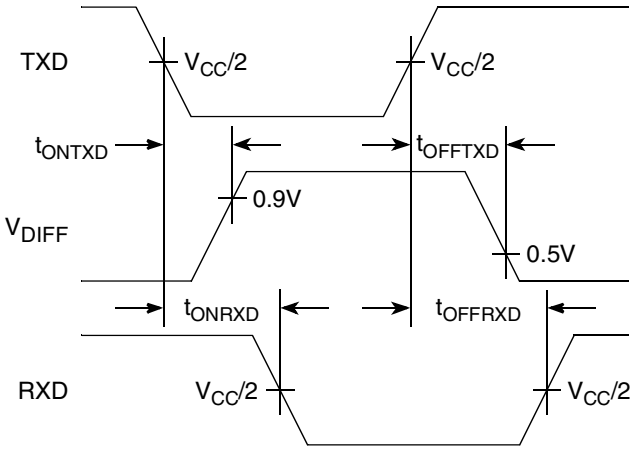

Figure 60. FlexCAN Timing Diagram

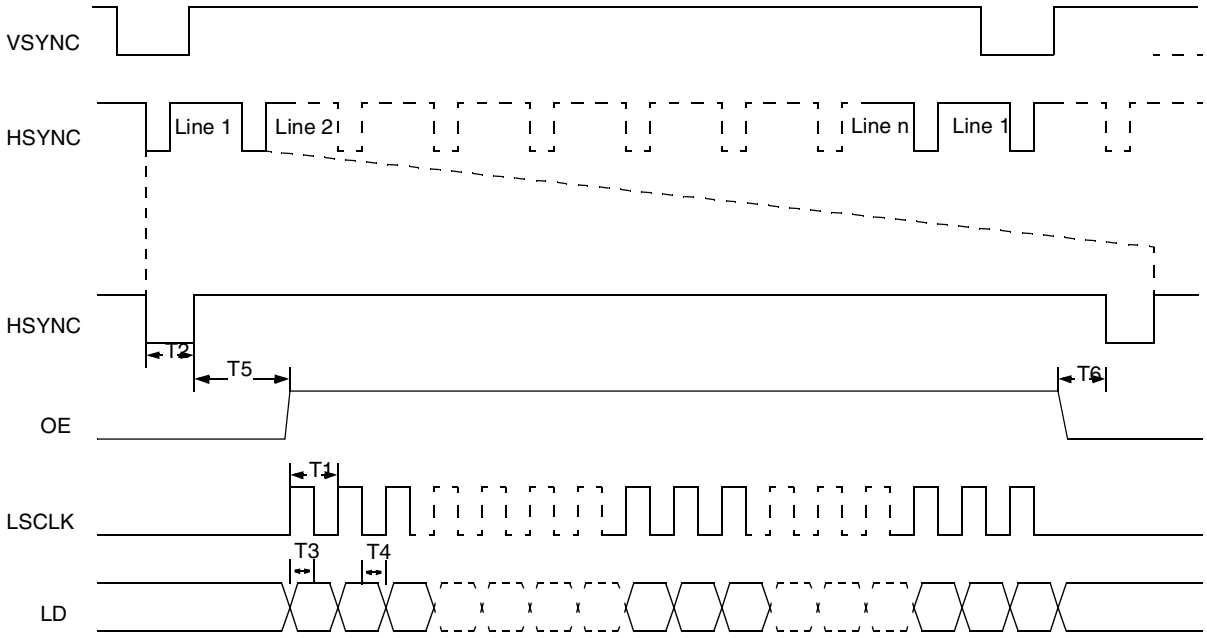

Figure 66. LCDC TFT Mode Timing Diagram

Table 72. LCDC TFT Mode Timing Parameters

ID	Description	Min.	Ma	Unit
T1	Pixel clock period	22.5	1000	ns
T2	HSYNC width	1	—	T[1]
T3	LD setup time	5	—	ns
T4	LD hold time	5	—	ns
T5	Delay from the end of HSYNC to the beginning of the OE pulse	3	—	T[1]
T6	Delay from end of OE to the beginning of the HSYNC pulse	1	—	T[1]

1 T is pixel clock period

3.7.13 Pulse Width Modulator (PWM) Timing Parameters

Figure 67 depicts the timing of the PWM, and Table 73 lists the PWM timing characteristics.

The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse width modulator output (PWMO) external pin.

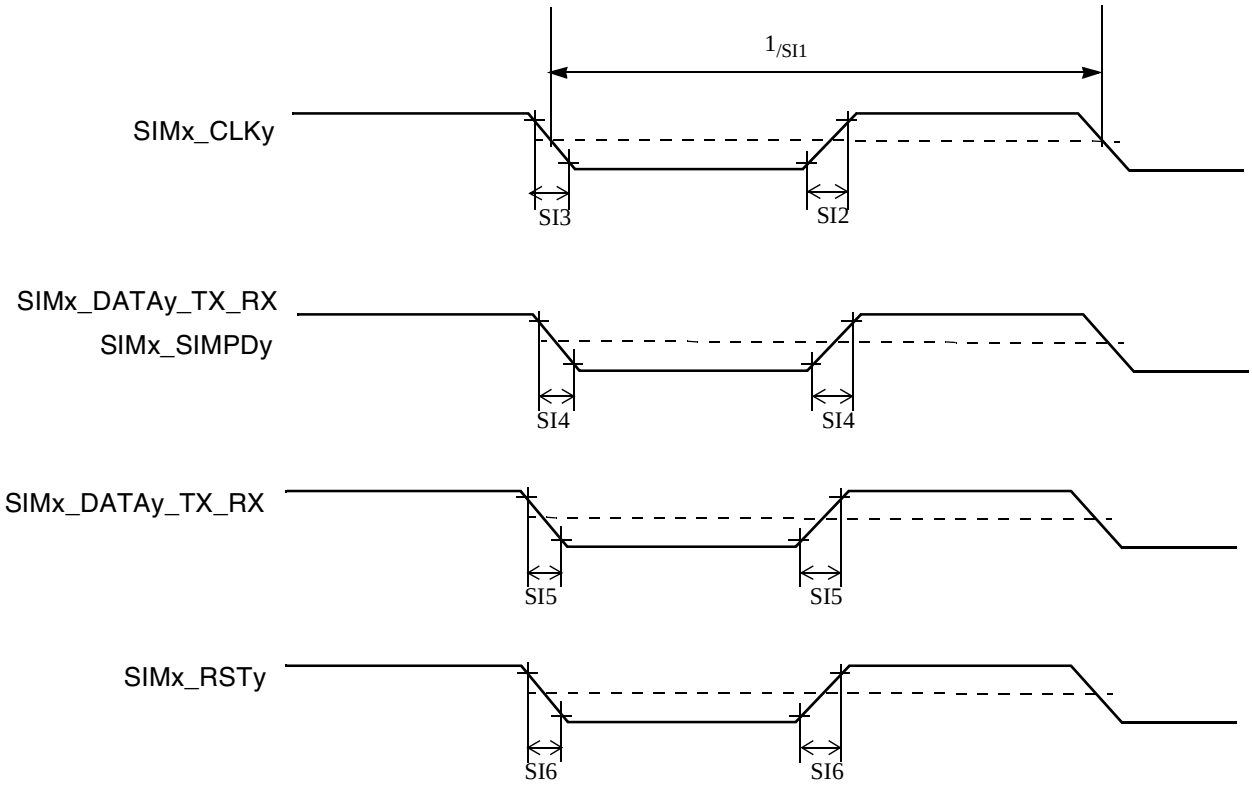

Figure 68. SIM Clock Timing Diagram

Table 74 defines the general timing requirements for the SIM interface.

Table 74. Timing Specifications, High Drive Strength

ID	Parameter	Symbol	Min.	Max.	Unit
SI1	SIM clock frequency (SIMx_CLKy)[1]	S_{freq}	0.01	25	MHz
SI2	SIM clock rise time (SIMx_CLKy)[2]	S_{rise}	—	$0.09 \times (1/S_{freq})$	ns
SI3	SIM clock fall time (SIMx_CLKy)[3]	S_{fall}	—	$0.09 \times (1/S_{freq})$	ns
SI4	SIM input transition time (SIMx_DATAy_RX_TX, SIMx_SIMPDy)	S_{trans}	10	25	ns
SI5	SIM I/O rise time / fall time (SIMx_DATAy_RX_TX)[4]	Tr/Tf	—	1	µs
SI6	SIM RST rise time / fall time (SIMx_RSTy)[5]	Tr/Tf	—	1	µs

1 50% duty cycle clock,
2 With C = 50 pF
3 With C = 50 pF
4 With Cin = 30 pF, Cout = 30 pF,
5 With Cin = 30 pF,

3.7.19.1 UART RS-232 Serial Mode Timing

3.7.19.1.1 UART Transmit Timing in RS-232 Serial Mode

Figure 85 shows the UART transmit timing in RS-232 serial mode, showing only 8 data bits and 1 stop bit. Table 86 describes the timing parameter (UA1) shown in the figure.

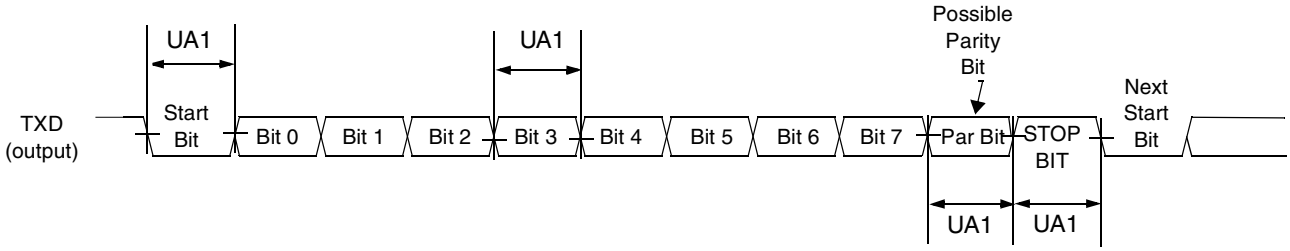

Figure 85. UART RS-232 Serial Mode Transmit Timing Diagram

Table 86. UART RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

3.7.19.1.2 UART Receive Timing in RS-232 Serial Mode

Figure 86 shows the UART receive timing in RS-232 serial mode, showing only 8 data bits and 1 stop bit. Table 87 describes the timing parameter (UA2) shown in the figure.

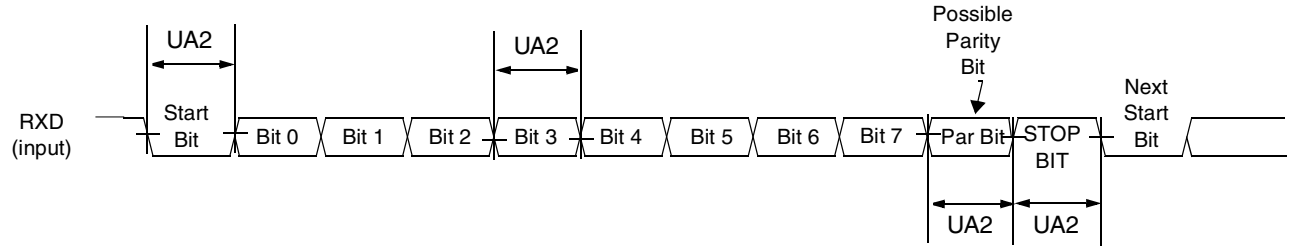

Figure 86. UART RS-232 Serial Mode Receive Timing Diagram

Table 87. UART RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA2	Receive bit time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

3.7.20 USBOTG Timing

This section describes timing for the USB OTG port and host ports. Both serial and parallel interfaces are described.

3.7.20.1 USB Serial Interface Timing

The USB serial transceiver is configurable to four modes supporting four different serial interfaces:

- DAT_SE0 bidirectional, 3-wire mode
- DAT_SE0 unidirectional, 6-wire mode
- VP_VM bidirectional, 4-wire mode
- VP_VM unidirectional, 6-wire mode

The following subsections describe the timings for these four modes.

3.7.20.1.1 DAT_SE0 Bidirectional Mode Timing

Table 90 defines the DAT_SE0 bidirectional mode signals.

Table 90. Signal Definitions—DAT_SE0 Bidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out In	Tx data when USB_TXOE_B is low Differential Rx data when USB_TXOE_B is high
USB_SE0_VM	Out In	SE0 drive when USB_TXOE_B is low SE0 Rx indicator when USB_TXOE_B is high

Figure 89 shows the USB transmit waveform in DAT_SE0 bidirectional mode diagram.

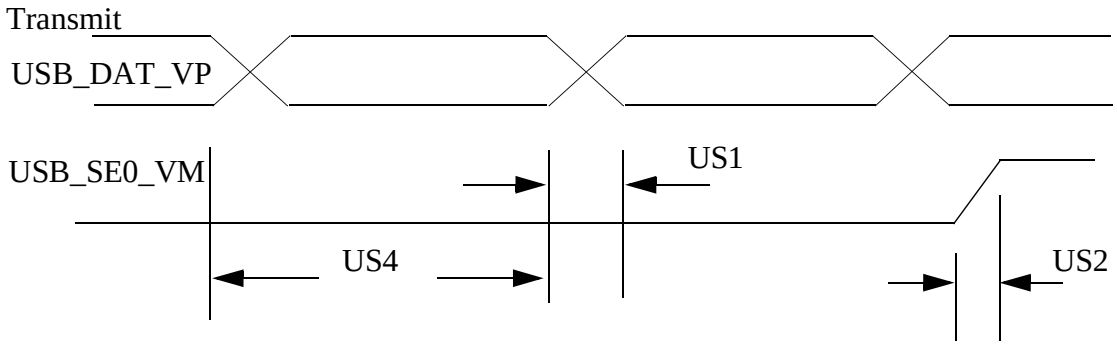

Figure 89. USB Transmit Waveform in DAT_SE0 Bidirectional Mode

Figure 95 shows the USB transmit waveform in VP_VM unidirectional mode diagram.

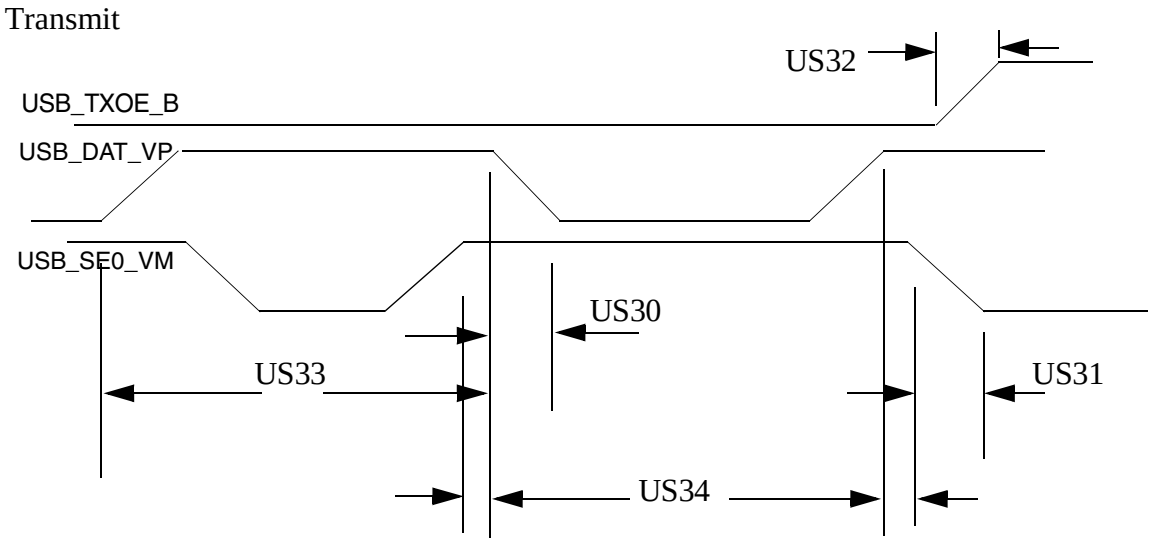

Figure 95. USB Transmit Waveform in VP_VM Unidirectional Mode

Figure 96 shows the USB receive waveform in VP_VM unidirectional mode diagram.

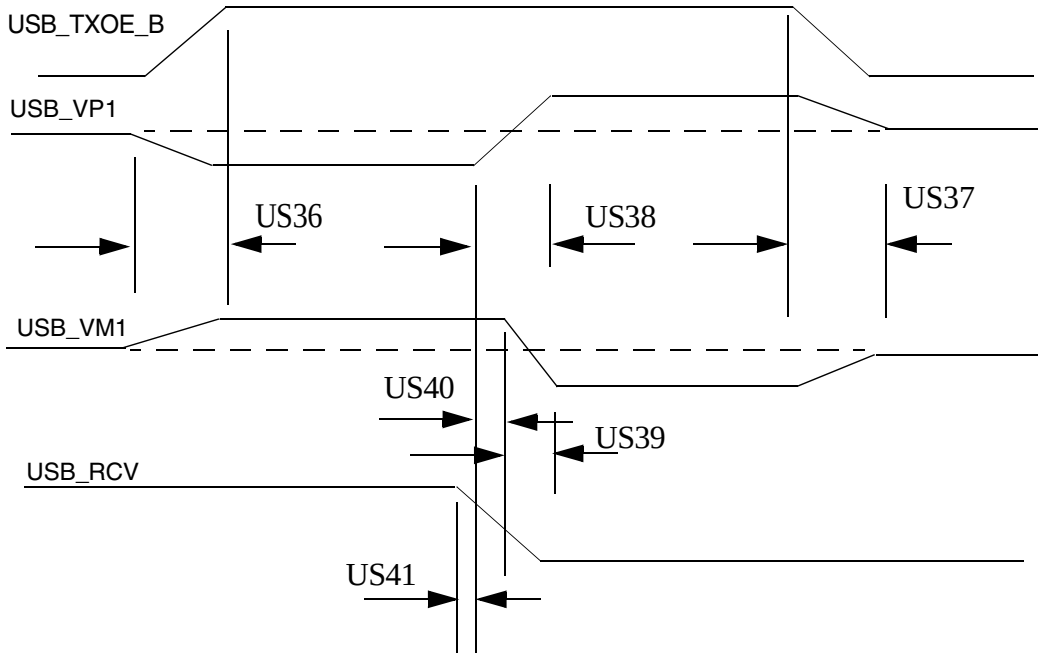

Figure 96. USB Receive Waveform in VP_VM Unidirectional Mode

Table 101. 17×17 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
LD2[2]	W7	LCDC	GPIO	OUTPUT	Low
LD3[2]	U8	LCDC	GPIO	OUTPUT	Low
LD4[2]	Y6	LCDC	GPIO	OUTPUT	Low
LD5[2]	V7	LCDC	GPIO	OUTPUT	Low
LD6[2]	W6	LCDC	GPIO	OUTPUT	Low
LD7[2]	Y5	LCDC	GPIO	OUTPUT	Low
LD8[2]	V6	LCDC	GPIO	OUTPUT	Low
LD9[2]	W5	LCDC	GPIO	OUTPUT	Low
LD10[2]	Y4	LCDC	GPIO	OUTPUT	Low
LD11[2]	Y3	LCDC	GPIO	OUTPUT	Low
LD12[2]	V5	LCDC	GPIO	OUTPUT	Low
LD13[2]	W4	LCDC	GPIO	OUTPUT	Low
LD14[2]	V4	LCDC	GPIO	OUTPUT	Low
LD15[2]	W3	LCDC	GPIO	OUTPUT	Low
HSYNC[2]	U7	LCDC	GPIO	OUTPUT	Low
VSYNC[2]	U6	LCDC	GPIO	OUTPUT	Low
LSCLK[2]	U5	LCDC	GPIO	OUTPUT	Low
OE_ACD[2]	V3	LCDC	GPIO	OUTPUT	Low
CONTRAST	U4	LCDC	GPIO	OUTPUT	Low
PWM[2]	W2	LCDC	GPIO	INPUT	100 KΩ Pull-Down
CSI_D2	F18	CSI	GPIO	INPUT	Keeper
CSI_D3	E19	CSI	GPIO	INPUT	Keeper
CSI_D4	F19	CSI	GPIO	INPUT	Keeper
CSI_D5	G18	CSI	GPIO	INPUT	Keeper
CSI_D6	E20	CSI	GPIO	INPUT	Keeper
CSI_D7	E18	CSI	GPIO	INPUT	Keeper
CSI_D8	G19	CSI	GPIO	INPUT	Keeper
CSI_D9	F20	CSI	GPIO	INPUT	Keeper
CSI_MCLK[2]	H18	CSI	GPIO	OUTPUT	Low
CSI_VSYNC[2]	G20	CSI	GPIO	INPUT	Keeper
CSI_HSYNC[2]	H19	CSI	GPIO	INPUT	Keeper
CSI_PIXCLK[2]	H20	CSI	GPIO	INPUT	Keeper

Table 101. 17×17 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
I2C1_CLK	F17	CSI	GPIO	INPUT	100 KΩ Pull-Up
I2C1_DAT	G17	CSI	GPIO	INPUT	100 KΩ Pull-Up
CSPI1_MOSI	T4	MISC	GPIO	INPUT	100 KΩ Pull-Up
CSPI1_MISO	W1	MISC	GPIO	OUTPUT	Low
CSPI1_SS0	R4	MISC	GPIO	INPUT	100 KΩ Pull-Up
CSPI1_SS1	V2	MISC	GPIO	INPUT	100 KΩ Pull-Up
CSPI1_SCLK	U3	MISC	GPIO	INPUT	100 KΩ Pull-Up
CSPI1_RDY	V1	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART1_RXD	U2	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART1_TXD	U1	MISC	GPIO	OUTPUT	High
UART1_RTS	T3	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART1_CTS	T2	MISC	GPIO	OUTPUT	High
UART2_RXD	P4	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART2_TXD	T1	MISC	GPIO	OUTPUT	High
UART2_RTS	R3	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART2_CTS	R2	MISC	GPIO	INPUT	-
SD1_CMD	K20	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_CLK	M20	SDIO	GPIO	OUTPUT	High
SD1_DATA0	L20	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_DATA1	N20	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_DATA2	M19	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_DATA3	J20	SDIO	GPIO	INPUT	47 KΩ Pull-Up
KPP_ROW0	N4	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_ROW1	R1	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_ROW2	P3	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_ROW3	P2	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL0	P1	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL1	N3	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL2	N2	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL3	N1	MISC	GPIO	INPUT	100 KΩ Pull-Up
FEC_MDC	L1	MISC	GPIO	OUTPUT	Low
FEC_MDIO	L2	MISC	GPIO	INPUT	22 KΩ Pull-Up

Table 103. i.MX25 17×17 Package Ball Map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
U	UART1_TXD	UART1_RXD	CSPI1_SCLK	CONTRAST	LSCLK	VSYNC	HSYNC	LD3	SJC_MOD	NVCC_JTAG	INAUX0	INAUX2	XN	WIPER	NC_BGA_U15	NC_BGA_U16	MPLL_GND	MPLL_VDD	POR_B	UPLL_BYPCLK
V	CSPI1_RDY	CSPI1_SS1	OE_ACD	LD14	LD12	LD8	LD5	LD1	TRSTB	TCK	REF	INAUX1	YP	XP	NC_BGA_V15	NC_BGA_V16	NC_BGA_V17	TEST_MODE	BOOT_MODE0	CLKO
W	CSPI1_MISO	PWM	LD15	LD13	LD9	LD6	LD2	DE_B	TDI	RTCK	NVCC_DRYICE	YN	NVCC_ADC	NC_BGA_W14	OSC24M_GND	OSC24M_VDD	USBPHY2_VSS	USBPHY2_VDD	CLK_SEL	BOOT_MODE1
Y	QGND	NC_BGA_Y2	LD11	LD10	LD7	LD4	LD0	TDO	TMS	OSC32K_XTAL	OSC32K_EXTAL	OSC_BYP	NGND_ADC	NC_BGA_Y14	OSC24M_EXTAL	OSC24M_XTAL	NC_BGA_Y17	USBPHY2_DP	USBPHY2_DM	QGND

Table 105. 12x12 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
UART2_RTS	T2	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART2_CTS	P5	MISC	GPIO	INPUT	-
SD1_CMD	N22	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_CLK	N21	SDIO	GPIO	OUTPUT	High
SD1_DATA0	P22	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_DATA1	R22	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_DATA2	M22	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_DATA3	M21	SDIO	GPIO	INPUT	47 KΩ Pull-Up
KPP_ROW0	R2	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_ROW1	R4	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_ROW2	U1	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_ROW3	P4	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL0	T1	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL1	N5	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL2	P2	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL3	N4	MISC	GPIO	INPUT	100 KΩ Pull-Up
FEC_MDC	P1	MISC	GPIO	OUTPUT	Low
FEC_MDIO	M2	MISC	GPIO	INPUT	22 KΩ Pull-Up
FEC_TDATA0	L2	MISC	GPIO	OUTPUT	High
FEC_TDATA1	M1	MISC	GPIO	OUTPUT	High
FEC_TX_EN	R1	MISC	GPIO	OUTPUT	Low

Table 105. 12x12 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
WIPER	AA17	ADC	ANALOG	ANALOG	-
INAUX0	AA15	ADC	ANALOG	ANALOG	-
INAUX1	W14	ADC	ANALOG	ANALOG	-
INAUX2	AB16	ADC	ANALOG	ANALOG	-

1 The state immediately after reset and before ROM firmware or software has executed.

2 During power-on reset this port acts as input for fuse override signal.

3 During power-on reset this port acts as output for diagnostic signal.

Table 106 lists the 12×12 mm package i.MX25 no connect contact assignments.

Table 106. 12×12 mm Package i.MX25 No Connect Contact Assignments

Signal Name	Contact Assignment
NC_BGA_E4	E4
NC_BGA_L4	L4

4.8 i.MX25 12x12 Package Ball Map

Table 107 shows the i.MX25 12×12 package ball map.

Table 107. i.MX25 12×12 Package Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	QGND	EB0	OE	A14	A16	A18	A22	BCLK	DQM1	SD9	SD10	SD7	SD0	SD3	SD5	SDCKE0	SDBA0	CS3	A1	A0	A4	QGND
B	ECB	QGND	LBA	EB1	A10	A20	A24	SD14	SD12	SD11	SD6	SD2	SD4	QGND	SDWE	CAS	CS2	A2	A5	A7	QGND	A12
C	NFRE_B	CS0																			A11	CS1_D2
D	NFCLE	CS5		CS1	RW	A15	A21	A25	SD15	SD8	DQM0	SD1	SDCLK	SDCLK_B	RAS	SDBA1	A3	A6	A9		A13	CSI_D6
E	NFWE_B	NFALE		NC_BGA_E4	CS4	A17	A19		A23		SD13	SDQS1		SDQS0	NVCC_EMI2		MA10	QGND	A8		CSI_D4	CSI_D8
F	D1	D0		NF_CE0									QGND	QGND	NVCC_EMI2	SDCKE1		QGND	CSI_D3		CSI_D7	CSI_MCLK