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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	347-LFBGA
Supplier Device Package	347-MAPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx257cjn4a

Table 2 shows the functional differences between the different parts in the i.MX25 family.

Table 2. i.MX25 Parts Functional Differences

Features	MCIMX253	MCIMX257	MCIMX258
Core	ARM 926EJ-S	ARM 926EJ-S	ARM 926EJ-S
CPU Speed	400 MHz	400 MHz	400 MHz
L1 I/D Cache	16K I/D	16K I/D	16K I/D
On-chip SRAM	128 KB	128 KB	128 KB
PATA/CE-ATA	Yes	Yes	Yes
LCD Controller	Yes	Yes	Yes
Touchscreen	—	Yes	Yes
CSI	—	Yes	Yes
FlexCAN (2)	—	Yes	Yes
ESAI	—	Yes	Yes
SIM (2)	—	Yes	Yes
Security	—	—	Yes
10/100 Ethernet	Yes	Yes	Yes
HS USB 2.0 OTG + PHY	Yes	Yes	Yes
HS USB 2.0 Host + PHY	Yes	Yes	Yes
12-bit ADC	Yes	Yes	Yes
SD/SDIO/MMC (2)	Yes	Yes	Yes
External Memory Controller	Yes	Yes	Yes
I^2C (3)	Yes	Yes	Yes
SSI/I2S (2)	Yes	Yes	Yes
CSPI (2)	Yes	Yes	Yes
UART (5)	Yes	Yes	Yes

1.2 Block Diagram

Figure 1 shows the simplified interface block diagram.

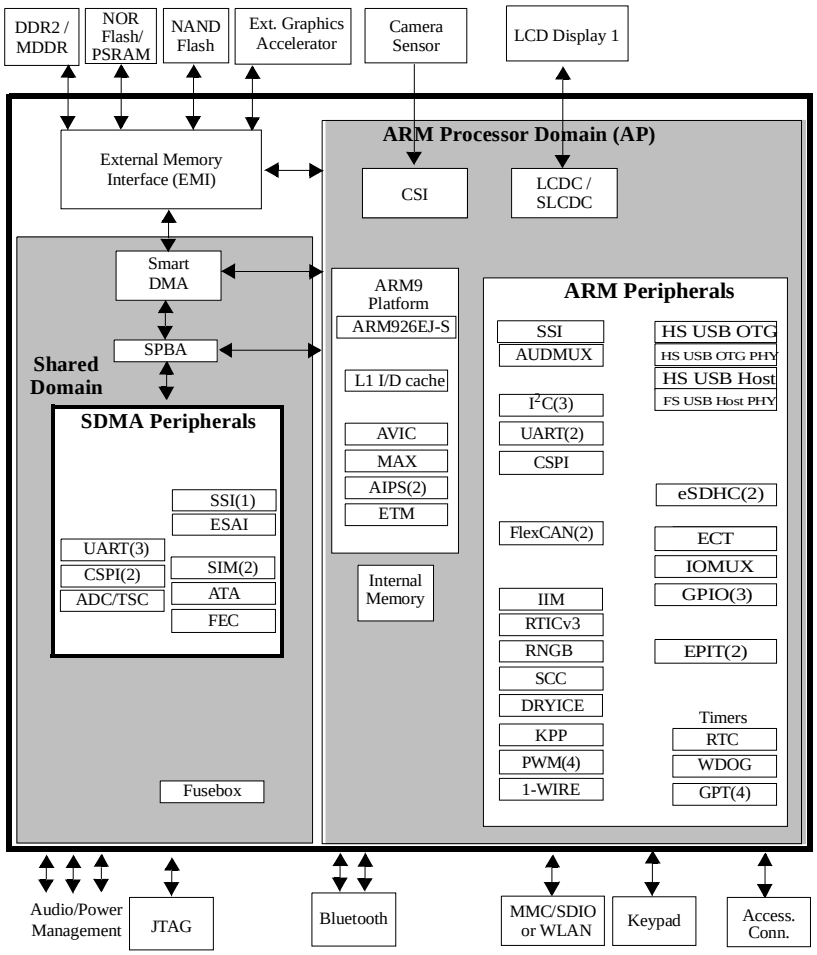

Figure 1. i.MX25 Simplified Interface Block Diagram

NOTE

- The user is advised to connect FUSEVDD to GND except when fuses are programmed, to prevent unintentional blowing of fuses.
- Other power-up sequences may be possible; however, the above sequence has been verified and is recommended.
- There is a 1 ms minimum time between supplies coming up, and a 1 ms minimum time between POR_B assert and de-assert.
- The dV/dT should be no faster than 0.25 V/µs for all power supplies, to avoid triggering ESD circuit.

Figure 2 shows the power-up sequence diagram. After POR_B is asserted, Core VDD and NVDDx can be powered up. After Core VDD and NVDDx are stable, the analog supplies can be powered up.

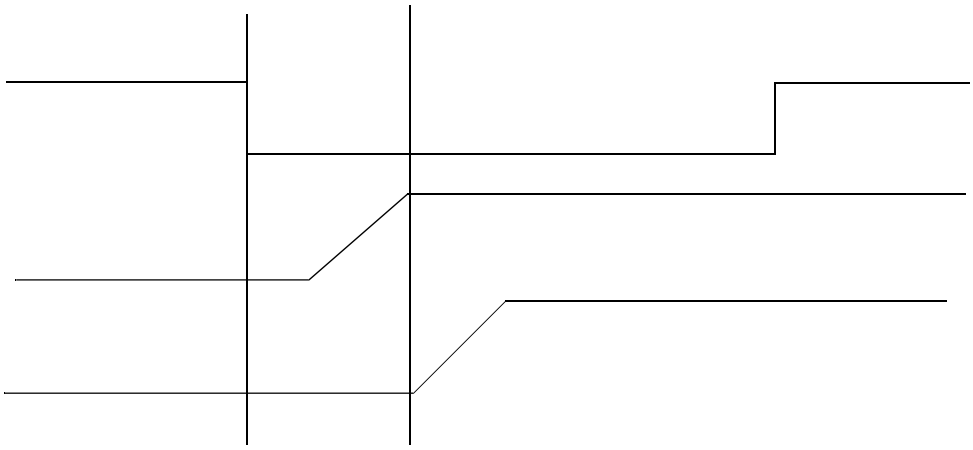

Figure 2. Power-Up Sequence Diagram

3.2.2 Power-Down Sequence

There are no special requirements for the power-down sequence. All power supplies can be shut down at the same time.

3.2.3 SRTC DryIce Power-Up/Down Sequence

In order to guarantee DryIce power-loss protection, including retention of SRTC time data during power down, users must do the following:

- Place a proper capacitor on the NVCC_DRYICE output pin, and
- Implement the below power-up/down sequence

1. Assert power on reset (POR).
2. Turn on NVCC_CRM.
3. Turn on QVDD digital logic domain supplies for not less than 1 ms and not more than 32 ms, after NVCC_CRM reaches 90% of 3.3 V.

Figure 3 shows the load circuit for output. Figure 4 through Figure 6 show the output transition time and propagation waveforms.

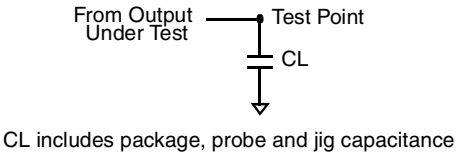

Figure 3. Load Circuit for Output

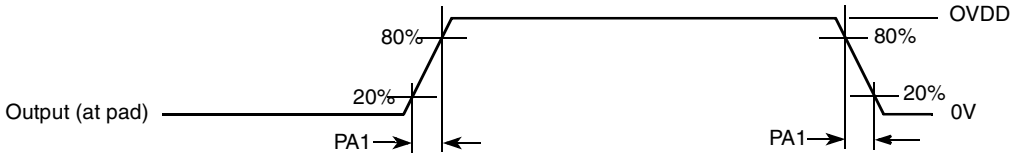

Figure 4. Output Pad Transition Time Waveform

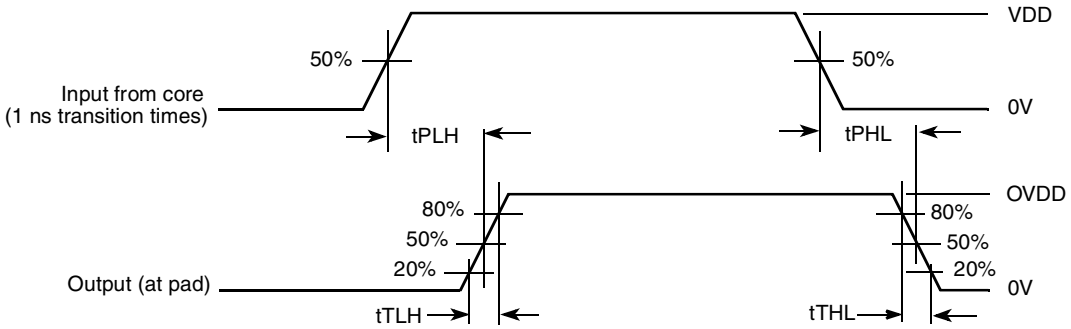

Figure 5. Output Pad Propagation and Transition Time Waveform

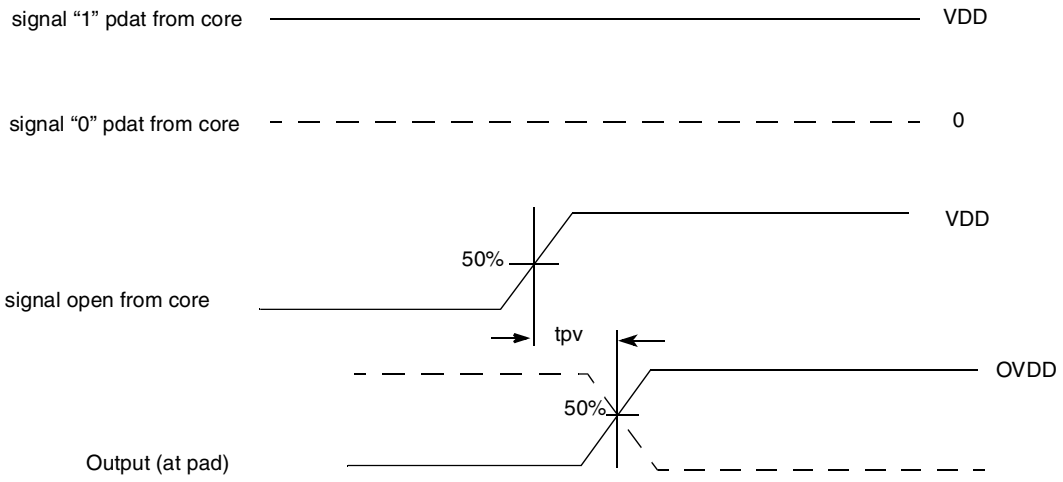

Figure 6. Output Enable to Output Valid

3.6.1 Slow I/O AC Parameters

Table 21 shows the slow I/O AC parameters.

Table 21. Slow I/O AC Parameters

Parameter	Symbol	Test Voltage	Test Capacitance	Min. Rise/Fall	Typ. Rise/Fall	Max. Rise/Fall	Units
Duty cycle	Fduty	—	—	40	—	60	%
Output pad transition times[1] (max. drive)	tpr	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	0.95/0.84 1.58/1.37 2.70/2.50 3.40/3.20	1.36/1.11 2.19/1.77 1.80/1.40 2.80/2.14	2.06/1.60 3.20/2.47 3.01/2.37 4.63/3.38	ns
Output pad transition times[1] (high drive)	tpr	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	1.60/1.39 2.94/2.51 1.85/1.48 2.93/2.37	2.23/1.79 4.05/3.17 2.90/2.17 4.56/3.40	3.26/2.50 5.72/4.27 4.75/3.43 7.33/5.26	
Output pad transition times[1] (standard drive)	tpr	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	3.07/2.62 5.82/4.95 3.04/2.47 5.37/4.40	4.22/3.30 7.94/6.19 4.73/3.50 7.70/8.10	6.03/4.48 11.28/8.28 3.01/2.36 4.63/3.38	
Output pad propagation delay[1] (max. drive), 50%–50%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	1.92/2.1 2.44/2.53 2.05/2.27 2.71/2.84	2.96/2.96 3.7/3.64 3.32/3.67 4.39/4.51	4.47/4.38 5.54/5.31 5.27/5.85 7.00/7.15	ns
Output pad propagation delay[1] (high drive), 50%–50%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	2.35/2.49 3.31/3.43 2.58/2.69 3.62/3.60	3.58/3.61 4.9/4.786 4.17/4.27 5.86/5.61	5.35/5.24 7.19/6.8 6.64/6.74 9.34/8.76	
Output pad propagation delay[1] (standard drive), 50%–50%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	3.39/3.51 5.28/5.35 3.71/3.68 5.52/5.32	5.03/4.89 7.6/7.14 6.03/5.75 8.80/7.96	7.39/6.95 10.97/9.45 9.64/8.97 13.9/11.3	
Output pad propagation delay[1] (max. drive), 40%–60%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	1.942/2.04 2.378/2.48 2.03/2.28 2.59/2.73	2.923/2.95 3.541/3.53 3.19/3.59 4.10/4.33	4.33/4.3 5.29/5.09 4.97/5.64 6.43/6.77	ns
Output pad propagation delay[1] (high drive), 40%–60%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	2.29/2.44 3.05/3.20 2.45/2.62 3.36/3.39	3.42/3.49 4.46/4.45 3.86/4.07 5.34/5.22	5.05/5.02 6.53/6.3 6.02/6.35 8.40/8.08	
Output pad propagation delay[1] (standard drive), 40%–60%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	3.12/3.26 4.60/4.73 3.43/3.46 4.89/4.79	4.58/4.53 6.61/6.32 5.48/5.34 7.75/7.16	6.69/6.42 9.5/8.32 8.65/8.26 12.2/9.97	

3.7.2.1 PIO Mode Timing Parameters

Figure 11 shows a timing diagram for PIO read mode.

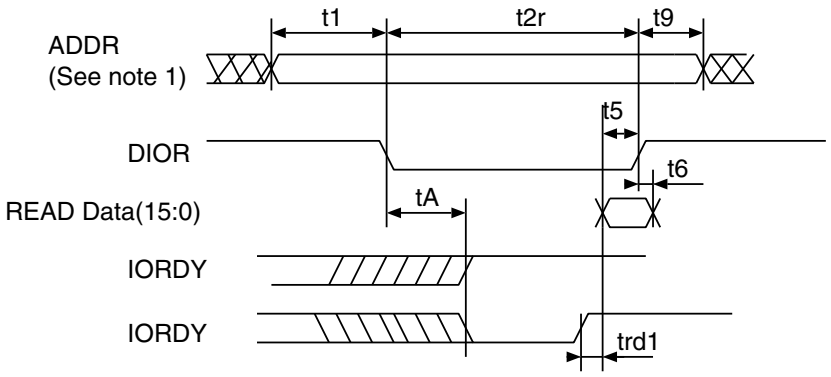

Figure 11. PIO Read Mode Timing

To meet PIO read mode timing requirements, a number of timing parameters must be controlled. Table 36 shows timing parameters and their determining relations, and indicates parameters that can be adjusted to meet required conditions.

Table 36. Timing Parameters for PIO Read Mode

ATA Parameter	PIO Read Mode Timing Parameter[1]	Relation	Adjustable Parameter
t1	t1	t1(min.) = time_1 × T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2r	t2(min.) = time_2r × T – (tskew1 + tskew2 + tskew5)	time_2r
t9	t9	t9(min.) = time_9 × T – (tskew1 + tskew2 + tskew6)	time_9
t5	t5	t5(min.) = tco + tsu + tbuf + tbuf + tcable1 + tcable2	If not met, increase time_2
t6	t6	0	—
tA	tA	tA(min.) = (1.5 + time_ax) × T – (tco + tsui + tcable2 + tcable2 + 2 × tbuf)	time_ax
trd	trd1	trd1(max.) = (–trd) + (tskew3 + tskew4) trd1(min.) = (time_pio_rdx – 0.5) × T – (tsu + thi) (time_pio_rdx – 0.5) × T > tsu + thi + tskew3 + tskew4	time_pio_rdx
t0	—	t0(min.) = (time_1 + time_2 + time_9) × T	time_1, time_2r, time_9

[1] See Figure 11.

Table 46. SDRAM Refresh Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	SDRAM clock low-level width	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD6	Address setup time	tAS	1.8	—	ns
SD7	Address hold time	tAH	1.8	—	ns
SD10	Precharge cycle period[1]	tRP	1	4	clock
SD11	Auto precharge command period[1]	tRC	2	20	clock

[1] SD10 and SD11 are determined by SDRAM controller register settings.

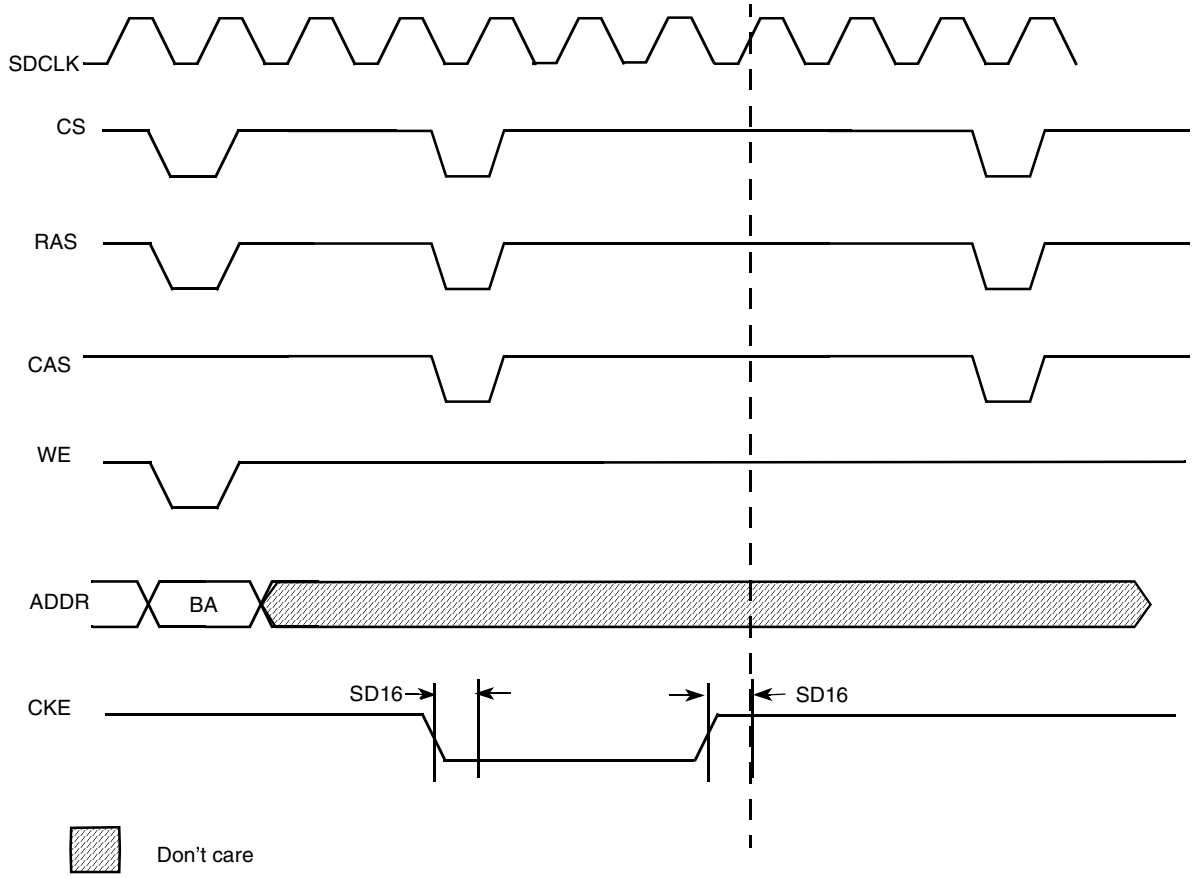

Figure 28. SDRAM Self-Refresh Cycle Timing Diagram

NOTE

The clock continues to run unless CKE is low. Then the clock is stopped in low state.

Table 55. NFC Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = NFC Clock Cycle		Example Timing for NFC Clock ≈ 33 MHz T = 30 ns		Unit
			Min.	Max.	Min.	Max.	
NF5	NF_WP pulse width	tWP	T–1.5 ns		28.5		ns
NF6	NFALE setup time	tALS	T	—	30	—	ns
NF7	NFALE hold time	tALH	T–3.0 ns	—	27	—	ns
NF8	Data setup time	tDS	2T ns	—	60	—	ns
NF9	Data hold time	tDH	T–5.0 ns	—	25	—	ns
NF10	Write cycle time	tWC	2T		60		ns
NF11	NFWE hold time	tWH	T–2.5 ns		27.5		ns
NF12	Ready to NFRE low	tRR	21T–10 ns	—	620	—	ns
NF13	NFRE pulse width	tRP	1.5T	—	45	—	ns
NF14	READ cycle time	tRC	2T	—	60	—	ns
NF15	NFRE high hold time	tREH	0.5T–2.5 ns		12.5	—	ns
NF16	Data setup on read	tDSR	N/A		10	—	ns
NF17	Data hold on read	tDHR	N/A		0	—	ns

1 The Flash clock maximum frequency is 50 MHz.

NOTE

For timing purposes, transition to signal high is defined as 80% of signal value; while signal low is defined as 20% of signal value.

Timing for HCLK is 133 MHz. The internal NFC clock (Flash clock) is approximately 33 MHz (30 ns). All timings are listed according to this NFC clock frequency (multiples of NFC clock phases), except NF16 and NF17, which are not related to the NFC clock.

3.7.6.3 Wireless External Interface Module (WEIM) Timing

Figure 38 depicts the timing of the WEIM module, and Table 56 describes the timing parameters (WE1–WE27) shown in the figure.

All WEIM output control signals may be asserted and negated by internal clock relative to BCLK rising edge or falling edge according to corresponding assertion/negation control fields. Address always begins relative to BCLK falling edge, but may be ended on rising or falling edge in muxed mode according to the control register configuration. Output data begins relative to BCLK rising edge except in muxed mode, where rising or falling edge may be used according to the control register configuration. Input data, ECB and DTACK are all captured relative to BCLK rising edge.

Figure 53 shows the ESAI HCKR timing diagram.

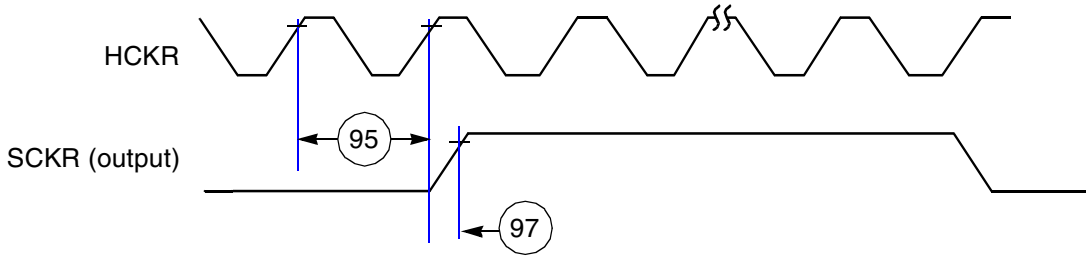

Figure 53. ESAI HCKR Timing

Table 60 describes the general timing requirements for the ESAI module. Table 58 and Table 59 describe respectively the conditions and signals cited in Table 60.

Table 58. ESAI Timing Conditions

Symbol	Significance	Comments
i ck	Internal clock	In the i.MX25, the internal clock frequency is equal to the IP bus frequency (133 MHz)
x ck	External clock	The external clock may be derived from the CRM module or other external clock sources
i ck a	Internal clock, asynchronous mode	In asynchronous mode, SCKT and SCKR are different clocks
i ck s	Internal clock, synchronous mode	In synchronous mode, SCKT and SCKR are the same clock

Table 59. ESAI Signals

Signal Name	Significance
SCKT	Transmit clock
SCKR	Receive clock
FST	Transmit frame sync
HCKT	Transmit high-frequency clock
HCKR	Receive high-frequency clock

Table 60. ESAI General Timing Requirements

No.	Characteristics[1 2]	Symbol	Expression[3]	Min.	Max.	Condition	Unit
62	Clock cycle[4]	t_{SSICC}	$4 \times T_c$ $4 \times T_c$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period For internal clock For external clock	— — —	— $2 \times T_c - 9.0$ $2 \times T_c$	— 6 15	— — —	— — —	ns
64	Clock low period For internal clock For external clock	 — —	 $2 \times T_c - 9.0$ $2 \times T_c$	 6 15	 — —	— —	ns

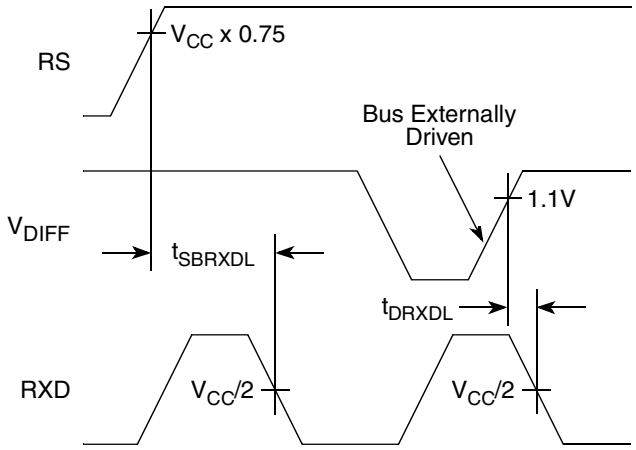

Figure 61. Timing Diagram for FlexCAN Standby Signal

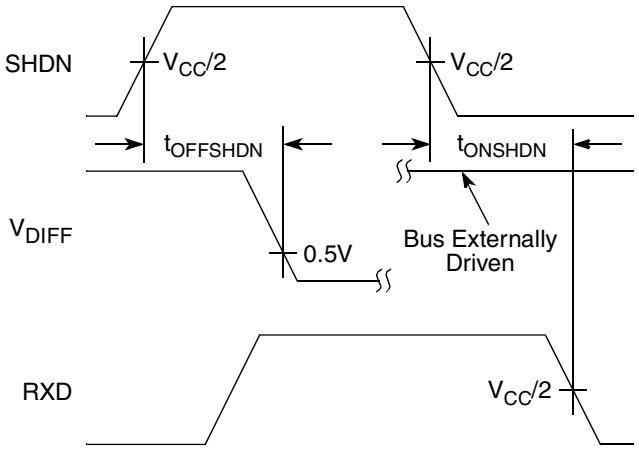

Figure 62. Timing Diagram for FlexCAN Shutdown Signal

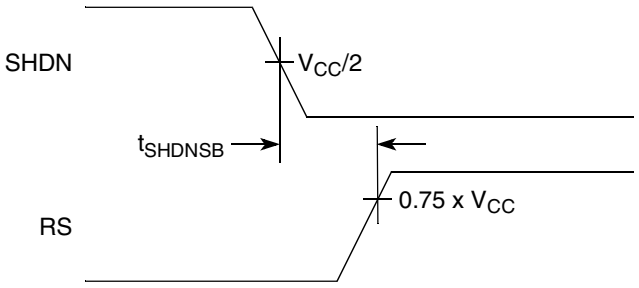

Figure 63. Timing Diagram for FlexCAN Shutdown-to-Standby Signal

Because integer multiples are not possible, taking into account the range of frequencies at which the SoC has to operate, DPLLs work in FOL mode only.

3.7.12 Liquid Crystal Display Controller (LCDC) Timing

Figure 65 and Figure 66 show LCDC timing in non-TFT and TFT mode respectively, and Table 71 and Table 72 list the timing parameters used in the associated figures.

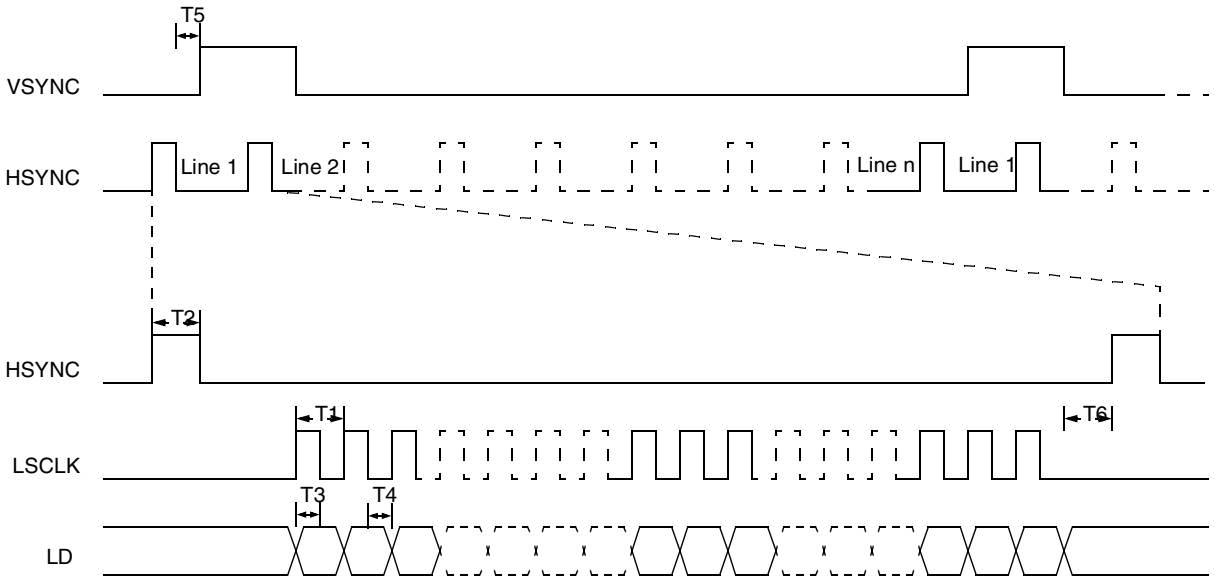

Figure 65. LCDC Non-TFT Mode Timing Diagram

Table 71. LCDC Non-TFT Mode Timing Parameters

ID	Description	Min.	Max.	Unit
T1	Pixel clock period	22.5	1000	ns
T2	HSYNC width	1	—	T[1]
T3	LD setup time	5	—	ns
T4	LD hold time	5	—	ns
T5	Wait between HSYNC and VSYNC rising edge	2	—	T[1]
T6	Wait between last data and HSYNC rising edge	1	—	T[1]

1 T is pixel clock period

- ”Tx” and “Rx” refer, respectively, to the transmit and receive sections of the SSI.
- For internal frame sync operation using external clock, the FS timing is the same as that of Tx data (for example, during AC97 mode of operation).

3.7.18 Touchscreen ADC Electrical Specifications and Timing

This section describes the electrical specifications, operation modes, and timing of the touchscreen ADC.

3.7.18.1 ADC Electrical Specifications

Table 85 shows the electrical specifications for the touchscreen ADC.

Table 85. Touchscreen ADC Electrical Specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
ADC					
Input sampling capacitance (C_S)	No pin/pad capacitance included	—	2	—	pF
Resolution	—		12		bits
Analog Bias					
Resistance value between *ref* and *agndref*	—	—	1.6	—	kΩ
Timing Characteristics					
Sampling rate (fs)	—	—	—	125	kHz
Internal ADC/TSC clock frequency	—	—	—	1.75	MHz
Multiplexed inputs	—		8		—
Data latency	—		12.5		clk cycles
Power-up time[1]	—		14		clk cycles
clk falling edge to sampling delay (tsd)	—	2	5	8	ns
soc input setup time before clk rising edge (tsocst)	—	0.5	1	3	ns
soc input hold time after clk rising edge (tsochld)	—	2	3	6	ns
eoc delay after clk rise edge (teoc)	With a 250 pF load	2	7	10	ns
Valid data out delay after eoc rise edge (tdata)	With a 250 pF load	5	8	13	ns
Power Supply Requirements					
Current consumption[2] NVCC_ADC QV_{DD}	—	—	—	2.1 0.5	mA mA

Figure 83 shows the timing for ADC normal operation.

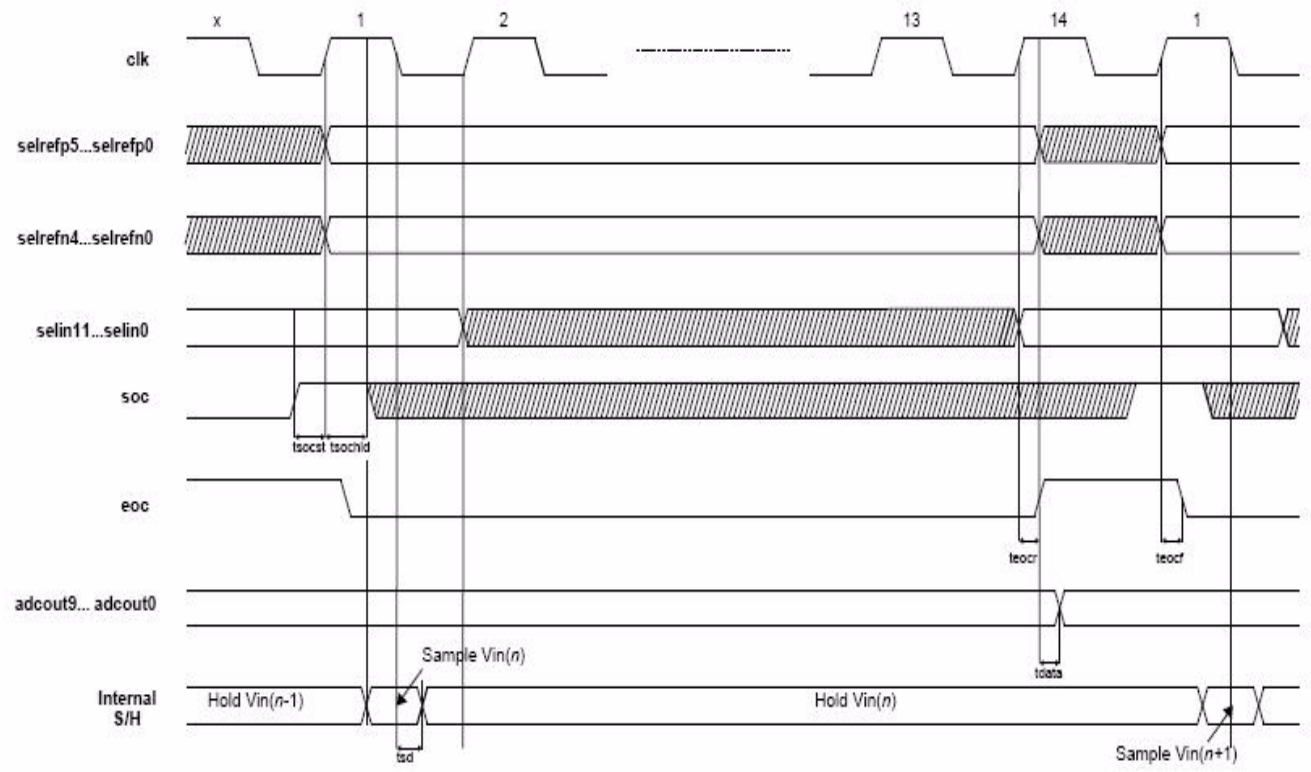

Figure 83. Timing for ADC Normal Operation

When the ADC is used so that the idle clock cycles occur between conversions (due to the negation of *soc*), the *selin* inputs must be stable at least 1 clock cycle before the clock's rising edge where the *soc* signal is latched. Also, *selrefp* and *selrefn* must be stable by the time the *soc* signal is latched. These conditions are met if *enadc=1* and *reset=0* throughout ADC operation, including the idle cycles. If the conditions are not met, or if power is lost during ADC operation, then a new start-up sequence is required for ADC to become operational again.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

3.7.20 USBOTG Timing

This section describes timing for the USB OTG port and host ports. Both serial and parallel interfaces are described.

3.7.20.1 USB Serial Interface Timing

The USB serial transceiver is configurable to four modes supporting four different serial interfaces:

- DAT_SE0 bidirectional, 3-wire mode
- DAT_SE0 unidirectional, 6-wire mode
- VP_VM bidirectional, 4-wire mode
- VP_VM unidirectional, 6-wire mode

The following subsections describe the timings for these four modes.

3.7.20.1.1 DAT_SE0 Bidirectional Mode Timing

Table 90 defines the DAT_SE0 bidirectional mode signals.

Table 90. Signal Definitions—DAT_SE0 Bidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out In	Tx data when USB_TXOE_B is low Differential Rx data when USB_TXOE_B is high
USB_SE0_VM	Out In	SE0 drive when USB_TXOE_B is low SE0 Rx indicator when USB_TXOE_B is high

Figure 89 shows the USB transmit waveform in DAT_SE0 bidirectional mode diagram.

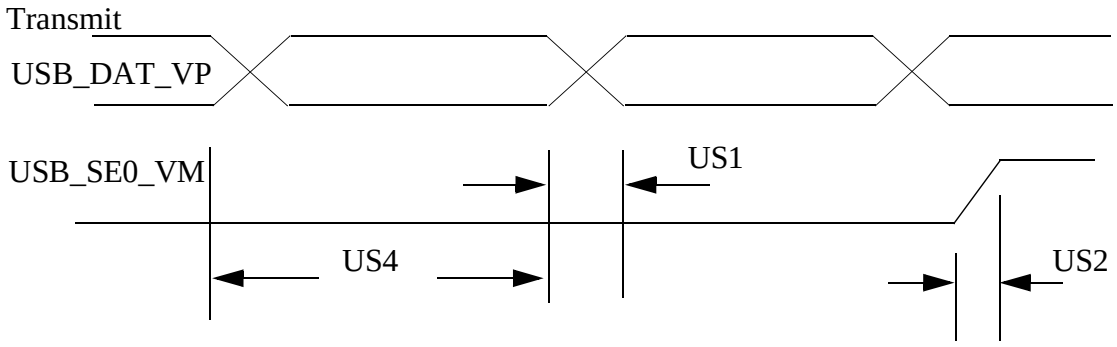

Figure 89. USB Transmit Waveform in DAT_SE0 Bidirectional Mode

Figure 90 shows the USB receive waveform in DAT_SE0 bidirectional mode diagram.

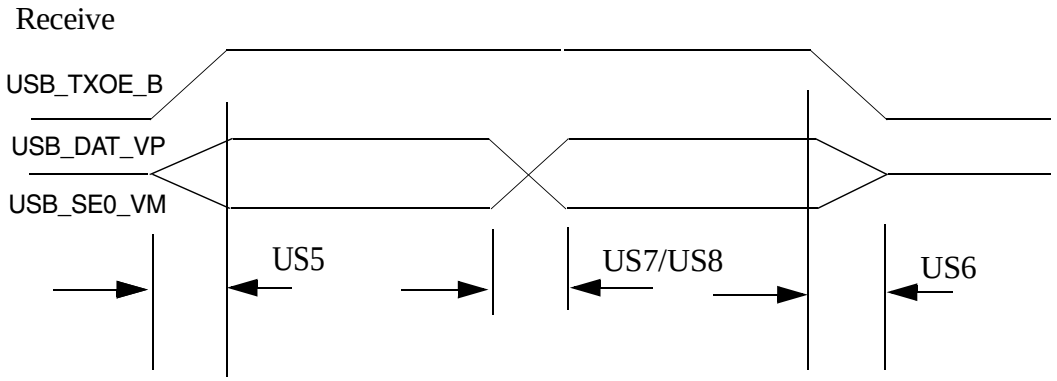

Figure 90. USB Receive Waveform in DAT_SE0 Bidirectional Mode

Table 91 shows the OTG port timing specification in DAT_SE0 bidirectional mode.

Table 91. OTG Port Timing Specification in DAT_SE0 Bidirectional Mode

No.	Parameter	Signal Name	Direction	Min.	Max.	Unit	Conditions/ Reference Signal
US1	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US2	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US3	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US4	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US5	Enable Delay	USB_DAT_VP USB_SE0_VM	In	—	8.0	ns	USB_TXOE_B
US6	Disable Delay	USB_DAT_VP USB_SE0_VM	In	—	10.0	ns	USB_TXOE_B
US7	Rx rise/fall time	USB_DAT_VP	In	—	3.0	ns	35 pF
US8	Rx rise/fall time	USB_SE0_VM	In	—	3.0	ns	35 pF

3.7.20.1.2 DAT_SE0 Unidirectional Mode Timing

Table 92 defines the DAT_SE0 unidirectional mode signals.

Table 92. Signal Definitions—DAT_SE0 Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	Tx data when USB_TXOE_B is low
USB_SE0_VM	Out	SE0 drive when USB_TXOE_B is low
USB_VP1	In	Buffered data on DP when USB_TXOE_B is high
USB_VM1	In	Buffered data on DM when USB_TXOE_B is high
USB_RCV	In	Differential Rx data when USB_TXOE_B is high

Table 97 shows the timing specifications for USB in VP_VM unidirectional mode.

Table 97. USB Timing Specifications in VP_VM Unidirectional Mode

No.	Parameter	Signal	Direction	Min.	Max.	Unit	Conditions/ Reference Signal
US30	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US31	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US32	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US33	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US34	Tx high overlap	USB_SE0_VM	Out	0.0	—	ns	USB_DAT_VP
US35	Tx low overlap	USB_SE0_VM	Out	—	0.0	ns	USB_DAT_VP
US36	Enable delay	USB_DAT_VP USB_SE0_VM	In	—	8.0	ns	USB_TXOE_B
US37	Disable delay	USB_DAT_VP USB_SE0_VM	In	—	10.0	ns	USB_TXOE_B
US38	Rx rise/fall time	USB_VP1	In	—	3.0	ns	35 pF
US39	Rx rise/fall time	USB_VM1	In	—	3.0	ns	35 pF
US40	Rx skew	USB_VP1	Out	–4.0	+4.0	ns	USB_SE0_VM
US41	Rx skew	USB_RCV	Out	–6.0	+2.0	ns	USB_DAT_VP

3.7.20.2 USB Parallel Interface Timing

Table 98 defines the USB parallel interface signals.

Table 98. Signal Definitions for USB Parallel Interface

Name	Direction	Signal Description
USB_Clk	In	Interface clock—All interface signals are synchronous to USB_Clk
USB_Data[7:0]	I/O	Bidirectional data bus, driven low by the link during idle—Bus ownership is determined by the direction
USB_Dir	In	Direction—Control the direction of the data bus
USB_Stp	Out	Stop—The link asserts this signal for one clock cycle to stop the data stream currently on the bus
USB_Nxt	In	Next—The PHY asserts this signal to throttle the data

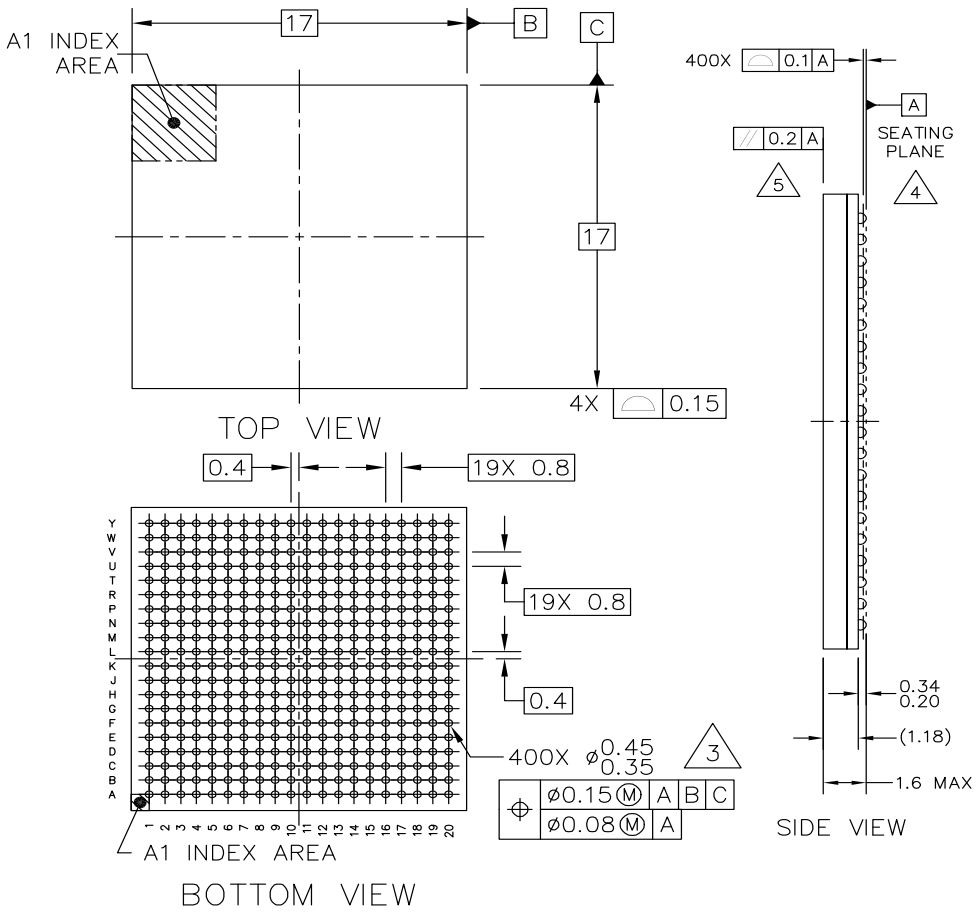

Figure 98. 17×17 i.MX25 Production Package

4.2 Ground, Power, Sense, and Reference Contact Assignments Case 17x17 mm, 0.8 mm Pitch

Table 100 shows the 17×17 mm package ground, power, sense, and reference contact assignments.

Table 100. 17×17 mm Package Ground, Power Sense, and Reference Contact Assignments

Contact Name	Contact Assignment
BATT_VDD	P10
FUSE_VDD	T17
MPLL_GND	U17
MPLL_VDD	U18
NGND_ADC	Y13
NVCC_ADC	W13
NVCC_CRM	N14
NVCC_CSI	J13, J14

Table 101. 17×17 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
FEC_TDATA0	L3	MISC	GPIO	OUTPUT	High
FEC_TDATA1	J4	MISC	GPIO	OUTPUT	High
FEC_TX_EN	M2	MISC	GPIO	OUTPUT	Low
FEC_RDATA0	M1	MISC	GPIO	INPUT	100 KΩ Pull-Down
FEC_RDATA1	M4	MISC	GPIO	INPUT	100 KΩ Pull-Down
FEC_RX_DV	M3	MISC	GPIO	INPUT	100 KΩ Pull-Down
FEC_TX_CLK	L4	MISC	GPIO	INPUT	100 KΩ Pull-Down
RTCK	W10	JTAG	GPIO	OUTPUT	Low
TCK	V10	JTAG	GPIO	INPUT	100 KΩ Pull-Down
TMS	Y9	JTAG	GPIO	INPUT	47 KΩ Pull-Up
TDI	W9	JTAG	GPIO	INPUT	47 KΩ Pull-Up
TDO	Y8	JTAG	GPIO	INPUT	-
TRSTB	V9	JTAG	GPIO	INPUT	47 KΩ Pull-Up
DE_B	W8	JTAG	GPIO	INPUT	47 KΩ Pull-Up
SJC_MOD	U9	JTAG	GPIO	INPUT	100 KΩ Pull-Up
USBPHY1_VBUS	K17	USBPHY1	ANALOG	ANALOG	-
USBPHY1_DP	L18	USBPHY1	ANALOG	ANALOG	-
USBPHY1_DM	K18	USBPHY1	ANALOG	ANALOG	-
USBPHY1_UID	J18	USBPHY1	ANALOG	ANALOG	-
USBPHY1_RREF	L17	USBPHY1_BIAS	ANALOG	ANALOG	-
USBPHY2_DM	Y19	USBPHY2	ANALOG	ANALOG	-
USBPHY2_DP	Y18	USBPHY2	ANALOG	ANALOG	-
GPIO_A	N19	CRM	GPIO	INPUT	-
GPIO_B	N18	CRM	GPIO	INPUT	100 KΩ Pull-Down
GPIO_C	P17	CRM	GPIO	INPUT	100 KΩ Pull-Down
GPIO_D	P19	CRM	GPIO	INPUT	-
GPIO_E	P18	CRM	GPIO	INPUT	100 KΩ Pull-Up
GPIO_F	R19	CRM	GPIO	INPUT	-
EXT_ARMCLK	R20	CRM	GPIO	INPUT	-
UPLL_BYPCLK	U20	CRM	GPIO	INPUT	-
VSTBY_REQ	R18	CRM	GPIO	OUTPUT	Low
VSTBY_ACK[3]	T20	CRM	GPIO	OUTPUT	Low

Table 101. 17×17 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
POWER_FAIL	T19	CRM	GPIO	INPUT	100 KΩ Pull-Down
RESET_B	T18	CRM	GPIO	INPUT	100 KΩ Pull-Up
POR_B	U19	CRM	GPIO	INPUT	100 KΩ Pull-Up
CLKO	V20	CRM	GPIO	OUTPUT	Low
BOOT_MODE0[2]	V19	CRM	GPIO	INPUT	100 KΩ Pull-Down
BOOT_MODE1[2]	W20	CRM	GPIO	INPUT	100 KΩ Pull-Down
CLK_SEL	W19	CRM	GPIO	INPUT	100 KΩ Pull-Down
TEST_MODE	V18	CRM	GPIO	INPUT	100 KΩ Pull-Down
OSC24M_EXTAL	Y15	OSC24M	ANALOG	ANALOG	-
OSC24M_XTAL	Y16	OSC24M	ANALOG	ANALOG	-
OSC32K_EXTAL	Y11	DRYICE	ANALOG	ANALOG	-
OSC32K_XTAL	Y10	DRYICE	ANALOG	ANALOG	-
TAMPER_A	N10	DRYICE	ANALOG	ANALOG	-
TAMPER_B	N11	DRYICE	ANALOG	ANALOG	-
MESH_C	P11	DRYICE	ANALOG	ANALOG	-
MESH_D	P12	DRYICE	ANALOG	ANALOG	-
OSC_BYP	Y12	DRYICE	ANALOG	ANALOG	-
XP	V14	ADC	ANALOG	ANALOG	-
XN	U13	ADC	ANALOG	ANALOG	-
YP	V13	ADC	ANALOG	ANALOG	-
YN	W12	ADC	ANALOG	ANALOG	-
WIPER	U14	ADC	ANALOG	ANALOG	-
INAUX0	U11	ADC	ANALOG	ANALOG	-
INAUX1	V12	ADC	ANALOG	ANALOG	-
INAUX2	U12	ADC	ANALOG	ANALOG	-

1 The state immediately after reset and before ROM firmware or software has executed.

2 During power-on reset this port acts as input for fuse override signal.

3 During power-on reset this port acts as output for diagnostic signal.

Table 105. 12x12 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
WIPER	AA17	ADC	ANALOG	ANALOG	-
INAUX0	AA15	ADC	ANALOG	ANALOG	-
INAUX1	W14	ADC	ANALOG	ANALOG	-
INAUX2	AB16	ADC	ANALOG	ANALOG	-

1 The state immediately after reset and before ROM firmware or software has executed.

2 During power-on reset this port acts as input for fuse override signal.

3 During power-on reset this port acts as output for diagnostic signal.

Table 106 lists the 12×12 mm package i.MX25 no connect contact assignments.

Table 106. 12×12 mm Package i.MX25 No Connect Contact Assignments

Signal Name	Contact Assignment
NC_BGA_E4	E4
NC_BGA_L4	L4

4.8 i.MX25 12x12 Package Ball Map

Table 107 shows the i.MX25 12×12 package ball map.

Table 107. i.MX25 12×12 Package Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	QGND	EB0	OE	A14	A16	A18	A22	BCLK	DQM1	SD9	SD10	SD7	SD0	SD3	SD5	SDCKE0	SDBA0	CS3	A1	A0	A4	QGND
B	ECB	QGND	LBA	EB1	A10	A20	A24	SD14	SD12	SD11	SD6	SD2	SD4	QGND	SDWE	CAS	CS2	A2	A5	A7	QGND	A12
C	NFRE_B	CS0																			A11	CS1_D2
D	NFCLE	CS5		CS1	RW	A15	A21	A25	SD15	SD8	DQM0	SD1	SDCLK	SDCLK_B	RAS	SDBA1	A3	A6	A9		A13	CSI_D6
E	NFWE_B	NFALE		NC_BGA_E4	CS4	A17	A19		A23		SD13	SDQS1		SDQS0	NVCC_EMI2		MA10	QGND	A8		CSI_D4	CSI_D8
F	D1	D0		NF_CE0									QGND	QGND	NVCC_EMI2	SDCKE1		QGND	CSI_D3		CSI_D7	CSI_MCLK