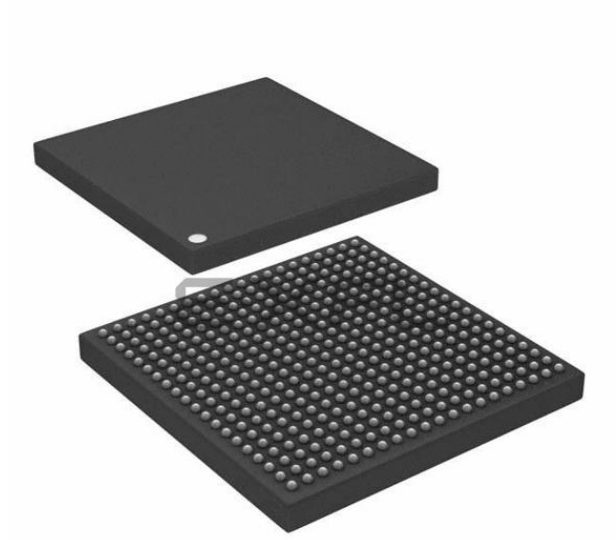

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-20°C ~ 70°C (TA)
Security Features	-
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx257djm4

Features of the i.MX25 processor include the following:

- Advanced power management—The heart of the device is a level of power management throughout the IC that enables the multimedia features and peripherals to achieve minimum system power consumption in active and various low-power modes. Power management techniques allow the designer to deliver a feature-rich product that requires levels of power far lower than typical industry expectations.
- Multimedia powerhouse—The multimedia performance of the i.MX25 processor is boosted by a 16 KB L1 instruction and data cache system and further enhanced by an LCD controller (with alpha blending), a CMOS image sensor interface, an A/D controller (integrated touchscreen controller), and a programmable Smart DMA (SDMA) controller.
- 128 Kbytes on-chip SRAM—The additional 128 Kbyte on-chip SRAM makes the device ideal for eliminating external RAM in applications with small footprint RTOS. The on-chip SRAM allows the designer to enable an ultra low power LCD refresh.
- Interface flexibility—The device interface supports connection to all common types of external memories: MobileDDR, DDR, DDR2, NOR Flash, PSRAM, SDRAM and SRAM, NAND Flash, and managed NAND.
- Increased security—Because the need for advanced security for tethered and untethered devices continues to increase, the i.MX25 processor delivers hardware-enabled security features that enable secure e-commerce, Digital Rights Management (DRM), information encryption, robust tamper detection, secure boot, and secure software downloads.
- On-chip PHY—The device includes an HS USB OTG PHY and FS USB HOST PHY.
- Fast Ethernet—For rapid external communication, a Fast Ethernet Controller (FEC) is included.
- i.MX25 only supports Little Endian mode.

Table 14. iMX25 Reduced Power Mode Current Consumption

Power Group	Power Supply	Voltage Setting	Typical Current Consumption
BAT_VDD	BAT_VDD	1.15 V	9.95 µA
		1.55 V	12.6 µA

3.2 Supply Power-Up/Power-Down Requirements and Restrictions

Any i.MX25 board design must comply with the power-up and power-down sequence guidelines given in this section to ensure reliable operation of the device. Recommended power-up and power-down sequences are given in the following subsections.

CAUTION

Deviations from the guidelines in this section may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the i.MX25 (worst-case scenario)

NOTE

For security applications, the coin battery must be connected during both power-up and power-down sequences to ensure that security keys are not unintentionally erased.

3.2.1 Power-Up Sequence

For those users that are not using DryIce/SRTC, the following power-up sequence is recommended:

1. Assert power on reset (POR).
2. Turn on QVDD digital logic domain supplies.
3. Turn on NVCCx digital I/O power supplies after QVDD is stable.
4. Turn on all other analog power supplies, including USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD, USBPHY1_VDDA, USBPHY2_VDD, OSC24M_VDD, MPPLL_VDD, UPLL_VDD, NVCC_ADC, and FUSEVDD (FUSEVDD is tied to GND if fuses are not programmed), after all NVCCx digital I/O supplies are stable.
5. Negate the POR signal.

Figure 9 and Figure 10 show write 1 and read sequence timing, respectively. Table 34 describes the timing parameters (OW7–OW8) that are shown in the figure.

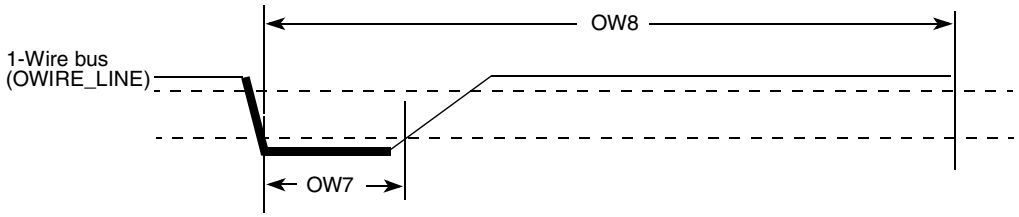

Figure 9. Write 1 Sequence Timing Diagram

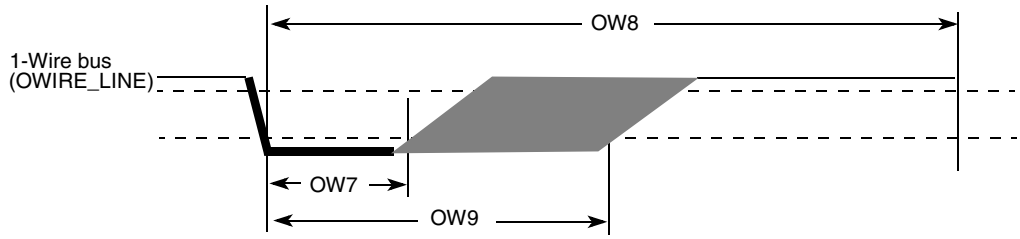

Figure 10. Read Sequence Timing Diagram

Table 34. WR1 /RD Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW7	Write 1 / read low time	t_{LOW1}	1	5	15	µs
OW8	Transmission time slot	t_{SLOT}	60	117	120	µs
OW9	Release time	$t_{RELEASE}$	15	—	45	µs

3.7.2 ATA Timing Parameters

Table 35 shows parameters used to specify the ATA timing. These parameters depend on the implementation of the ATA interface on silicon, the bus buffer used, the cable delay and cable skew.

Table 35. Timing Parameters

Name	Description	Value/Contributing Factor
T	Bus clock period	Peripheral clock frequency
ti_ds	Set-up time **ata_data** to **ata_iordy** edge (UDMA-in only) UDMA0 UDMA1 UDMA2,UDMA3 UDMA4 UDMA5	 15 ns 10 ns 7 ns 5 ns 4 ns
ti_dh	Hold time ata_iordy edge to ata_data (UDMA-in only) UDMA0,UDMA1,UDMA2,UDMA3,UDMA4 UDMA5	 5.0 ns 4.6 ns
tco	Propagation delay bus clock L-to-H to ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data, ata_buffer_en	12.0 ns
tsu	Set-up time **ata_data** to bus clock L-to-H	8.5 ns
tsui	Set-up time **ata_iordy** to bus clock H-to-L	8.5 ns
thi	Hold time **ata_iordy** to bus clock H-to-L	2.5 ns
tskew1	Maximum difference in propagation delay bus clock L-to-H to any of the following signals **ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data** (write), **ata_buffer_en**	7 ns
tskew2	Maximum difference in buffer propagation delay for any of the following signals **ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data** (write), **ata_buffer_en**	Transceiver
tskew3	Maximum difference in buffer propagation delay for any of the following signals **ata_iordy, ata_data** (read)	Transceiver
tbuf	Maximum buffer propagation delay	Transceiver
tcable1	cable propagation delay for **ata_data**	Cable
tcable2	cable propagation delay for control signals **ata_dior**, **ata_diow**, **ata_iordy**, **ata_dmack**	Cable
tskew4	Maximum difference in cable propagation delay between **ata_iordy** and **ata_data** (read)	Cable
tskew5	Maximum difference in cable propagation delay between (**ata_dior**, **ata_diow**, **ata_dmack**) and **ata_cs0**, **ata_cs1**, **ata_da2**, **ata_da1**, **ata_da0**, **ata_data**(write)	Cable
tskew6	Maximum difference in cable propagation delay without accounting for ground bounce	Cable

3.7.5 Configurable Serial Peripheral Interface (CSPI) Timing

Figure 23 and Figure 24 provide CSPI master and slave mode timing diagrams, respectively. Table 43 describes the timing parameters (t1–t14) that are shown in the figures. The values shown in timing diagrams were tested using a worst-case core voltage of 1.1 V, slow pad voltage of 2.68 V, and fast pad voltage of 1.65 V.

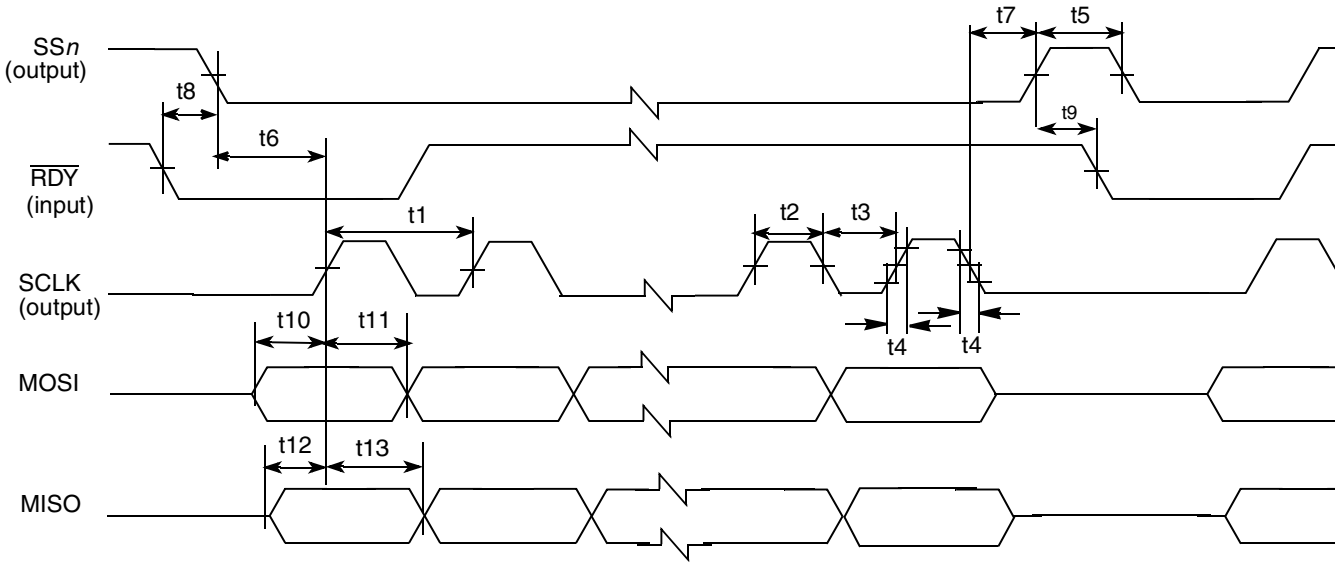

Figure 23. CSPI Master Mode Timing Diagram

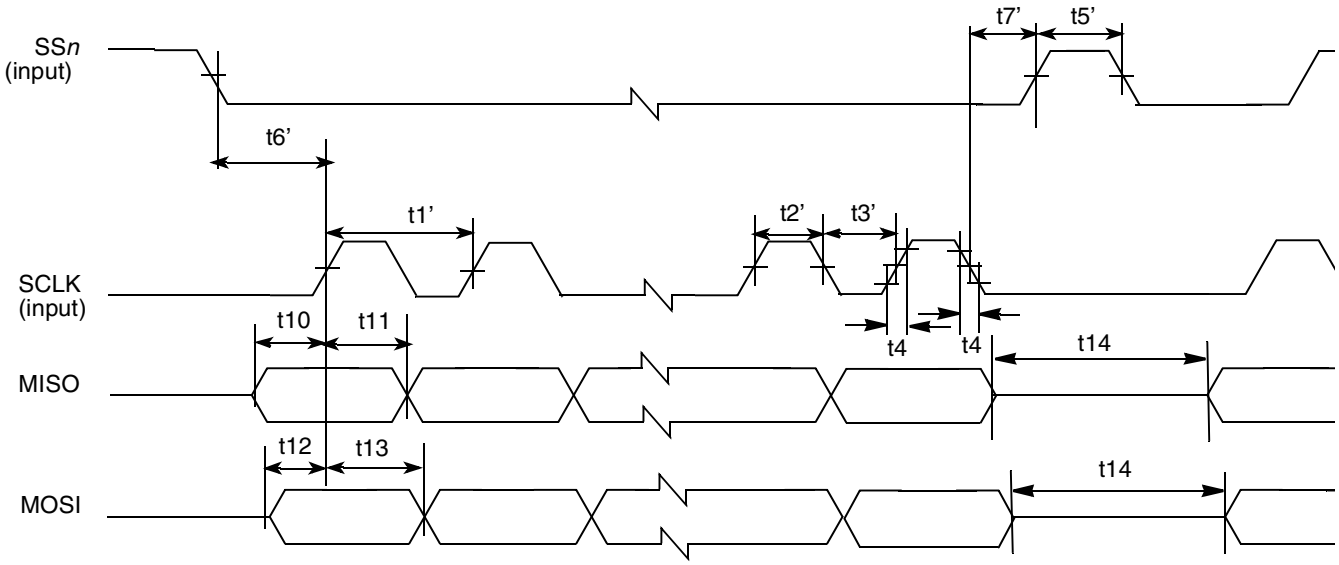

Figure 24. CSPI Slave Mode Timing Diagram

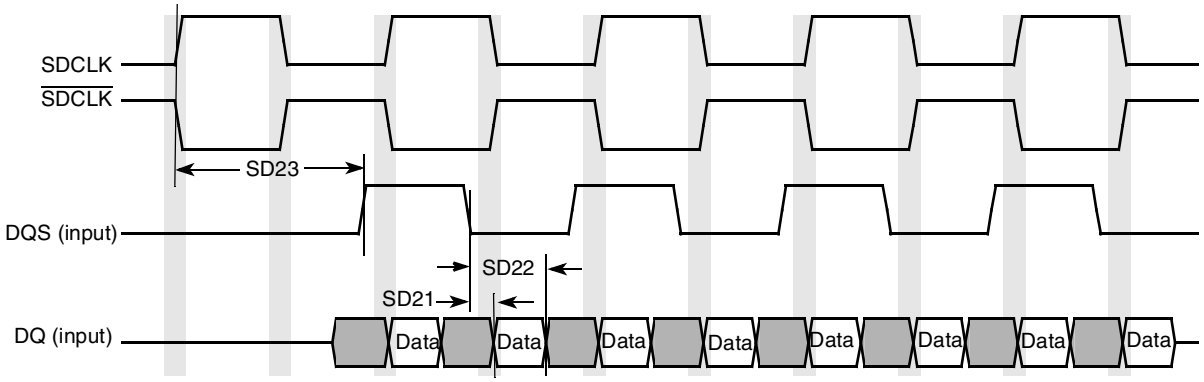

Figure 30. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 49. Mobile DDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD21	DQS – DQ Skew (defines the data valid window in read cycles related to DQS)	tDQSQ	—	0.85	ns
SD22	DQS DQ HOLD time from DQS	tQH	2.3	—	ns
SD23	DQS output access time from SDCLK posedge	tDQSCK	—	6.7	ns

Table 50. DDR2 SDRAM Timing Parameter Table (continued)

ID	Parameter	Symbol	DDR2-400		Unit
			Min.	Max.	
DDR4	CS, RAS, CAS, CKE, WE setup time	t_{IS}	1.2	—	ns
DDR5	CS, RAS, CAS, CKE, WE hold time	t_{IH}	1.2	—	ns
DDR6	Address output setup time	t_{IS}	1.2	—	ns
DDR7	Address output hold time	t_{IH}	0.475	—	ns

Table 50 shows values for a command/address slew rate of 1 V/ns and an SDCLK, SDCLK_B differential slew rate of 2 V/ns. Table 51 shows additional values for DDR2-400 and DDR2-533.

Table 51. tIS, tIH Derating Values for DDR2-400, DDR2-533

Command/ Address Slew Rate (V/Ns)	CK, CK Differential Slew Rate						Units
	2.0 V/ns		1.5 V/ns		1.0 V/ns		
	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	
4.0	+187	+94	+217	+124	+247	+154	ps
3.5	+179	+89	+209	+119	+239	+149	ps
3.0	+167	+83	+197	+113	+227	+143	ps
2.5	+150	+75	+180	+105	+210	+135	ps
2.0	+125	+45	+155	+75	+185	+105	ps
1.5	+83	+21	+113	+51	+143	+81	ps
1.0	0	0	+30	+30	+60	+60	ps
0.9	–11	–14	+19	+16	+49	+46	ps
0.8	–25	–31	+5	–1	+35	+29	ps
0.7	–43	–54	–13	–24	+17	+6	ps
0.6	–67	–83	–37	–53	–7	–23	ps
0.5	–110	–125	–80	–95	–50	–65	ps
0.4	–175	–188	–145	–158	–115	–128	ps
0.3	–285	–292	–255	–262	–225	–232	ps
0.25	–350	–375	–320	–345	–290	–315	ps
0.2	–525	–500	–495	–470	–465	–440	ps
0.15	–800	–708	–770	–678	–740	–648	ps
0.1	–1450	–1125	–1420	–1095	–1390	–1065	ps

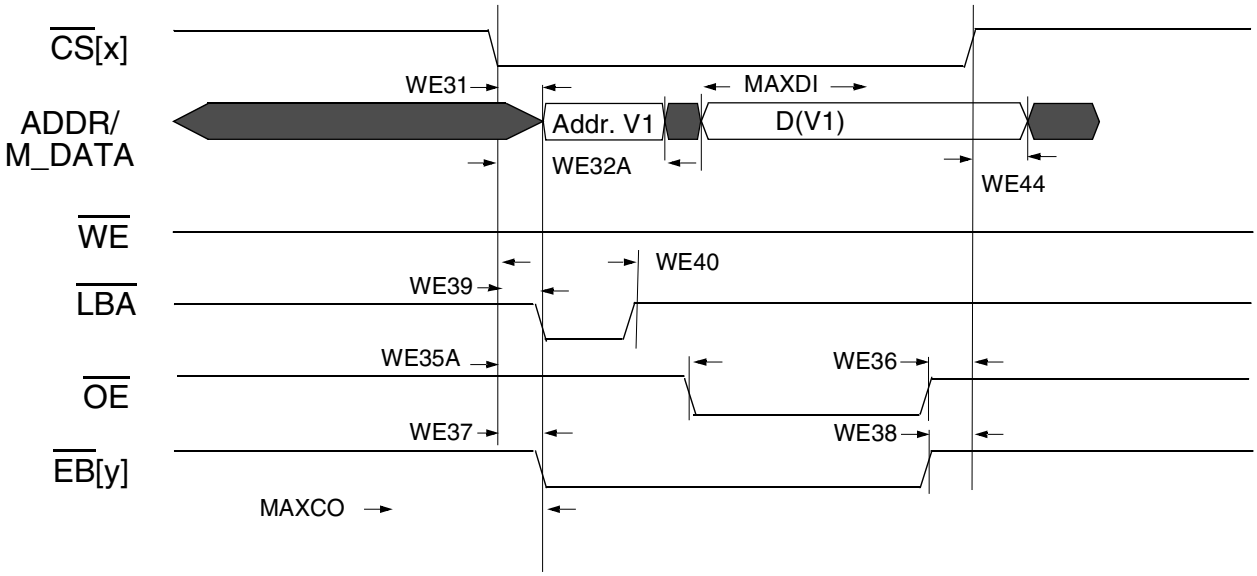

Figure 46. Asynchronous A/D Muxed Read Access (RWSC = 5)

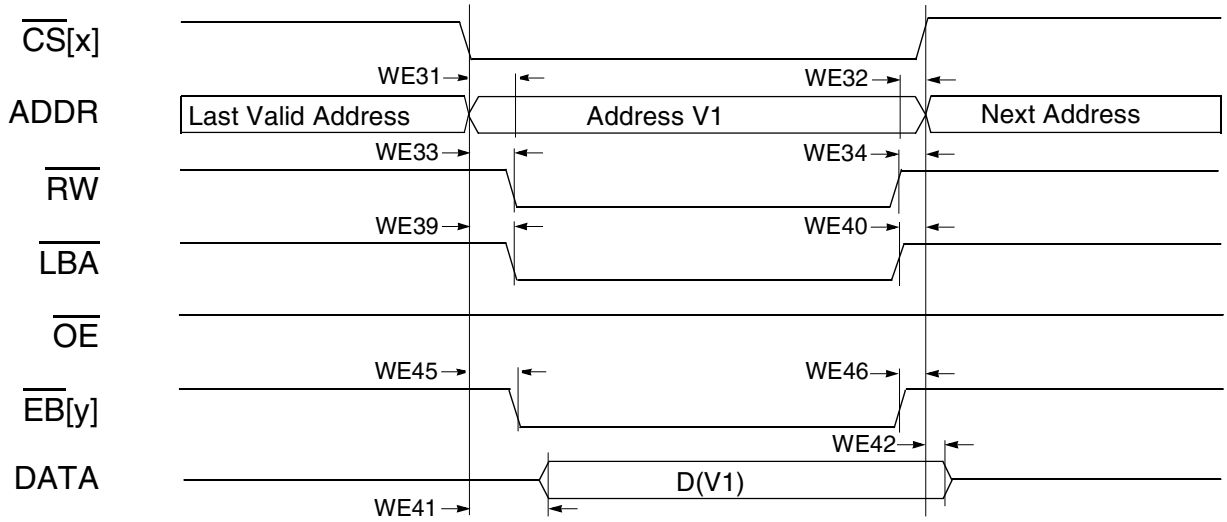

Figure 47. Asynchronous Memory Write Access

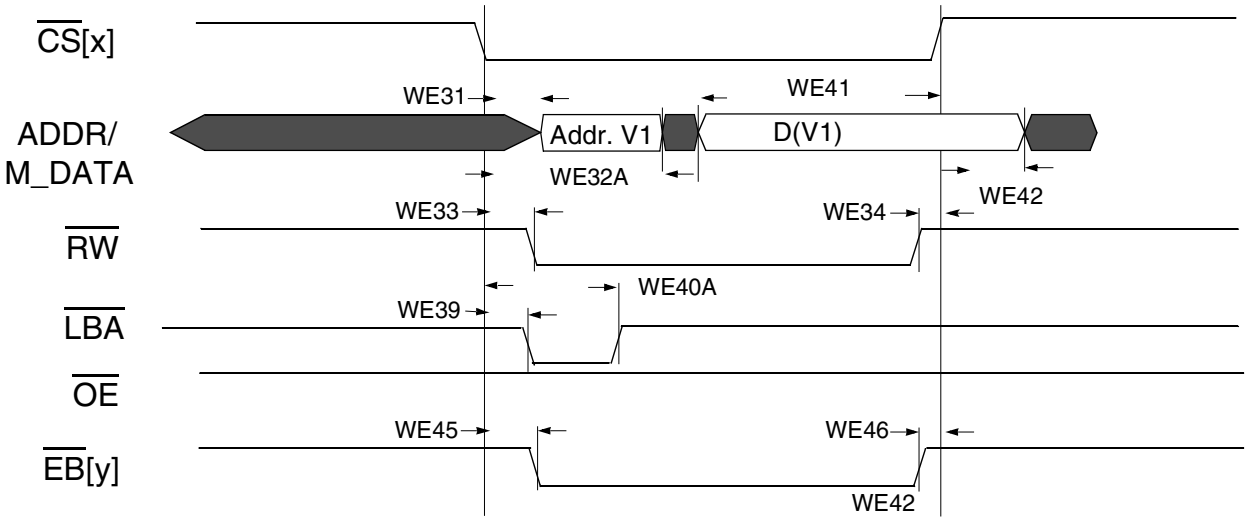

Figure 48. Asynchronous A/D Mux Write Access

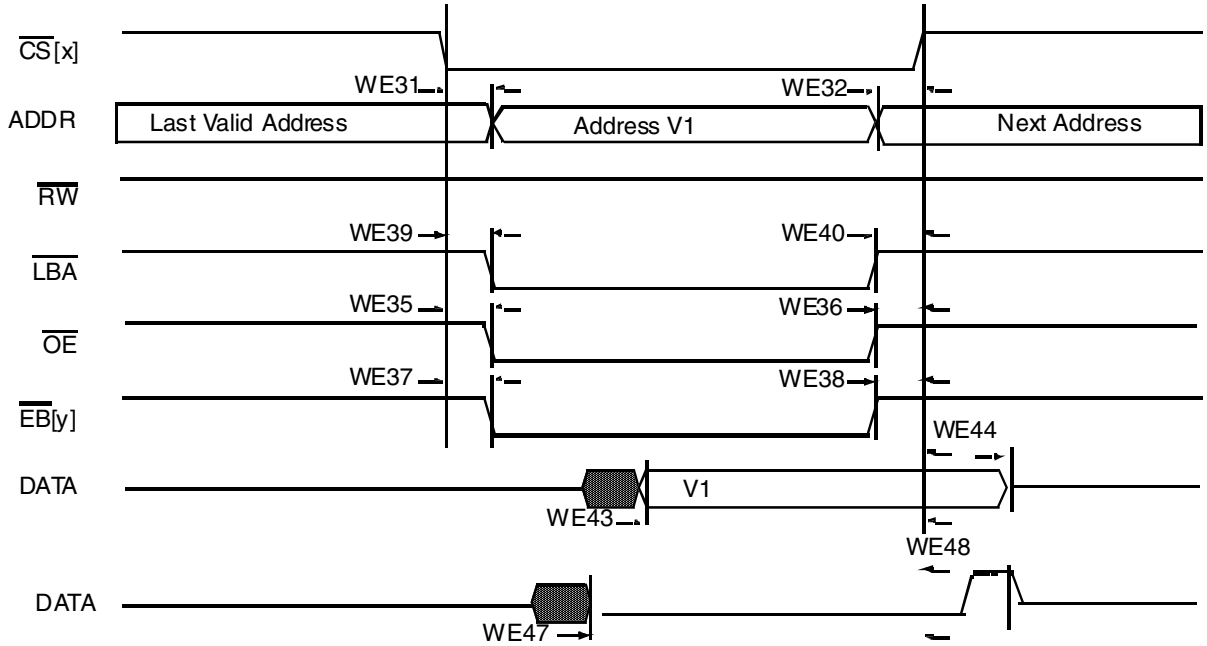

Figure 49. DTACK Read Access

Table 57. WEIM Asynchronous Timing Parameters Relative to Chip Select Table

Ref No.	Parameter	Determination By Synchronous Measured Parameters[1]	Min	Max (If 133 MHz is supported by SoC)	Unit
WE31	$\overline{CS}$[x] valid to Address Valid	WE4 – WE6 – CSA[2]	—	3 – CSA	ns
WE32	Address Invalid to $\overline{CS}$[x] invalid	WE7 – WE5 – CSN[3]	—	3 – CSN	ns

3.7.9.1.5 MII Transmit Signal Timing (FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER, and FEC_TX_CLK)

The transmitter functions correctly up to an FEC_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the FEC_TX_CLK frequency.

Figure 56 shows MII transmit signal timings. Table 63 describes the timing parameters (M5–M8) shown in the figure.

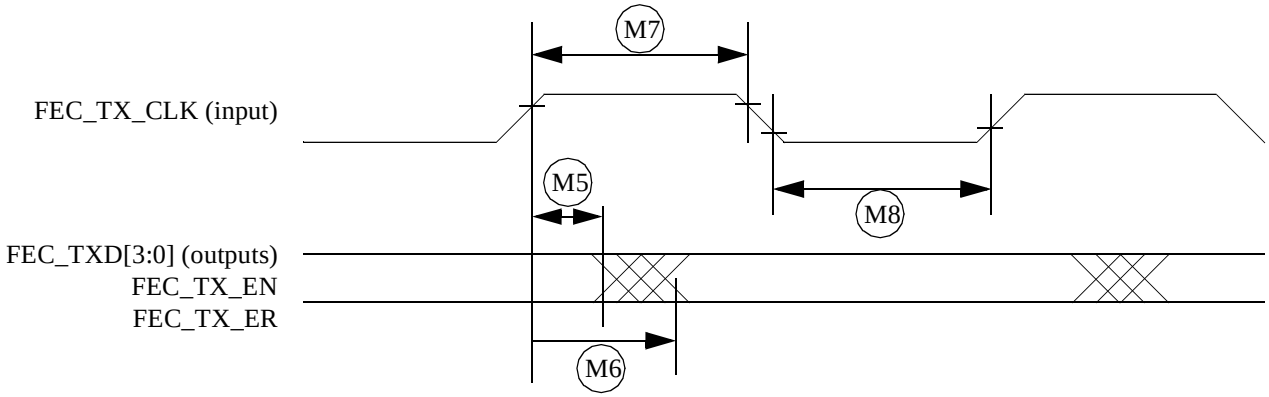

Figure 56. MII Transmit Signal Timing Diagram

Table 63. MII Transmit Signal Timing

ID	Characteristic[1]	Min.	Max.	Unit
M5	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER invalid	5	—	ns
M6	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER valid	—	20	ns
M7	FEC_TX_CLK pulse width high	35%	65%	FEC_TX_CLK period
M8	FEC_TX_CLK pulse width low	35%	65%	FEC_TX_CLK period

[1] FEC_TX_EN, FEC_TX_CLK, and FEC_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

3.7.9.1.6 MII Asynchronous Inputs Signal Timing (FEC_CRS and FEC_COL)

Figure 57 shows MII asynchronous input timings. Table 64 describes the timing parameter (M9) shown in the figure.

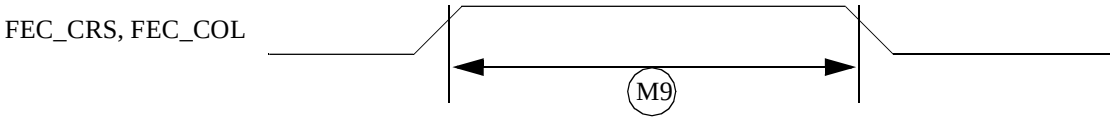

Figure 57. MII Async Inputs Timing Diagram

Table 64. MII Asynchronous Inputs Signal Timing

ID	Characteristic	Min.	Max.	Unit
M9[1]	FEC_CRS to FEC_COL minimum pulse width	1.5	—	FEC_TX_CLK period

[1] FEC_COL has the same timing in 10-Mbit 7-wire interface mode.

3.7.9.2 MII Serial Management Channel Timing (FEC_MDIO and FEC_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to comply with the IEEE 802.3 standard MII specification. However the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Figure 58 shows MII asynchronous input timings. Table 65 describes the timing parameters (M10—M15) shown in the figure.

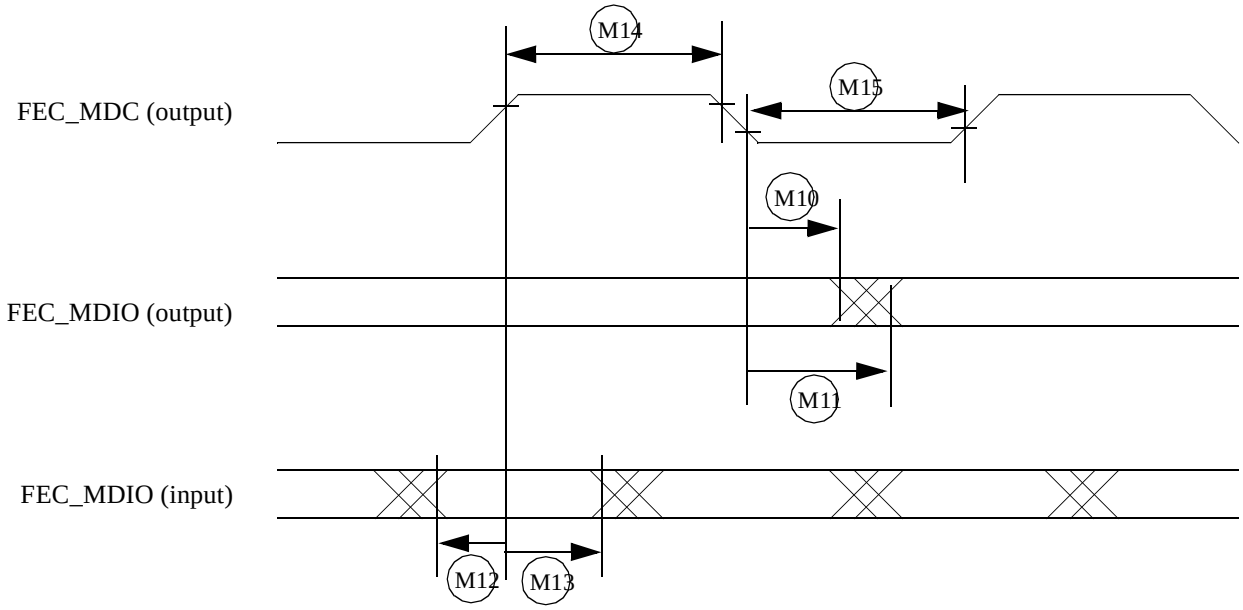

Figure 58. MII Serial Management Channel Timing Diagram

Table 65. MII Serial Management Channel Timing

ID	Characteristic	Min.	Max.	Unit
M10	FEC_MDC falling edge to FEC_MDIO output invalid (min. propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max. propagation delay)	—	5	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	18	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

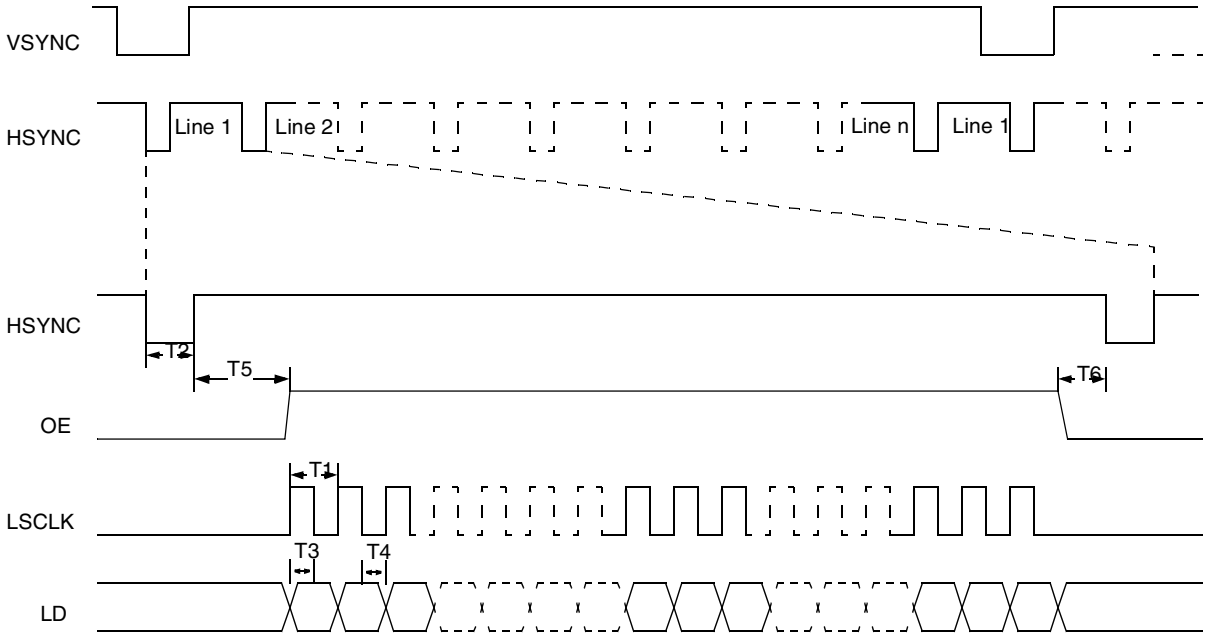

Figure 66. LCDC TFT Mode Timing Diagram

Table 72. LCDC TFT Mode Timing Parameters

ID	Description	Min.	Ma	Unit
T1	Pixel clock period	22.5	1000	ns
T2	HSYNC width	1	—	T[1]
T3	LD setup time	5	—	ns
T4	LD hold time	5	—	ns
T5	Delay from the end of HSYNC to the beginning of the OE pulse	3	—	T[1]
T6	Delay from end of OE to the beginning of the HSYNC pulse	1	—	T[1]

1 T is pixel clock period

3.7.13 Pulse Width Modulator (PWM) Timing Parameters

Figure 67 depicts the timing of the PWM, and Table 73 lists the PWM timing characteristics.

The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse width modulator output (PWMO) external pin.

3.7.14.1 SIM Reset Sequences

SIM cards may have internal reset, or active low reset. The following subset describes the reset sequences in these two cases.

3.7.14.1.1 SIM Cards with Internal Reset

Figure 69 shows the reset sequence for SIM cards with internal reset. The reset sequence comprises the following steps:

- After power-up, the clock signal is enabled on SIM*x*_CLK*y* (time T0)
- After 200 clock cycles, SIM*x*_DATA*y*_RX_TX must be asserted.
- The card must send a response on SIM*x*_DATA*y*_RX_TX acknowledging the reset between 400–40000 clock cycles after T0.

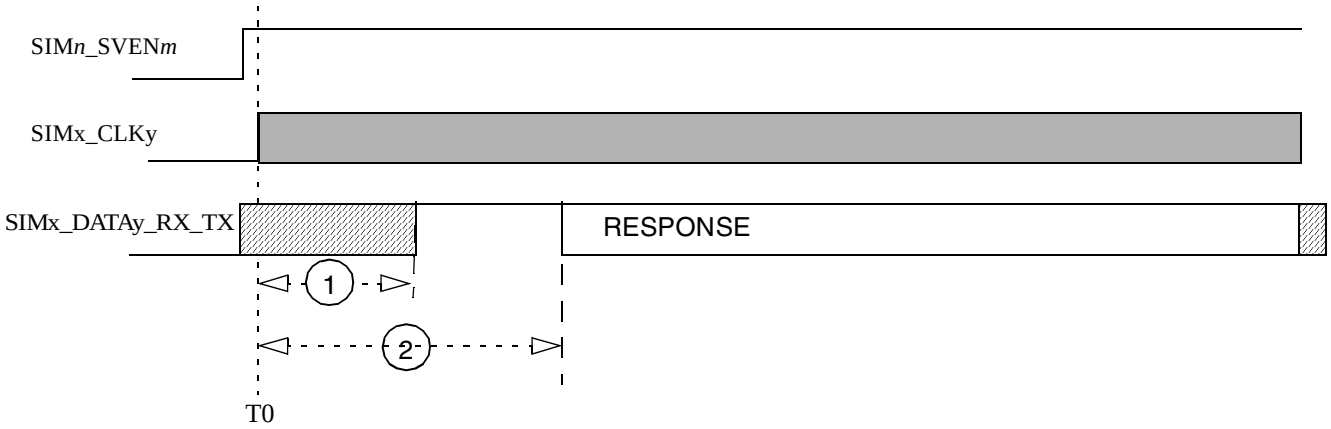

Figure 69. Internal Reset Card Reset Sequence

Table 75 defines the general timing requirements for the SIM interface.

Table 75. Timing Specifications, Internal Reset Card Reset Sequence

Ref No.	Min.	Max.	Units
1	—	200	clk cycles
2	400	40,000	clk cycles

3.7.14.1.2 SIM Cards with Active Low Reset

Figure 70 shows the reset sequence for SIM cards with active low reset. The reset sequence comprises the following steps:

- After power-up, the clock signal is enabled on SIM*x*_CLK*y* (time T0)
- After 200 clock cycles, SIM*x*_DATA*y*_RX_TX must be asserted.
- SIM*x*_RST*y* must remain low for at least 40,000 clock cycles after T0 (no response is to be received on RX during those 40,000 clock cycles)
- SIM*x*_RST*y* is asserted (at time T1)
- SIM*x*_RST*y* must remain asserted for at least 40,000 clock cycles after T1, and a response must be received on SIM*x*_DATA*y*_RX_TX between 400 and 40,000 clock cycles after T1.

3.7.16 Smart Liquid Crystal Display Controller (SLCDC)

Figure 76 and Figure 77 show SLCDC timing for serial and parallel transfers respectively. Table 79 and Table 80 describe the timing parameters shown in the respective figures.

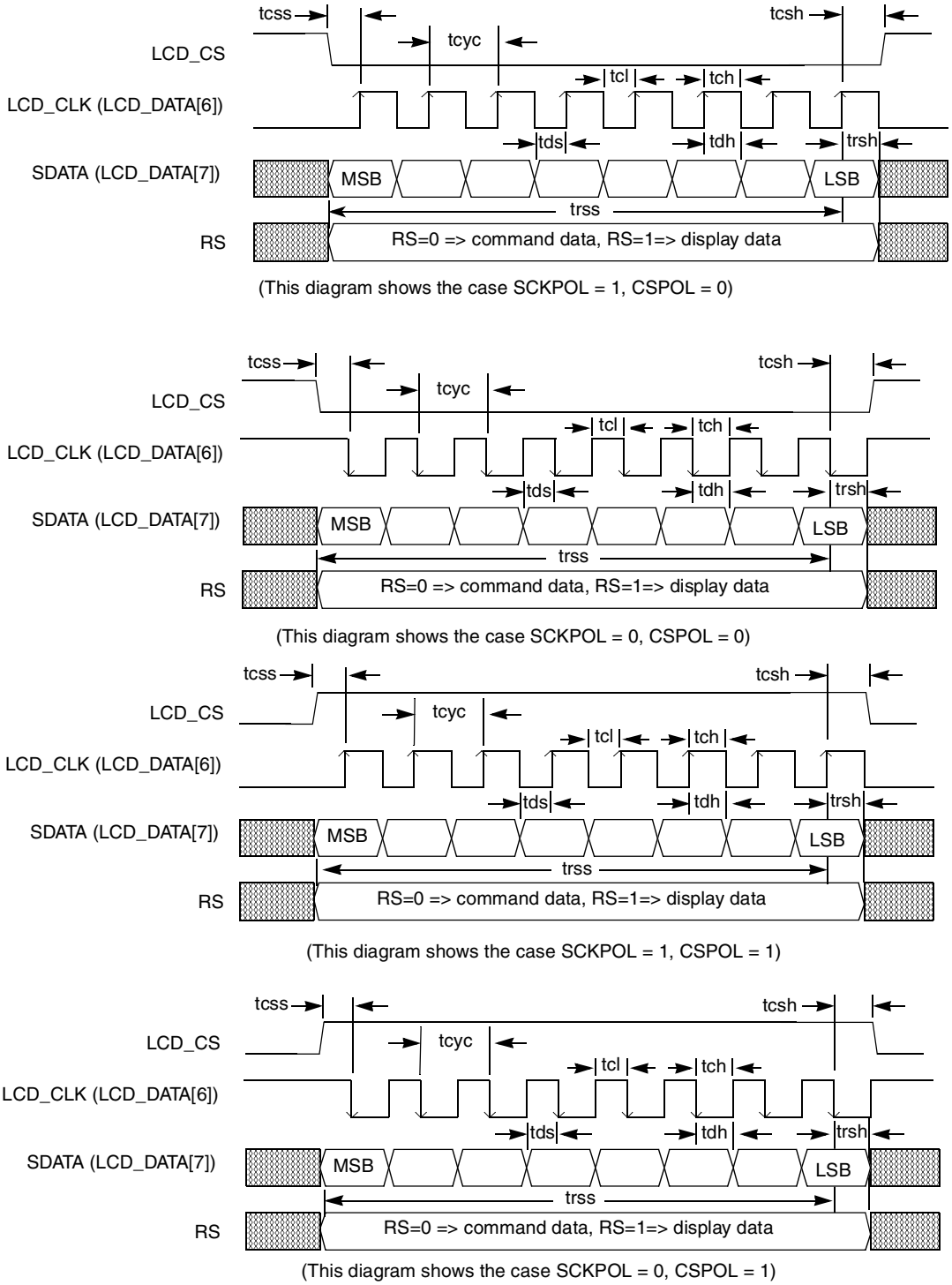

Figure 76. SLCDC Timing Diagram—Serial Transfers to LCD Device

Table 81. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min.	Max.	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) internal FS rise time	—	6.0	ns
SS15	(Tx/Rx) internal FS fall time	—	6.0	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS17	(Tx) CK high to STXD high/low	—	15.0	ns
SS18	(Tx) CK high to STXD high impedance	—	15.0	ns
SS19	STXD rise/fall time	—	6.0	ns
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0.0	—	ns
SS52	Loading	—	25.0	pf

Note:

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on pads when SSI is being used for a data transfer.
- ”Tx” and “Rx” refer, respectively, to the transmit and receive sections of the SSI.
- For internal frame sync operation using external clock, the FS timing is the same as that of Tx data (for example, during AC97 mode of operation).

Figure 84 represents the usage of the ADC with idle cycles between conversions. This diagram is valid for any value of *N* equal or greater than 1.

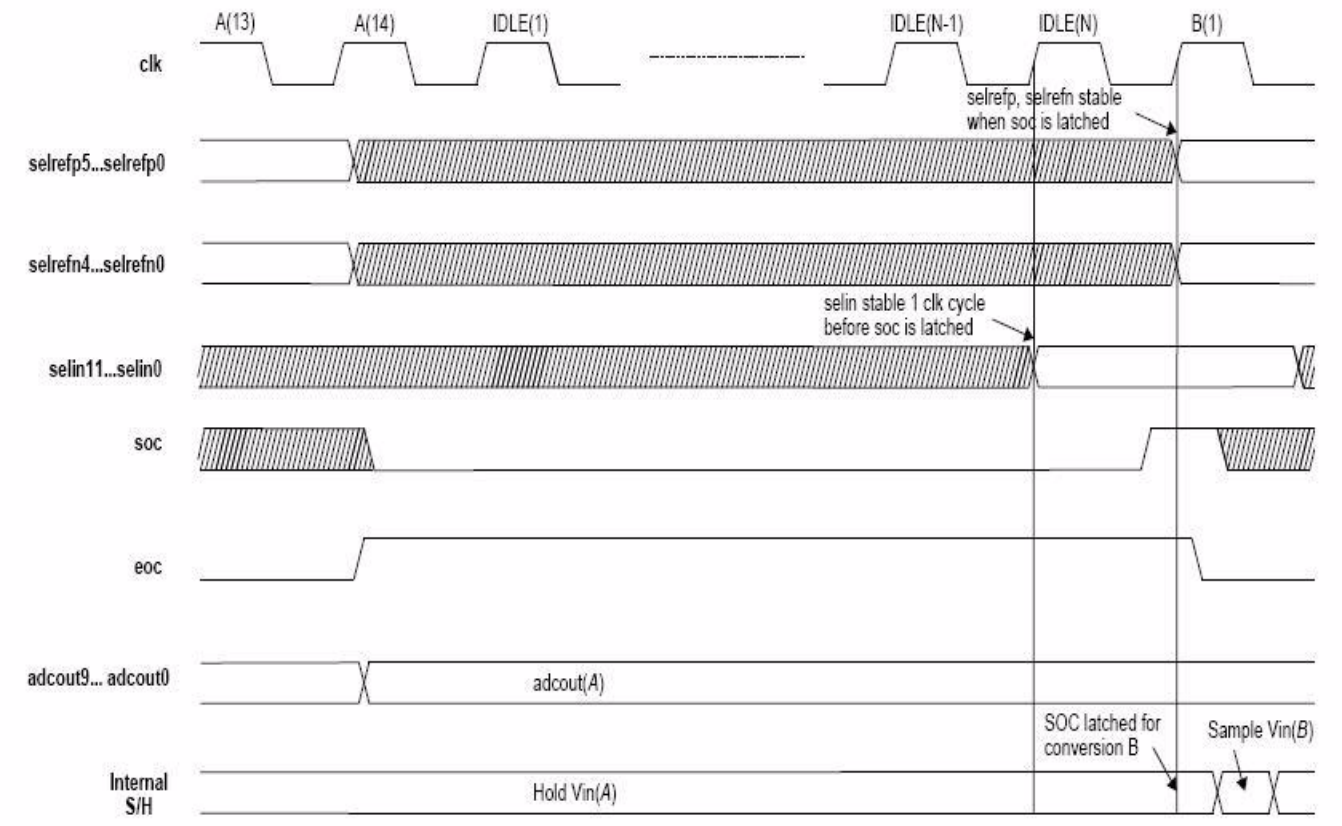

Figure 84. ADC Usage with Idle Cycles Between Conversions

3.7.19 UART Timing

This section describes the timing of the UART module in serial and parallel mode.

Table 101. 17×17 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
I2C1_CLK	F17	CSI	GPIO	INPUT	100 KΩ Pull-Up
I2C1_DAT	G17	CSI	GPIO	INPUT	100 KΩ Pull-Up
CSPI1_MOSI	T4	MISC	GPIO	INPUT	100 KΩ Pull-Up
CSPI1_MISO	W1	MISC	GPIO	OUTPUT	Low
CSPI1_SS0	R4	MISC	GPIO	INPUT	100 KΩ Pull-Up
CSPI1_SS1	V2	MISC	GPIO	INPUT	100 KΩ Pull-Up
CSPI1_SCLK	U3	MISC	GPIO	INPUT	100 KΩ Pull-Up
CSPI1_RDY	V1	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART1_RXD	U2	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART1_TXD	U1	MISC	GPIO	OUTPUT	High
UART1_RTS	T3	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART1_CTS	T2	MISC	GPIO	OUTPUT	High
UART2_RXD	P4	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART2_TXD	T1	MISC	GPIO	OUTPUT	High
UART2_RTS	R3	MISC	GPIO	INPUT	100 KΩ Pull-Up
UART2_CTS	R2	MISC	GPIO	INPUT	-
SD1_CMD	K20	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_CLK	M20	SDIO	GPIO	OUTPUT	High
SD1_DATA0	L20	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_DATA1	N20	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_DATA2	M19	SDIO	GPIO	INPUT	47 KΩ Pull-Up
SD1_DATA3	J20	SDIO	GPIO	INPUT	47 KΩ Pull-Up
KPP_ROW0	N4	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_ROW1	R1	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_ROW2	P3	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_ROW3	P2	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL0	P1	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL1	N3	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL2	N2	MISC	GPIO	INPUT	100 KΩ Pull-Up
KPP_COL3	N1	MISC	GPIO	INPUT	100 KΩ Pull-Up
FEC_MDC	L1	MISC	GPIO	OUTPUT	Low
FEC_MDIO	L2	MISC	GPIO	INPUT	22 KΩ Pull-Up

Table 101. 17×17 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
POWER_FAIL	T19	CRM	GPIO	INPUT	100 KΩ Pull-Down
RESET_B	T18	CRM	GPIO	INPUT	100 KΩ Pull-Up
POR_B	U19	CRM	GPIO	INPUT	100 KΩ Pull-Up
CLKO	V20	CRM	GPIO	OUTPUT	Low
BOOT_MODE0[2]	V19	CRM	GPIO	INPUT	100 KΩ Pull-Down
BOOT_MODE1[2]	W20	CRM	GPIO	INPUT	100 KΩ Pull-Down
CLK_SEL	W19	CRM	GPIO	INPUT	100 KΩ Pull-Down
TEST_MODE	V18	CRM	GPIO	INPUT	100 KΩ Pull-Down
OSC24M_EXTAL	Y15	OSC24M	ANALOG	ANALOG	-
OSC24M_XTAL	Y16	OSC24M	ANALOG	ANALOG	-
OSC32K_EXTAL	Y11	DRYICE	ANALOG	ANALOG	-
OSC32K_XTAL	Y10	DRYICE	ANALOG	ANALOG	-
TAMPER_A	N10	DRYICE	ANALOG	ANALOG	-
TAMPER_B	N11	DRYICE	ANALOG	ANALOG	-
MESH_C	P11	DRYICE	ANALOG	ANALOG	-
MESH_D	P12	DRYICE	ANALOG	ANALOG	-
OSC_BYP	Y12	DRYICE	ANALOG	ANALOG	-
XP	V14	ADC	ANALOG	ANALOG	-
XN	U13	ADC	ANALOG	ANALOG	-
YP	V13	ADC	ANALOG	ANALOG	-
YN	W12	ADC	ANALOG	ANALOG	-
WIPER	U14	ADC	ANALOG	ANALOG	-
INAUX0	U11	ADC	ANALOG	ANALOG	-
INAUX1	V12	ADC	ANALOG	ANALOG	-
INAUX2	U12	ADC	ANALOG	ANALOG	-

1 The state immediately after reset and before ROM firmware or software has executed.

2 During power-on reset this port acts as input for fuse override signal.

3 During power-on reset this port acts as output for diagnostic signal.

Table 107. i.MX25 12×12 Package Ball Map (continued)

	P	N	M	L	K	J	H	G
1	FEC_MDC	FEC_TX_CLK	FEC_TDATA1	D7	D6	D5	D3	D2
2	KPP_COL2	FEC_RDATA1	FEC_MDIO	FEC_TDATA0	D15	D13	D4	D8
3								
4	KPP_ROW3	KPP_COL3	FEC_RDATA0	NC_BGA_L4	D14	D12	D10	NFWP_B
5	UART2_CTS	KPP_COL1		FEC_RX_DV	D11		D9	NFRB
6								QGND
7	NVCC_MISC	QVDD	QGND	QGND	NVCC_NFC	NVCC_NFC	QVDD	QVDD
8	NVCC_MISC	QVDD	QGND	QGND	NVCC_NFC	NVCC_NFC	NVCC_EMI1	NVCC_EMI1
9			QGND	QGND			NVCC_EMI1	NVCC_EMI1
10		QGND	QGND	QGND	QGND		NVCC_EMI1	NVCC_EMI1
11	QGND	QGND	QGND	QGND	QGND	QGND	QGND	QGND
12	QGND	QGND	QGND	QGND	QGND	QGND	QGND	QGND
13		QGND	QGND	QGND	QGND		QVDD	QVDD
14			QGND	QGND			QGND	QGND
15	NVCC_ADC	NGND_ADC	QGND	QGND	USBPHY1_VDDA	NVCC_CSI	NVCC_EMI2	NVCC_EMI2
16	NVCC_CRM	UPLL_GND	QGND	QGND	USBPHY1_VDDA	NVCC_CSI	NVCC_EMI2	NVCC_EMI2
17								
18	FUSE_VDD		UPLL_VDD		USBPHY1_VSSA_BIAS	QVDD	QVDD	
19	GPIO_D	NVCC_SDIO	USBPHY1_UPLLVSS	USBPHY1_RREF	USBPHY1_VSSA	CSI_PIXCLK	CSI_D9	CSI_D5
20								
21	GPIO_B	SD1_CLK	SD1_DATA3	USBPHY1_UPLLVDD	USBPHY1_DP	USBPHY1_DM	I2C1_DAT	CSI_VSYNC
22	SD1_DATA0	SD1_CMD	SD1_DATA2	USBPHY1_VDDA_BIAS	USBPHY1_VBUS	USBPHY1_UID	I2C1_CLK	CSI_HSYNC

Table 107. i.MX25 12×12 Package Ball Map (continued)

	AB	AA	Y	W	V	U	T	R	
1	QGND	CSPI1_MOSI	CSPI1_SCLK	UART1_RTS	UART2_RXD	KPP_ROW2	KPP_COL0	FEC_TX_EN	1
2	LSCLK	QGND	CONTRAST	QGND	CSPI1_SS0	UART1_RXD	UART2_RTS	KPP_ROW0	2
3	LD14	OE_ACD							3
4	LD12	HSYNC		PWM	CSPI1_MISO	CSPI1_SS1	UART2_TXD	KPP_ROW1	4
5	LD10	LD15		VSYNC		CSPI1_RDY	QGND	UART1_CTS	5
6	LD8	LD9		LD13	UART1_TXD		QGND		6
7	LD6	LD7		LD11			NVCC_MISC	NVCC_MISC	7
8	LD4	LD5		LD1			NVCC_LCDC	NVCC_LCDC	8
9	LD2	LD3		QGND			QVDD	NVCC_LCDC	9
10	LD0	BAT_VDD		NVCC_JTAG	QVDD		QVDD	QVDD	10
11	SJC_MOD	TDO		DE_B	TAMPER_A		QGND	QGND	11
12	OSC32K_XTAL	TMS		TDI			QGND	QGND	12
13	OSC32K_EXTAL	TCK		RTCK	TAMPER_B		MESH_C	MESH_D	13
14	TRSTB	REF		INAUX1				NVCC_DRYICE	14
15	OSC_BYP	INAUX0		YN	OSC24M_VDD		OSC24M_GND	QVDD	15
16	INAUX2	XN		USBPHY2_VSS			USBPHY2_VDD	QVDD	16
17	YP	WIPER		USBPHY2_DP	MPLL_GND				17
18	QGND	XP		USBPHY2_DM	QGND		QGND	QGND	18
19	OSC24M_EXTAL	TEST_MODE		MPLL_VDD	QGND	RESET_B	POWER_FAIL	GPIO_F	19
20	OSC24M_XTAL	CLK_SEL							20
21	QGND	QGND	QGND	BOOT_MODE1	POR_B	UPLL_BYPCLK	VSTBY_REQ	GPIO_E	21
22	QGND	BOOT_MODE0	CLKO	VSTBY_ACK	EXT_ARMCLK	GPIO_C	GPIO_A	SD1_DATA1	22