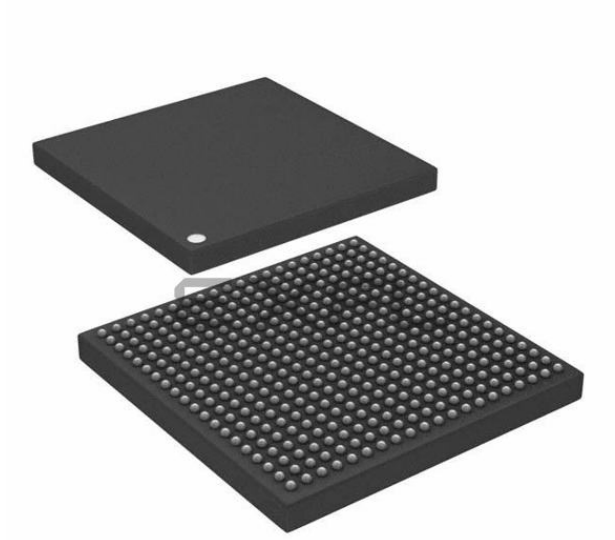

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-20°C ~ 70°C (TA)
Security Features	-
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx257djm4a

1.2 Block Diagram

Figure 1 shows the simplified interface block diagram.

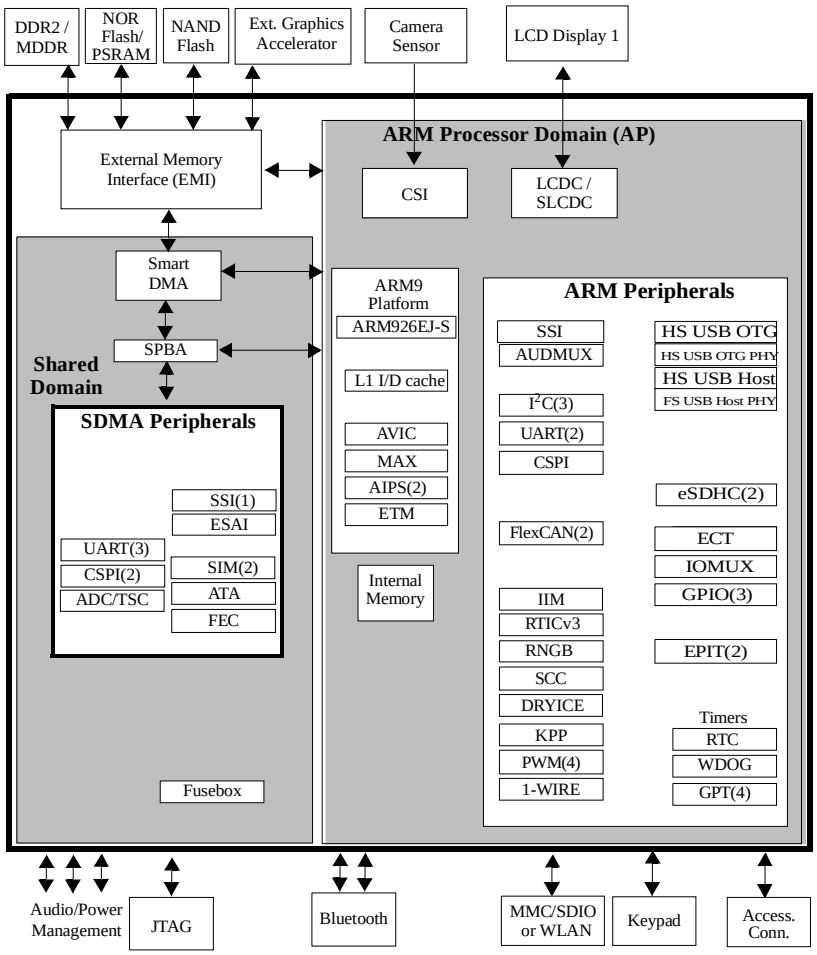

Figure 1. i.MX25 Simplified Interface Block Diagram

3.1.3 Fusebox Supply Current Parameters

Table 7 lists the fusebox supply current parameters.

Table 7. Fusebox Supply Current Parameters

Parameter	Symbol	Min.	Typ.	Max.	Units
eFuse program current[1] Current to program one eFuse bit The associated VDD_FUSE supply = 3.6 V	$I_{program}$	26	35	62	mA
eFuse read current[2] Current to read an 8-bit eFuse word	I_{read}	—	12.5	15	mA

1 The current $I_{program}$ is during program time ($t_{program}$).

2 The current I_{read} is present for approximately 50 ns of the read access to the 8-bit word.

3.1.4 Interface Frequency Limits

Table 8 provides information for interface frequency limits.

Table 8. Interface Frequency Limits

Parameter	Min.	Typ.	Max.	Units
JTAG: TCK Frequency of Operation	DC	5	10	MHz
OSC24M_XTAL Oscillator	—	24	—	MHz
OSC32K_XTAL Oscillator	—	32.768	—	kHz

Table 9 provides the recommended external crystal specifications.

Table 9. Recommended External Crystal Specifications

	24 MHz	32.768 kHz
Frequency Tolerance	<= ± 30 ppm	<= ± 30 ppm
ESR	< 80 Ω	50 K~60 K
Load Capacitor	8 pF–12 pF	6 pF–8 pF (12 pF–16 pF on each pin)
Shunt Capacitor	< 7 pF	1 pF
Drive Level	> 150 µW	> 1 µW

Table 10 provides the recommended external reference clock oscillator specifications (when reference is used from an external clock source).

Table 10. Recommended External Reference Clock Specifications

	24 MHz	32.768 kHz
V_{OH}	min = 0.7* VDD	min = 0.7* VDD
V_{OL}	max = 0.3* VDD	max = 0.3* VDD
Frequency Tolerance	= 30 ppm	= 30 ppm

Table 14. iMX25 Reduced Power Mode Current Consumption

Power Group	Power Supply	Voltage Setting	Typical Current Consumption
BAT_VDD	BAT_VDD	1.15 V	9.95 µA
		1.55 V	12.6 µA

3.2 Supply Power-Up/Power-Down Requirements and Restrictions

Any i.MX25 board design must comply with the power-up and power-down sequence guidelines given in this section to ensure reliable operation of the device. Recommended power-up and power-down sequences are given in the following subsections.

CAUTION

Deviations from the guidelines in this section may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the i.MX25 (worst-case scenario)

NOTE

For security applications, the coin battery must be connected during both power-up and power-down sequences to ensure that security keys are not unintentionally erased.

3.2.1 Power-Up Sequence

For those users that are not using DryIce/SRTC, the following power-up sequence is recommended:

1. Assert power on reset (POR).
2. Turn on QVDD digital logic domain supplies.
3. Turn on NVCCx digital I/O power supplies after QVDD is stable.
4. Turn on all other analog power supplies, including USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD, USBPHY1_VDDA, USBPHY2_VDD, OSC24M_VDD, MPPLL_VDD, UPLL_VDD, NVCC_ADC, and FUSEVDD (FUSEVDD is tied to GND if fuses are not programmed), after all NVCCx digital I/O supplies are stable.
5. Negate the POR signal.

Table 19. DDR2 (SSTL_18) I/O DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Termination voltage[5]	Vtt	—	OVDD/2 – 0.04	OVDD/2	OVDD/2 + 0.04	
Input current[6](no pull-up/down)	IIN	VI = 0 VI = OVDD	—	—	110 60	nA
High-impedance I/O supply current[6]	Icc-ovdd	VI = OVDD or 0	—	—	980	nA
High-impedance core supply current[6]	Icc-vddi	VI = VDD or 0	—	—	1210	nA

1 OVDD = 1.7 V; V_{out} = 1.42 V. (V_{out}-OVDD)/IOH must be less than 21 W for values of V_{out} between OVDD and OVDD-0.28 V.

2 OVDD = 1.7 V; V_{out} = 280 mV. V_{out}/IOL must be less than 21 W for values of V_{out} between 0 V and 280 mV. Simulation circuit for parameters V_{oh} and V_{ol} for I/O cells is below.

3 Vin(dc) specifies the allowable DC excursion of each differential input.

4 Vid(dc) specifies the input differential voltage required for switching. The minimum value is equal to Vih(dc) - Vil(dc).

5 Vtt is expected to track OVDD/2.

6 Minimum condition: BCS model, 1.95 V, and –40 °C. Typical condition: typical model, 1.8 V, and 25 °C. Maximum condition: wcs model, 1.65 V, and 105 °C.

3.5.2 GPIO I/O DC Parameters

Table 20 shows the I/O parameters for GPIO.

Table 20. GPIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
High-level output voltage[1]	Voh	Ioh=–1mA Ioh = Specified Drive	OVDD – 0.15 0.8 × OVDD	—	—	V
Low-level output voltage[1]	Vol	Iol=1mA Iol=Specified Drive	—	—	0.15 0.2 × OVDD	V
High-level output current for slow mode	I Ioh	Voh=0.8 × OVDD Standard Drive High Drive Max. Drive	 –2.0 –4.0 –8.0	—	—	mA
High-level output current for fast mode	I Ioh	Voh=0.8 × OVDD Standard Drive High Drive Max. Drive	 –4.0 –6.0 –8.0	—	—	mA
Low-level output current for slow mode	I Iol	Voh=0.2 × OVDD Standard Drive High Drive Max. Drive	 2.0 4.0 8.0	—	—	mA
Low-level output current for fast mode	I Iol	Voh=0.2 × OVDD Standard Drive High Drive Max. Drive	 4.0 6.0 8.0	—	—	mA
High-level DC input voltage	VIH	—	0.7 × OVDD	—	OVDD	V
Low-level DC input voltage	VIL	—	–0.3 V	—	0.3 × OVDD	V

Table 20. GPIO DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input hysteresis	VHYS	OVDD = 3.3 V OVDD = 1.8V	370 290	—	420 320	mV
Schmitt trigger VT+[1]	VT+	—	0.5 × OVDD	—	—	V
Schmitt trigger VT–[1]	VT–	—	—	—	0.5 × OVDD	V
Pull-up resistor (22 kΩ PU)	Rpu	Vi=0	18.5	22	25.6	kΩ
Pull-up resistor (47 kΩ PU)	Rpu	Vi=0	41	47	55	kΩ
Pull-up resistor (100 kΩ PU)	Rpu	Vi=0	85	100	120	kΩ
Pull-down resistor (100 kΩ PD)	Rpd	VI = OVDD	85	100	120	kΩ
Input current (no pull-up/down)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	—	—	100 60 77 50	nA
Input current (22 kΩ PU)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	117 0.0001 64 0.0001	—	184 0.0001 104 0.0001	µA
Input current (47 kΩ PU)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	54 0.0001 30 0.0001	—	88 0.0001 49 0.0001	µA
Input current (100 kΩ PU)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	25 0.0001 14 0.0001	—	42 0.0001 23 0.0001	µA
Input current (100 kΩ PD)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	25 0.0001 14 0.0001	—	42 0.001 23 0.0001	µA
High-impedance I/O supply current	Icc–ovdd	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	—	—	688 688 560 560	nA
High-impedance core supply current	Icc–vddi	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	—	—	490 490 410 410	nA

[1] Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

3.6 AC Electrical Characteristics

This section provides the AC parameters for slow and fast I/O.

Table 22. Fast I/O AC Parameters for OVDD = 1.65–1.95 V (continued)

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Output pad dI/dt[3] (max. drive)	tdit	25 pF 50 pF	7 7	43 46	112 118	mA/ns
Output pad dI/dt[3] (high drive)	tdit	25 pF 50 pF	11 12	31 33	81 85	mA/ns
Output pad dI/dt[3] (standard drive)	tdit	25 pF 50 pF	9 10	27 28	71 74	mA/ns
Input pad propagation delay without hysteresis, 50%–50%[4]	tpi	1.6 pF	0.74/1	1.1/1.5	1.75/2.16	ns
Input pad propagation delay with hysteresis, 50%–50%[4]	tpi	1.6 pF	1.75/1.63	2.67/2.22	2.92/3	ns
Input pad propagation delay without hysteresis, 40%–60%[4]	tpi	1.6 pF	1.82/1.55	2.28/1.87	2.95/2.54	ns
Input pad propagation delay with hysteresis, 40%–60%[4]	tpi	1.6 pF	2.4/2.6	3/3.07	3.77/3.71	ns
Input pad transition times without hysteresis[4]	trfi	1.6 pF	0.16/0.12	0.30/0.18	0.33/0.29	ns
Input pad transition times with hysteresis[4]	trfi	1.6 pF	0.16/0.13	0.30/0.18	0.33/0.29	ns
Maximum input transition times[5]	trm	—	—	—	25	ns

1 Maximum condition for tpr, tpo, and tpv: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.95 V, and –40 °C. Input transition time from core is 1 ns (20%–80%).

2 Minimum condition for tps: wcs model, 1.1 V, I/O 1.65 V and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

3 Maximum condition for tdit: bcs model, 1.3 V, I/O 1.95 V and –40 °C.

4 Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.65 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

5 Hysteresis mode is recommended for input with transition time greater than 25 ns.

Table 23 shows the fast I/O AC parameters for OVDD = 3.0–3.6 V.

Table 23. Fast I/O AC Parameters for OVDD = 3.0–3.6 V

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty Cycle	Fduty		40		60	%
Output Pad Transition Times[1] (Max Drive)	tpr	25 pF 50 pF	0.80/0.70 1.40/1.60	1.12/2.51 1.60/2.39	1.64/1.32 2.84/2.10	ns
Output Pad Transition Times[1] (High Drive)	tpr	25 pF 50 pF	1.00/0.90 1.95/1.66	1.43/1.16 2.66/2.09	2.05/1.60 3.70/2.80	ns
Output Pad Transition Times[1] (Standard Drive)	tpr	25 pF 50 pF	1.50/1.30 2.90/2.50	2.09/1.67 3.40/3.09	3.00/2.30 5.56/4.12	ns
Output Pad Propagation Delay[1] (Max Drive), 50%–50%	tpo	25 pF 50 pF	1.20/1.28 1.67/1.75	1.74/1.73 2.39/2.32	2.67/2.52 3.58/3.33	ns

3.6.3.2 DDR_TYPE = 01 SDRAM I/O AC Parameters and Requirements

Table 27 shows AC parameters for SDRAM I/O.

Table 27. AC Parameters for SDRAM I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	50	60	%
Clock frequency[1]	f	—	—	—	133	MHz
Output pad transition times[1] (max. drive)	tpr	25 pF 50 pF	0.82/0.87 1.56/1.67	1.14/1.13 2.13/2.09	1.62/1.50 3.015/2.77	ns
Output pad transition times[1] (high drive)	tpr	25 pF 50 pF	1.23/1.31 2.31/2.47	1.71/1.68 3.22/3.12	2.39/2.22 4.53/4.16	ns
Output pad transition times[1] (standard drive)	tpr	25 pF 50 pF	2.44/2.60 4.65/4.99	3.38/3.27 6.38/6.23	4.73/4.38 9.05/8.23	ns
Output pad propagation delay[1] (max. drive), 50%–50%	tpo	15 pF 35 pF	0.97/1.19 2.85/3.21	1.69/0.75 2.02/2.30	2.17/2.46 2.93/3.27	ns
Output pad propagation delay[1] (high drive), 50%–50%	tpo	15 pF 35 pF	1.15/1.39 3.57/3.91	1.72/1.93 2.54/2.85	2.51/2.77 3.66/3.97	ns
Output pad propagation delay[1] (standard drive), 50%–50%	tpo	15 pF 35 pF	2.01/1.57 5.73/6.05	2.45/2.69 4.10/4.51	3.54/3.77 5.84/6.13	ns
Output pad propagation delay[1] (max. drive), 40%–60%	tpo	15 pF 35 pF	1.06/1.26 1.38/1.38	1.53/1.73 1.96/2.23	2.18/2.47 2.78/3.12	ns
Output pad propagation delay[1] (high drive), 40%–60%	tpo	15 pF 35 pF	1.15/1.20 1.75/1.67	1.72/1.93 2.37/2.66	2.45/2.71 3.35/3.67	ns
Output pad propagation delay[1] (standard drive), 40%–60%	tpo	15 pF 35 pF	1.91/2.01 2.88/2.56	2.30/2.52 3.59/3.97	3.26/3.50 5.06/5.36	ns
Output enable to output valid delay[1] (max. drive), 50%–50%	tpv	15 pF 35 pF	0.90/1.27 1.07/1.77	1.44/1.89 1.66/2.51	2.19/2.87 2.51/3.69	ns
Output enable to output valid delay[1] (high drive), 50%–50%	tpv	15 pF 35 pF	1.01/1.48 1.37/2.33	1.58/2.16 2.06/3.09	2.38/3.23 3.06/4.46	ns
Output enable to output valid delay[1] (standard drive), 50%–50%	tpv	15 pF 35 pF	1.32/2.14 2.04/3.67	2.02/3.00 3.00/4.91	3.01/4.36 4.40/6.90	ns
Output enable to output valid delay[1] (max. drive), 40%–60%	tpv	15 pF 35 pF	1.03/1.34 1.16/1.74	1.54/1.94 1.74/2.44	2.26/2.88 2.55/3.54	ns
Output enable to output valid delay[1] (high drive), 40%–60%	tpv	15 pF 35 pF	1.11/1.51 1.39/2.10	1.65/2.15 2.03/2.89	2.43/3.16 2.95/4.13	ns
Output enable to output valid delay[1] (standard drive), 40%–60%	tpv	15 pF 35 pF	1.35/2.03 1.91/3.23	1.99/2.83 2.76/4.30	2.89/4.03 3.98/6.01	ns
Output pad slew rate[2] (max. drive)	tps	25 pF 50 pF	1.11/1.20 0.97/0.65	1.74/1.75 0.92/0.94	2.42/2.46 1.39/1.30	V/ns
Output pad slew rate[2] (high drive)	tps	25 pF 50 pF	0.76/0.80 0.40/0.43	1.16/1.19 0.61/0.63	1.76/1.66 0.93/0.87	V/ns

Table 30. AC Parameters for DDR2 pbijtov18_33_ddr_clk I/O (continued)

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Output pad propagation delay[1], 40%–60% input signals and crossing of output signals	tpo	25 pF 50 pF	1.47/1.38 1.75/1.67	2.13/2.00 2.54/2.40	3.072/2.87 3.65/3.45	ns
Output enable to output valid delay, 50%–50%[1]	tpv	25 pF 50 pF	1.32/1.28 1.66/1.65	2.11/2.00 2.61/2.50	3.31/3.12 4.06/3.81	ns
Output enable to output valid delay, 40%–60%[1]	tpv	25 pF 50 pF	1.40/1.37 1.67/1.66	2.16/2.06 2.56/2.45	3.30/3.13 3.89/3.67	ns
Output pad slew rate[2]	tps	25 pF 50 pF	0.86/0.98 0.46/054	1.35/1.5 0.72/0.81	2.15/2.19 1.12/1.16	V/ns
Output pad dI/dt[3]	tdit	25 pF 50 pF	72 77	172 183	400 422	mA/ns
Input pad transition times[4]	trfi	1.0 pF	0.07/0.08	0.10/0.12	0.17/0.20	ns
Input pad propagation delay, 50%–50%[4]	tpi	1.0 pF	0.89/0.87	1.41/1.37	2.16/2.07	ns
Input pad propagation delay, 40%–60%[4]	tpi	1.0 pF	1.71/1.69	2.22/2.18	2.98/2.88	ns

1 Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 1. V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.9 V and –40 °C. Input transition time from core is 1 ns (20%–80%).

2 Minimum condition for tps: wcs model, 1.1 V, I/O 1.7 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

3 Maximum condition for tdit: bcs model, 1.3 V, I/O 1.9 V, and –40 °C.

4 Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.7 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.9 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

Table 31 shows the AC requirements for DDR2 I/O.

Table 31. AC Requirements for DDR2 I/O

Parameter[1]	Symbol	Min.	Max.	Units
AC input logic high	VIH(ac)	OVDD/2 + 0.25	OVDD + 0.3	V
AC input logic low	VIL(ac)	–0.3	OVDD/2 – 0.25	V
AC differential input voltage[2]	Vid(ac)	0.5	OVDD + 0.6	V
AC differential cross point voltage for input[3]	Vix(ac)	OVDD/2–0.175	OVDD/2 + 0.175	V
AC differential cross point voltage for output[4]	Vox(ac)	OVDD/2–0.125	OVDD/2 + 0.125	V

1 The Jedec SSTL_18 specification (JESD8-15a) for an SSTL interface for class II operation supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr–Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The minimum value is equal to Vih(ac)–Vil(ac)

3 The typical value of Vix(ac) is expected to be about 0.5 × OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4 The typical value of Vox(ac) is expected to be about 0.5 × OVDD and Vox(ac) is expected to track variation in OVDD. Vox(ac) indicates the voltage at which differential output signal must cross. Cload = 25 pF.

Table 43. CSPI Interface Timing Parameters

ID	Parameter Description	Symbol	Minimum	Maximum	Units
t1	CSPI master SCLK cycle time	t_{clko}	60.2	—	ns
t2	CSPI master SCLK high time	t_{clkoH}	22.65	—	ns
t3	CSPI master SCLK low time	t_{clkoL}	22.47	—	ns
t1’	CSPI slave SCLK cycle time	t_{clki}	60.2	—	ns
t2’	CSPI slave SCLK high time	t_{clkiH}	30.1	—	ns
t3’	CSPI slave SCLK low time	t_{clkiL}	30.1	—	ns
t4	CSPI SCLK transition time	t_{pr}[1]	2.6	8.5	ns
t5	SS*n* output pulse width	t_{Wsso}	$2T_{sclk}$[2] $+T_{wait}$[3]	—	—
t5’	SS*n* input pulse width	t_{Wssi}	T_{per}[4]	—	—
t6	SS*n* output asserted to first SCLK edge (SS output setup time)	t_{Ssso}	$3T_{sclk}$	—	—
t6’	SS*n* input asserted to first SCLK edge (SS input setup time)	t_{Sssi}	T_{per}	—	—
t7	CSPI master: Last SCLK edge to SS*n* negated (SS output hold time)	t_{Hsso}	$2T_{sclk}$	—	—
t7’	CSPI slave: Last SCLK edge to SS*n* negated (SS input hold time)	t_{Hssi}	30	—	ns
t8	CSPI master: CSPI1_RDY low to SS*n* asserted (CSPI1_RDY setup time)	t_{Srdy}	$2T_{per}$	$5T_{per}$	—
t9	CSPI master: SS*n* negated to CSPI1_RDY low	t_{Hrdy}	0	—	ns
t10	Output data setup time	t_{Sdatao}	(t_{clkoL} or t_{clkoH} or t_{clkiL} or t_{clkiH}) – T_{ipg}[5]	—	—
t11	Output data hold time	t_{Hdatao}	t_{clkoL} or t_{clkoH} or t_{clkiL} or t_{clkiH}	—	—
t12	Input data setup time	t_{Sdatai}	T_{ipg} + 0.5	—	ns
t13	Input data hold time	t_{Hdatai}	0	—	ns
t14	Pause between data word	t_{pause}	0	—	ns

1 The output SCLK transition time is tested with 25 pF drive.

2 T_{sclk} = CSPI clock period

3 T_{wait} = Wait time, as specified in the sample period control register

4 T_{per} = CSPI reference baud rate clock period (PERCLK2)

5 T_{ipg} = CSPI main clock IPG_CLOCK period

3.7.6 External Memory Interface (EMI) Timing

The EMI module includes the enhanced SDRAM/LPDDR memory controller (ESDCTL), NAND Flash controller (NFC), and wireless external interface module (WEIM). The following subsections give timing information for these submodules.

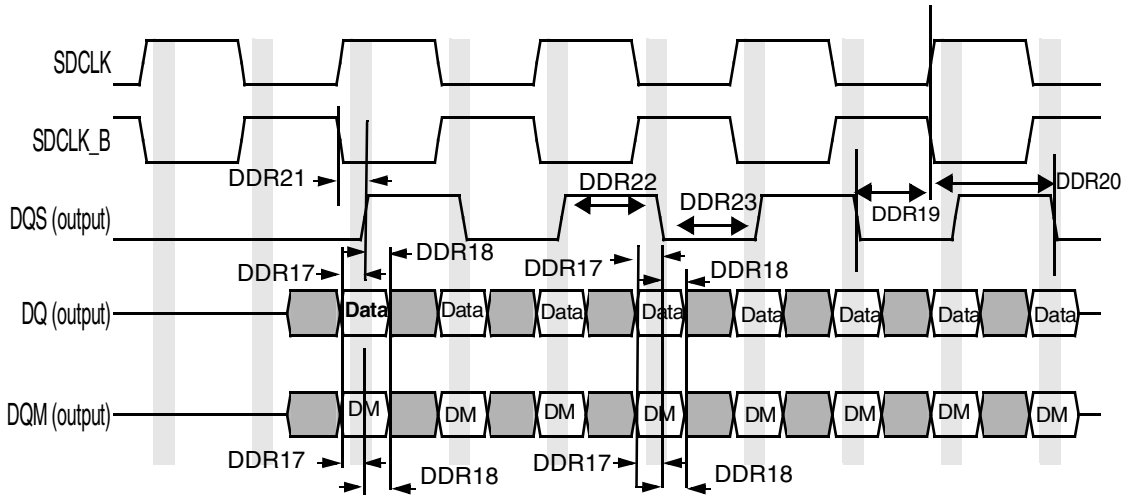

Figure 32. DDR2 SDRAM Write Cycle Timing Diagram

Table 52. DDR2 SDRAM Write Cycle Parameter Table

ID	Parameter	Symbol	DDR2-400		Unit
			Min.	Max.	
DDR17	DQ & DQM setup time to DQS (single-ended strobe)[1]	$t_{DS1(base)}$	0.6	—	ns
DDR18	DQ & DQM hold time to DQS (single-ended strobe)[1]	$t_{DH1(base)}$	0.6	—	ns
DDR19	Write cycle DQS falling edge to SDCLK output setup time	t_{DSS}	0.3	—	tCK
DDR20	Write cycle DQS falling edge to SDCLK output hold time	t_{DSH}	0.3	—	tCK
DDR21	DQS latching rising transitions to associated clock edges	t_{DQSS}	-0.2	0.2	tCK
DDR22	DQS high-level width	t_{DQSH}	0.35	—	tCK
DDR23	DQS low-level width	t_{DQSL}	0.35	—	tCK

[1] These values are for a DQ/DM slew rate of 1 V/ns and a DQS slew rate of 1 V/ns. For additional values use Table 53, “DtDS1, DtDH1 Derating Values for DDR2-400, DDR2-533.”

Table 53. ΔtDS1, ΔtDH1 Derating Values for DDR2-400, DDR2-533[1,2,3]

	DQS Single-Ended Slew Rate																	
	2.0 V/ns		1.5 V/ns		1.0 V/ns		0.9 V/ns		0.8 V/ns		0.7 V/ns		0.6 V/ns		0.5 Vns		0.4 V/ns	
	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1

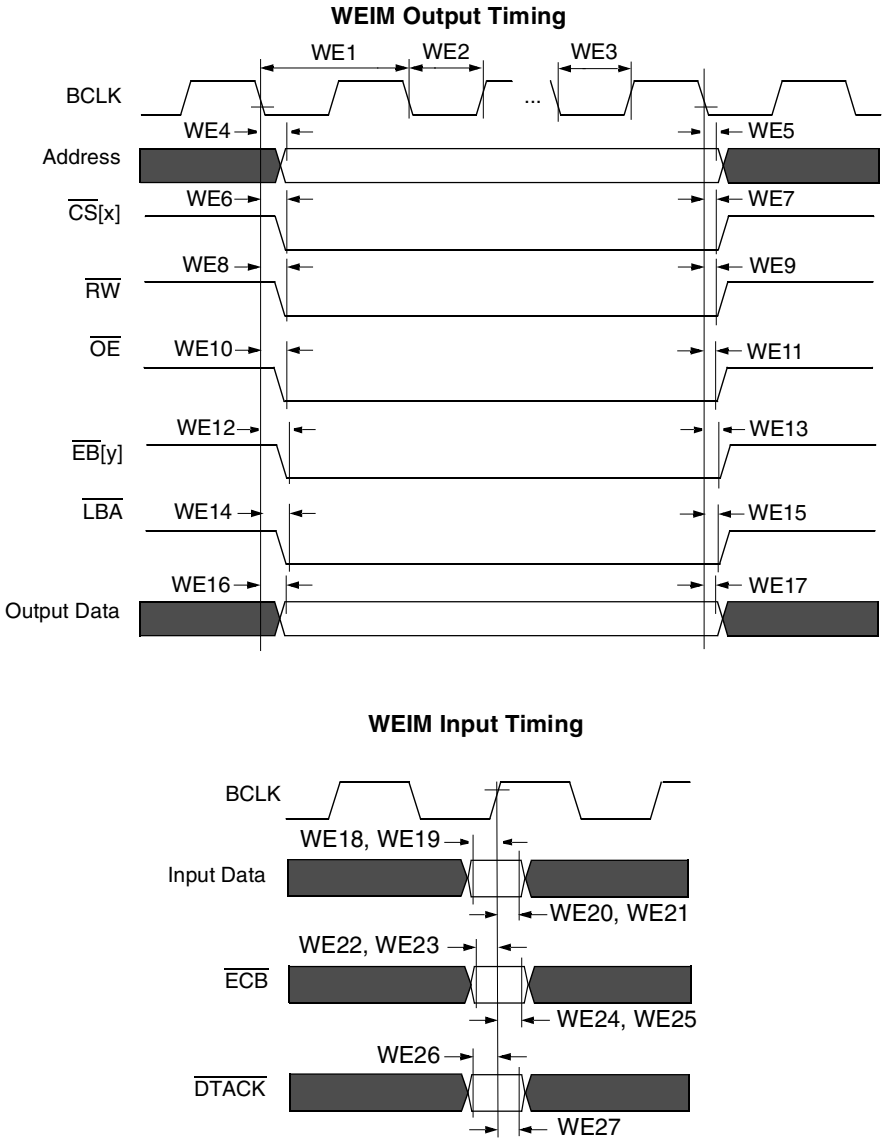

Figure 38. WEIM Bus Timing Diagram

Table 56. WEIM Bus Timing Parameters[1]

ID	Parameter	Min.	Max.	Unit
WE1	BCLK cycle time[2]	14.5	—	ns
WE2	BCLK low-level width[2]	7	—	ns
WE3	BCLK high-level width[2]	7	—	ns
WE4	Clock fall to address valid	15	21	ns
WE5	Clock rise/fall to address invalid	22	25	ns
WE6	Clock rise/fall to $\overline{CS}$[x] valid	15	19	ns
WE7	Clock rise/fall to $\overline{CS}$[x] invalid	3.3	5	ns

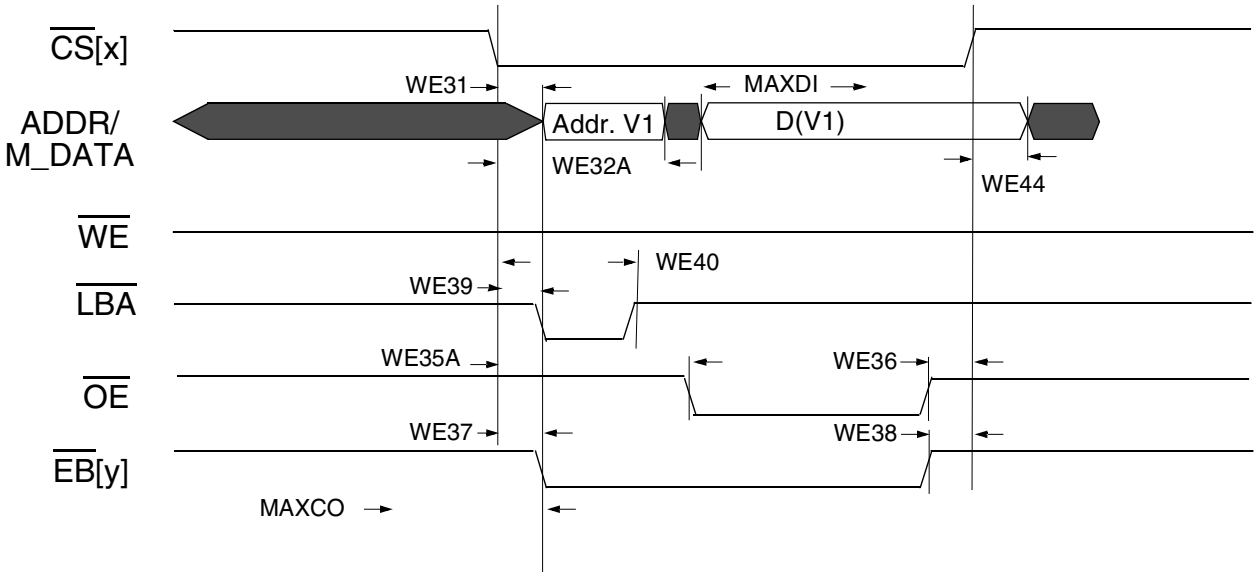

Figure 46. Asynchronous A/D Muxed Read Access (RWSC = 5)

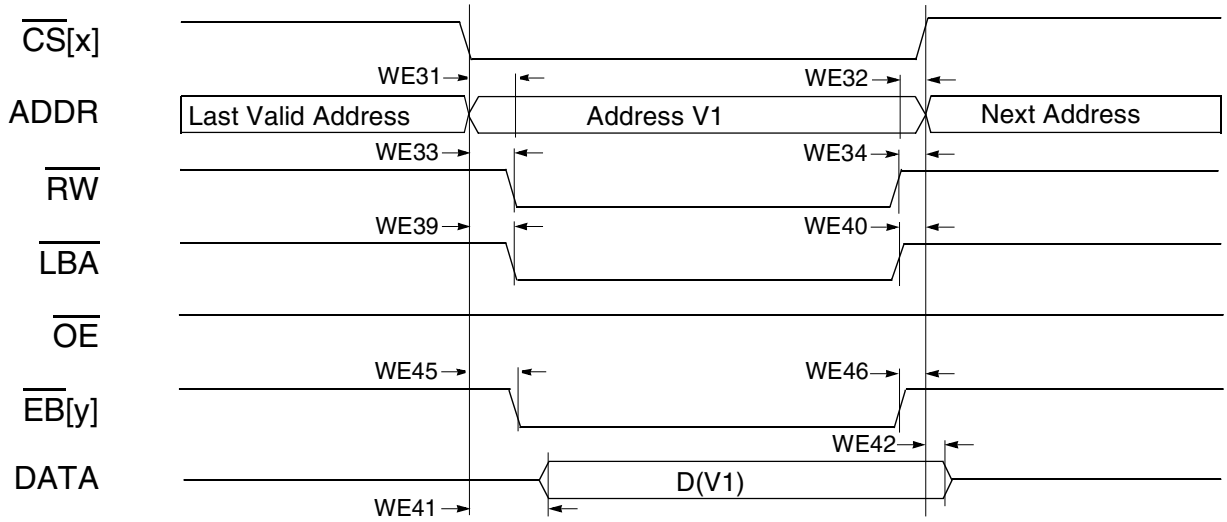

Figure 47. Asynchronous Memory Write Access

[1] For the value of parameters WE4–WE21, see column BCD = 0 in Table 56.
[2] $\overline{CS}$ Assertion. This bit field determines when the $\overline{CS}$ signal is asserted during read/write cycles.
[3] $\overline{CS}$ Negation. This bit field determines when the $\overline{CS}$ signal is negated during read/write cycles.
[4] $\overline{BE}$ Assertion. This bit field determines when the $\overline{BE}$ signal is asserted during read cycles.
[5] $\overline{BE}$ Negation. This bit field determines when the $\overline{BE}$ signal is negated during read cycles.
[6] Output maximum delay from internal driving ADDR/control FFs to chip outputs.
[7] Output maximum delay from $\overline{CS}$[x] internal driving FFs to $\overline{CS}$[x] out.
[8] DATA maximum delay from chip input data to its internal FF.
[9] DTACK maximum delay from chip dtack input to its internal FF.

NOTE

All configuration parameters (CSA, CSN, EBWA, EBWN, LBA, LBN, LAH, OEN, OEA, EBRA, and EBRN) are in cycle units.

3.7.9.1.5 MII Transmit Signal Timing (FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER, and FEC_TX_CLK)

The transmitter functions correctly up to an FEC_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the FEC_TX_CLK frequency.

Figure 56 shows MII transmit signal timings. Table 63 describes the timing parameters (M5–M8) shown in the figure.

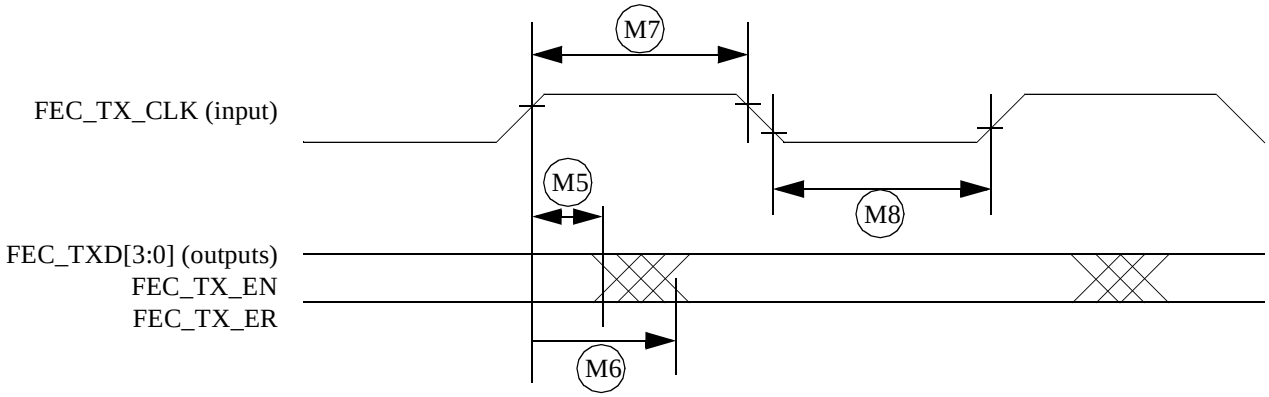

Figure 56. MII Transmit Signal Timing Diagram

Table 63. MII Transmit Signal Timing

ID	Characteristic[1]	Min.	Max.	Unit
M5	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER invalid	5	—	ns
M6	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER valid	—	20	ns
M7	FEC_TX_CLK pulse width high	35%	65%	FEC_TX_CLK period
M8	FEC_TX_CLK pulse width low	35%	65%	FEC_TX_CLK period

[1] FEC_TX_EN, FEC_TX_CLK, and FEC_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

3.7.9.1.6 MII Asynchronous Inputs Signal Timing (FEC_CRS and FEC_COL)

Figure 57 shows MII asynchronous input timings. Table 64 describes the timing parameter (M9) shown in the figure.

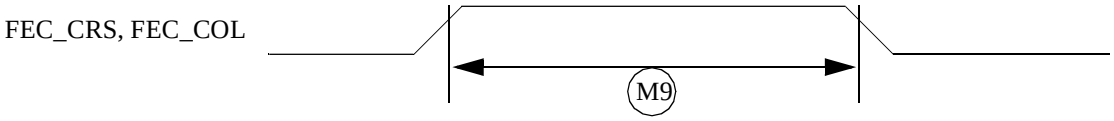

Figure 57. MII Async Inputs Timing Diagram

Table 85. Touchscreen ADC Electrical Specifications (continued)

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power-down current NVCC_ADC QV_{DD}	—	—	—	1 10	uA uA
Touchscreen Interface					
Expected plate resistance	—	100	—	1500	Ω
Switch drivers on resistance	GND and VDD switches	—	—	10	Ω
Conversion Characteristics[3]					
DNL[4]	fin = 1 kHz	—	+/–0.75	—	LSB
INL[4]	fin = 1 kHz	—	+/–2.0	—	LSB
Gain + Offset Error	—	—	—	+/–2	%FS

1 This comprises only the required initial dummy conversion cycle. Additional power-up time depends on the *enadc*, *reset* and *soc* signals applied to the touchscreen controller.

2 This value only includes the ADC and the driver switches, but it does not take into account the current consumption in the touchscreen plate. For example, if the plate resistance is 100 W, the total current consumption is about 33 mA.

3 At avdd = 3.3 V, dvdd = 1.2 V, Tjunction = 50 °C, fclk = 1.75 MHz, any process corner, unless otherwise noted.

4 Value measured with a –0.5 dBFS sinusoidal input signal and computed with the code density test.

3.7.18.2 ADC Timing Diagrams

Figure 82 represents the synchronization between the signals *clk*, *soc*, *eoc*, and the output bits in the usage of the internal ADC. After a conversion cycle *eoc* is asserted, a new conversion begins only when the

3.7.20.1.3 VP_VM Bidirectional Mode Timing

Table 94 defines the VP_VM bidirectional mode signals.

Table 94. Signal Definitions—VP_VM Bidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	• Transmit enable, active low
USB_DAT_VP	Out (Tx) In (Rx)	• Tx VP data when USB_TXOE_B is low • Rx VP data when USB_TXOE_B is high
USB_SE0_VM	Out (Tx) In (Rx)	• Tx VM data when USB_TXOE_B low • Rx VM data when USB_TXOE_B high
USB_RCV	In	• Differential Rx data

Figure 93 shows the USB transmit waveform in VP_VM bidirectional mode diagram.

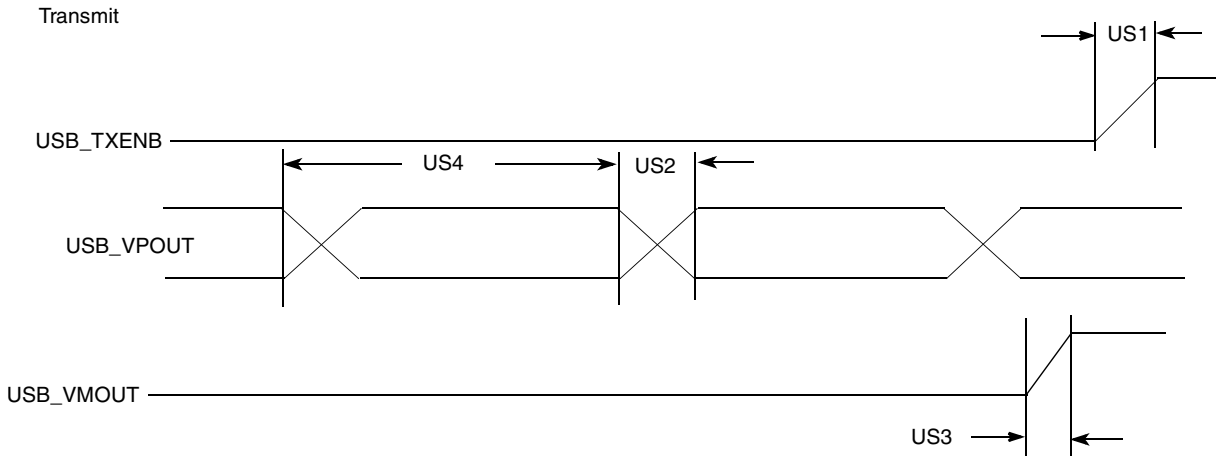

Figure 93. USB Transmit Waveform in VP_VM Bidirectional Mode

Figure 94 shows the USB receive waveform in VP_VM bidirectional mode diagram.

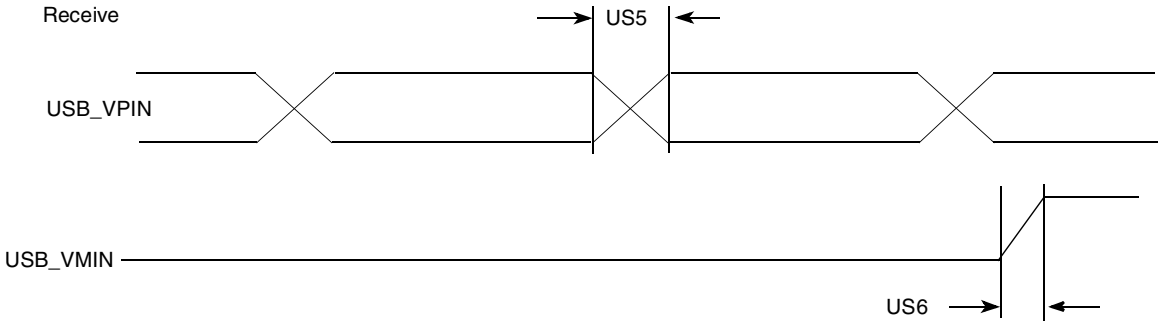

Figure 94. USB Receive Waveform in VP_VM Bidirectional Mode

Table 95 shows the USB port timing specification in VP_VM bidirectional mode.

Table 95. USB Port Timing Specifications in VP_VM Bidirectional Mode

No.	Parameter	Signal Name	Direction	Min.	Max.	Unit	Condition/ Reference Signal
US18	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US19	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US20	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US21	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US22	Tx high overlap	USB_SE0_VM	Out	0.0	—	ns	USB_DAT_VP
US23	Tx low overlap	USB_SE0_VM	Out	—	0.0	ns	USB_DAT_VP
US24	Enable delay	USB_DAT_VP USB_SE0_VM	In	—	8.0	ns	USB_TXOE_B
US25	Disable delay	USB_DAT_VP USB_SE0_VM	In	—	10.0	ns	USB_TXOE_B
US26	Rx rise/fall time	USB_DAT_VP	In	—	3.0	ns	35 pF
US27	Rx rise/fall time	USB_SE0_VM	In	—	3.0	ns	35 pF
US28	Rx skew	USB_DAT_VP	Out	–4.0	+4.0	ns	USB_SE0_VM
US29	Rx skew	USB_RCV	Out	–6.0	+2.0	ns	USB_DAT_VP

3.7.20.1.4 VP_VM Unidirectional Mode Timing

Table 96 defines the signals for USB in VP_VM unidirectional mode.

Table 96. Signal Definitions for USB VP_VM Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	Tx VP data when USB_TXOE_B is low
USB_SE0_VM	Out	Tx VM data when USB_TXOE_B is low
USB_VP1	In	Rx VP data when USB_TXOE_B is high
USB_VM1	In	Rx VM data when USB_TXOE_B is high
USB_RCV	In	Differential Rx data

Table 101. 17×17 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
SD3	D14	EMI1	DDR	INPUT	Keeper
SD4	D13	EMI1	DDR	INPUT	Keeper
SD5	A13	EMI1	DDR	INPUT	Keeper
SD6	D12	EMI1	DDR	INPUT	Keeper
SD7	A10	EMI1	DDR	INPUT	Keeper
SD8	B9	EMI1	DDR	INPUT	Keeper
SD9	D10	EMI1	DDR	INPUT	Keeper
SD10	B10	EMI1	DDR	INPUT	Keeper
SD11	C10	EMI1	DDR	INPUT	Keeper
SD12	C9	EMI1	DDR	INPUT	Keeper
SD13	A9	EMI1	DDR	INPUT	Keeper
SD14	D9	EMI1	DDR	INPUT	Keeper
SD15	A8	EMI1	DDR	INPUT	Keeper
SDBA1	A16	EMI2	DDR	OUTPUT	Low
SDBA0	B15	EMI2	DDR	OUTPUT	Low
DQM0	C12	EMI1	DDR	OUTPUT	High
DQM1	C8	EMI1	DDR	OUTPUT	High
RAS	C14	EMI2	DDR	OUTPUT	High
CAS	C16	EMI2	DDR	OUTPUT	High
SDWE	A15	EMI2	DDR	OUTPUT	High
SDCKE0	D15	EMI2	DDR	OUTPUT	High
SDCKE1	C15	EMI2	DDR	OUTPUT	High
SDCLK	B14	EMI2	DDR	OUTPUT	Low
SDCLK_B	A14	EMI2	DDR	OUTPUT	High
SDQS0	B12	EMI2	DDR	INPUT	Keeper
SDQS1	B8	EMI2	DDR	INPUT	Keeper
EB0	B3	EMI1	DDR	OUTPUT	High
EB1	C5	EMI1	DDR	OUTPUT	High
OE	D6	EMI1	DDR	OUTPUT	High
CS0	C3	EMI1	DDR	OUTPUT	High
CS1	D3	EMI1	DDR	OUTPUT	High
CS2	B16	EMI2	DDR	OUTPUT	High

Table 104. 12x12 mm Package Ground, Power Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
USBPHY1_VSSA	K19
USBPHY1_VSSA_BIAS	K18
USBPHY2_VDD	T16
USBPHY2_VSS	W16

[1] NVCC_DRYICE is a supply output. An external capacitor no less than 4 µF must be connected to it. A 4.7 µF capacitor is recommended.

4.7 Signal Contact Assignments—12 x 12 mm, 0.5 mm Pitch

Table 105 lists the 12×12 mm package i.MX25 signal contact assignments.

Table 105. 12x12 mm Package i.MX25 Signal Contact Assignment

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
A0	A20	EMI2	DDR	OUTPUT	Low
A1	A19	EMI2	DDR	OUTPUT	Low
A2	B18	EMI2	DDR	OUTPUT	Low
A3	D17	EMI2	DDR	OUTPUT	Low
A4	A21	EMI2	DDR	OUTPUT	Low
A5	B19	EMI2	DDR	OUTPUT	Low
A6	D18	EMI2	DDR	OUTPUT	Low
A7	B20	EMI2	DDR	OUTPUT	Low
A8	E19	EMI2	DDR	OUTPUT	Low
A9	D19	EMI2	DDR	OUTPUT	Low
A10	B5	EMI1	DDR	OUTPUT	Low
MA10	E17	EMI2	DDR	OUTPUT	Low
A11	C21	EMI2	DDR	OUTPUT	Low
A12	B22	EMI2	DDR	OUTPUT	Low
A13	D21	EMI2	DDR	OUTPUT	Low
A14	A4	EMI1	DDR	OUTPUT	Low
A15	D6	EMI1	DDR	OUTPUT	Low
A16	A5	EMI1	DDR	OUTPUT	Low
A17	E6	EMI1	DDR	OUTPUT	Low
A18	A6	EMI1	DDR	OUTPUT	Low
A19	E7	EMI1	DDR	OUTPUT	Low

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