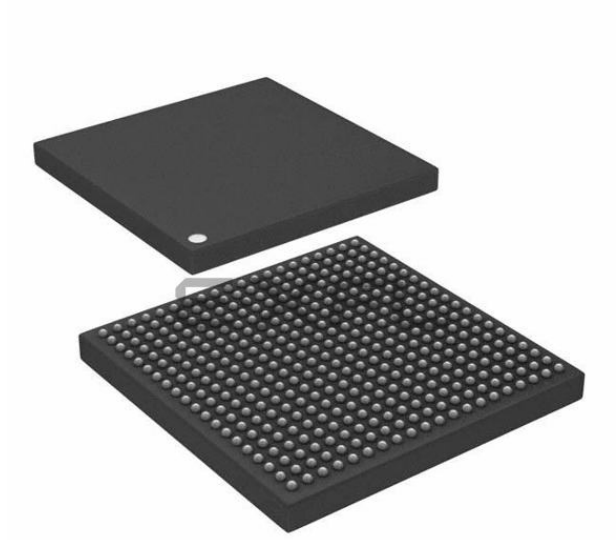

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-20°C ~ 70°C (TA)
Security Features	-
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx257dvm4

Table 2 shows the functional differences between the different parts in the i.MX25 family.

Table 2. i.MX25 Parts Functional Differences

Features	MCIMX253	MCIMX257	MCIMX258
Core	ARM 926EJ-S	ARM 926EJ-S	ARM 926EJ-S
CPU Speed	400 MHz	400 MHz	400 MHz
L1 I/D Cache	16K I/D	16K I/D	16K I/D
On-chip SRAM	128 KB	128 KB	128 KB
PATA/CE-ATA	Yes	Yes	Yes
LCD Controller	Yes	Yes	Yes
Touchscreen	—	Yes	Yes
CSI	—	Yes	Yes
FlexCAN (2)	—	Yes	Yes
ESAI	—	Yes	Yes
SIM (2)	—	Yes	Yes
Security	—	—	Yes
10/100 Ethernet	Yes	Yes	Yes
HS USB 2.0 OTG + PHY	Yes	Yes	Yes
HS USB 2.0 Host + PHY	Yes	Yes	Yes
12-bit ADC	Yes	Yes	Yes
SD/SDIO/MMC (2)	Yes	Yes	Yes
External Memory Controller	Yes	Yes	Yes
I^2C (3)	Yes	Yes	Yes
SSI/I2S (2)	Yes	Yes	Yes
CSPI (2)	Yes	Yes	Yes
UART (5)	Yes	Yes	Yes

Table 6. DC Operating Conditions (continued)

Parameter	Symbol	Min.	Typ.	Max.	Units
I/O supply voltage, GPIO CRM,LCDC,JTAG,MISC	NV_{DD_GPIO2}	3.0	3.3	3.6	—
I/O supply voltage DDR (Mobile DDR mode) EMI1, EMI2	NV_{DD_MDDR}	1.75	—	1.95	V
I/O supply voltage DDR (DDR2 mode) EMI1,EMI2	NV_{DD_DDR2}	1.75	—	1.9	V
I/O supply voltage DDR (SDRAM mode) EMI1,EMI2	NV_{DD_SDRAM}	1.75	—	3.6	V
Supply of USBPHY1 (HS) USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD,USBPHY1_VDDA	$V_{DD\_usbphy1}$	3.17	3.3	3.43	V
Supply of USBPHY2 (FS) USBPHY2_VDD	$V_{DD\_usbphy2}$	3.0	3.3	3.6	V
Supply of OSC24M OSC24M_VDD	V_{DD_OSC24M}	3.0	3.3	3.6	V
Supply of PLL MPLL_VDD,UPLL_VDD	V_{DD_PLL}	1.4	—	1.65	V
Supply of touchscreen ADC NVCC_ADC	V_{DD_tsc}	3.0	3.3	3.6	V
External reference of touchscreen ADC Ref	Vref	2.5	V_{DD_tsc}	V_{DD_tsc}	V
Fusebox program supply voltage FUSE_VDD[2]	$FUSEV_{DD}$ (program mode)	3.3 ± 5%	—	3.6	V
Supply output[3] NVCC_DRYICE	$V_{DD\_}$	1.0	—	1.55	V
Operating ambient temperature	T_A	–40	—	85	°C

1 V_{DD_BAT} must always be powered by battery in security application. In non-security case, V_{DD_BAT} can be connected to QV_{DD}.

2 The fusebox read supply is connected to supply of the full speed USBPHY2_VDD. FUSE_VDD is only used for programming. It is recommended that FUSE_VDD be connected to ground when not being used for programming. See Table 7 for current parameters.

3 NVCC_DRYICE is a supply output. An external capacitor no less than 4 µF must be connected to it. A 4.7 µF capacitor is recommended.

Table 14. iMX25 Reduced Power Mode Current Consumption

Power Group	Power Supply	Voltage Setting	Typical Current Consumption
BAT_VDD	BAT_VDD	1.15 V	9.95 µA
		1.55 V	12.6 µA

3.2 Supply Power-Up/Power-Down Requirements and Restrictions

Any i.MX25 board design must comply with the power-up and power-down sequence guidelines given in this section to ensure reliable operation of the device. Recommended power-up and power-down sequences are given in the following subsections.

CAUTION

Deviations from the guidelines in this section may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the i.MX25 (worst-case scenario)

NOTE

For security applications, the coin battery must be connected during both power-up and power-down sequences to ensure that security keys are not unintentionally erased.

3.2.1 Power-Up Sequence

For those users that are not using DryIce/SRTC, the following power-up sequence is recommended:

1. Assert power on reset (POR).
2. Turn on QVDD digital logic domain supplies.
3. Turn on NVCCx digital I/O power supplies after QVDD is stable.
4. Turn on all other analog power supplies, including USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD, USBPHY1_VDDA, USBPHY2_VDD, OSC24M_VDD, MPPLL_VDD, UPLL_VDD, NVCC_ADC, and FUSEVDD (FUSEVDD is tied to GND if fuses are not programmed), after all NVCCx digital I/O supplies are stable.
5. Negate the POR signal.

NOTE

This is to guarantee that POR is stable already at NVCC_CRM/QVDD power domain interface before QVDD is turned on, and POR instantly propagates to QVDD domain after QVDD is turned on.

4. Turn on other NVCCx digital I/O power supplies for not less than 1 ms and not more than 32 ms, after QVDD reaches 90% of 1.2 V.
5. Turn on all other analog power supplies, including USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD, USBPHY1_VDDA, USBPHY2_VDD, NVCC_ADC, OSC24M_VDD, MPPLL_VDD, UPLL_VDD, and FUSEVDD (FUSEVDD is tied to GND if fuses are not programmed) for not less than 1 ms and not more than 32 ms, after NVCCx reaches 90% of 3.3 V.

NOTE

This is to guarantee that analog peripherals can get properly initialized (reset) values from QVDD domain and NVCCx domain.

6. Negate the POR signal for at least 90 µs after all previous steps.

NOTE

- This is to guarantee that both POR logic and clocks are stable inside the i.MX25 chip, before POR is removed.
- The dV/dT should be no faster than 0.25 V/us for all power supplies, to avoid triggering ESD circuit.

In addition, the following power-down sequence is recommended:

1. Turn off power for analog parts, including USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD, USBPHY1_VDDA, USBPHY2_VDD, NVCC_ADC, and FUSEVDD (FUSEVDD is tied to GND if fuses are not programmed).
2. Turn off QVDD.
3. Turn off NVCCx, PLL, OSC, and other powers.

NOTE

The power-down steps can be executed simultaneously, or very shortly one after another.

3.3 Power Characteristics

Table 15 shows values representing maximum current numbers for the i.MX25 under worst case voltage and temperature conditions. These values are derived from the i.MX25 with core clock speed up to 400 MHz. Additionally, no power saving techniques such as clock gating were implemented when measuring these values. Common supplies are bundled according to the i.MX25 power-up sequence requirements. Peak numbers are provided for system designers so that the i.MX25 power supply requirements are satisfied during startup and transient conditions. Freescale recommends that system

Table 24. AC Parameters for Mobile DDR I/O (continued)

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Output pad propagation delay[1] (high drive), 40%–60%	tpo	15 pF 35 pF	1.04/1.09 1.63/1.56	1.73/1.83 2.43/2.52	2.69/2.62 3.79/3.62	ns
Output pad propagation delay[1] (standard drive), 40%–60%	tpo	15 pF 35 pF	1.50/1.74 2.73/2.42	2.36/2.41 3.77/3.78	3.67/3.46 5.86/5.37	ns
Output enable to output valid delay[1] (max. drive), 50%–50%	tpv	15 pF 35 pF	1.17/1.01 1.43/1.30	1.93/1.61 2.33/2.00	3.06/2.55 3.69/3.13	ns
Output enable to output valid delay[1] (high drive), 50%–50%	tpv	15 pF 35 pF	1.38/1.28 1.97/1.92	2.25/1.99 3.16/2.86	3.58/3.10 5.01/4.39	ns
Output enable to output valid delay[1] (standard drive), 50%–50%	tpv	15 pF 35 pF	1.92/1.57 3.12/3.16	3.11/2.79 4.97/4.59	4.98/4.13 7.97/6.98	ns
Output enable to output valid delay[1] (max. drive), 40%–60%	tpv	15 pF 35 pF	1.28/1.12 1.49/1.36	2.01/1.70 2.33/2.01	3.09/2.60 3.60/3.06	ns
Output enable to output valid delay[1] (high drive), 40%–60%	tpv	15 pF 35 pF	1.43/1.33 1.90/1.84	2.24/1.99 2.96/2.68	3.47/3.02 4.59/4.03	ns
Output enable to output valid delay[1] (standard drive), 40%–60%	tpv	15 pF 35 pF	1.85/1.78 2.80/2.81	2.91/2.62 4.37/4.53	4.54/3.96 6.88/6.05	ns
Output pad slew rate[2] (max. drive)	tps	25 pF 50 pF	0.80/0.92 0.43/0.50	1.35/1.50 0.72/0.81	2.23/2.27 1.66/1.68	V/ns
Output pad slew rate[2] (high drive)	tps	25 pF 50 pF	0.37/0.43 0.19/0.23	0.62/0.70 0.33/0.37	1.03/1.05 0.75/0.77	V/ns
Output pad slew rate[2] (standard drive)	tps	25 pF 50 pF	0.18/0.22 0.10/0.12	0.31/0.35 0.16/0.18	0.51/0.53 0.38/0.39	V/ns
Output pad dI/dt[3] (max. drive)	tdit	25 pF 50 pF	64 69	171 183	407 432	mA/ns
Output pad dI/dt[3] (high drive)	tdit	25 pF 50 pF	37 39	100 106	232 246	mA/ns
Output pad di/dt[3] (standard drive)	tdit	25 pF 50 pF	18 20	50 52	116 123	mA/ns
Input pad transition times[4]	trfi	1.0 pF	0.07/0.08	0.11/0.13	0.16/0.20	ns
Input pad propagation delay, 50%–50%[4]	tpi	1.0 pF	0.77/1.00	1.22/1.45	1.89/2.21	ns
Input pad propagation delay, 40%–60%[4]	tpi	1.0 pF	1.59/1.82	2.04/2.27	2.69/3.01	ns

1 Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from core is 1 ns (20%–80%).

2 Minimum condition for tps: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

3 Maximum condition for tdit: bcs model, 1.3 V, I/O 1.95 V, and –40 °C.

4 Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.65 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

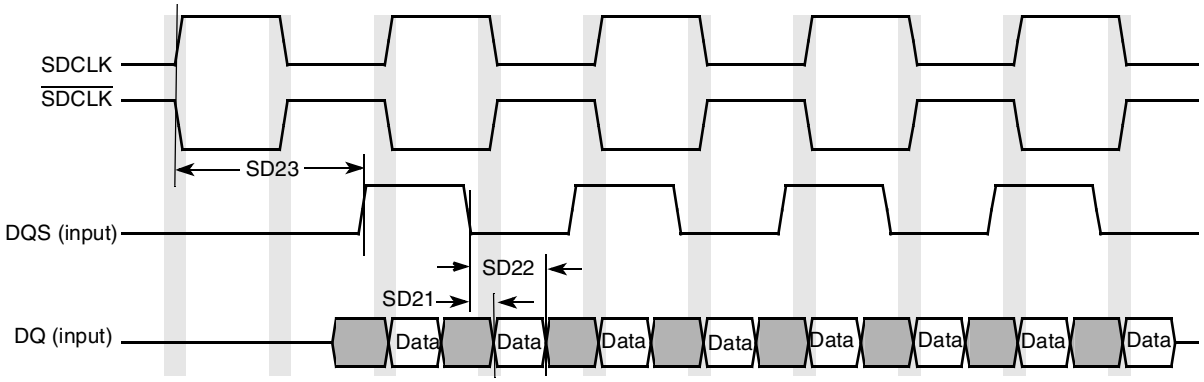


Figure 30. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 49. Mobile DDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD21	DQS – DQ Skew (defines the data valid window in read cycles related to DQS)	tDQSQ	—	0.85	ns
SD22	DQS DQ HOLD time from DQS	tQH	2.3	—	ns
SD23	DQS output access time from SDCLK posedge	tDQSCK	—	6.7	ns

Table 53. ΔtDS1, ΔtDH1 Derating Values for DDR2-400, DDR2-533[1,2,3] (continued)

		DQS Single-Ended Slew Rate																	
DQ Slew Rate V/ns	2.0	188	188	167	146	125	63	—	—	—	—	—	—	—	—	—	—	—	—
	1.5	146	167	125	125	83	42	81	43	—	—	—	—	—	—	—	—	—	—
	1.0	63	125	42	83	0	0	–2	1	–7	–13	—	—	—	—	—	—	—	—
	0.9	—	—	31	69	–11	–14	–13	–13	–18	–27	–29	–45	—	—	—	—	—	—
	0.8	—	—	—	—	–25	–31	–27	–30	–32	–44	–43	–62	–60	–86	—	—	—	—
	0.7	—	—	—	—	—	—	–45	–53	–50	–67	–61	–85	–78	–109	–108	–152	—	—
	0.6	—	—	—	—	—	—	—	—	–74	–96	–85	–114	–102	–138	–132	–181	–183	–246
	0.5	—	—	—	—	—	—	—	—	—	—	–128	–156	–145	–180	–175	–223	–226	–288
	0.4	—	—	—	—	—	—	—	—	—	—	—	—	–210	–243	–240	–286	–291	–351

1 All units in 'ps'.

2 Test conditions are at capacitance=15pF for DDR PADS. Recommended drive strengths are medium for SDCLK and high for address and controls.

3 SDRAM CLK and DQS related parameters are measured from the 50% point. That is, high is defined as 50% of the signal value, and low is defined as 50% of the signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and SDCLK (inverted clock).

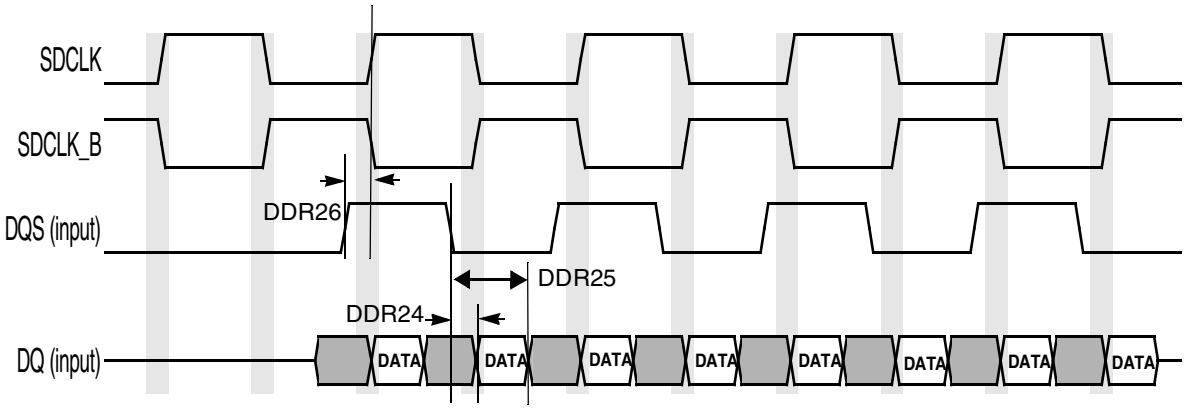


Figure 33. DDR2 SDRAM DQ vs. DQS and SDCLK READ Cycle Timing Diagram

Table 54. DDR2 SDRAM Read Cycle Parameter Table[1,2]

ID	Parameter	Symbol	DDR2-400		Unit
			Min.	Max.	
DDR24	DQS - DQ Skew (defines the Data valid window in read cycles related to DQS)	t_{DQSQ}	—	0.6	ns
DDR25	DQS DQ in HOLD time from DQS[3]	t_{QH}	2.5	—	ns
DDR26	DQS output access time from SDCLK posedge	t_{DQSCK}	–0.5	0.5	ns

1 Test conditions are at capacitance=15 pF for DDR PADS. Recommended drive strengths are medium for SDCLK and high for address and controls.

Table 56. WEIM Bus Timing Parameters[1] (continued)

ID	Parameter	Min.	Max.	Unit
WE8	Clock rise/fall to $\overline{RW}$ valid	8	12	ns
WE9	Clock rise/fall to $\overline{RW}$ invalid	3	8	ns
WE10	Clock rise/fall to $\overline{OE}$ valid	7	12	ns
WE11	Clock rise/fall to $\overline{OE}$ invalid	3.6	5.5	ns
WE12	Clock rise/fall to $\overline{EB}$[y] valid	6	11.5	ns
WE13	Clock rise/fall to $\overline{EB}$[y] invalid	6	10	ns
WE14	Clock rise/fall to $\overline{LBA}$ valid	17.5	20	ns
WE15	Clock rise/fall to $\overline{LBA}$ invalid	0	1	ns
WE16	Clock rise/fall to output data valid	5	10	ns
WE17	Clock rise to output data invalid	0	2.5	ns
WE18	Input data valid to clock rise, FCE=1	1	—	ns
WE19	Input Data Valid to Clock rise, FCE=0 (in the case there is $\overline{ECB}$ asserted during access)	1/2 BCLK +2.63	—	ns
	Input Data Valid to Clock rise, FCE=0 (in the case there is NO $\overline{ECB}$ asserted during access)	6.9	—	ns
WE20	Clock rise to input data invalid, FCE=1	1	—	ns
WE21	Clock rise to input data invalid, FCE=0	2.4	—	ns
WE22	$\overline{ECB}$ setup time, FCE=1	5	—	ns
WE23	$\overline{ECB}$ setup time, FCE=0	7.2	—	ns
WE24	$\overline{ECB}$ hold time, FCE=1	5	—	ns
WE25	$\overline{ECB}$ hold time, FCE=0	0	—	ns
WE26	$\overline{DTACK}$ setup time	5.4	—	ns
WE27	$\overline{DTACK}$ hold time	–3.2	—	ns

1 High is defined as 80% of signal value; low is defined as 20% of signal value.

2 BCLK parameters are being measured from the 50% point. For example, high is defined as 50% of signal value and low is defined as 50% as signal value.

NOTE

The test condition load capacitance was 25 pF. Recommended drive strength for all controls, address, and BCLK is maximum drive.

Recommended drive strength for all controls, address and BCLK is maximum drive.

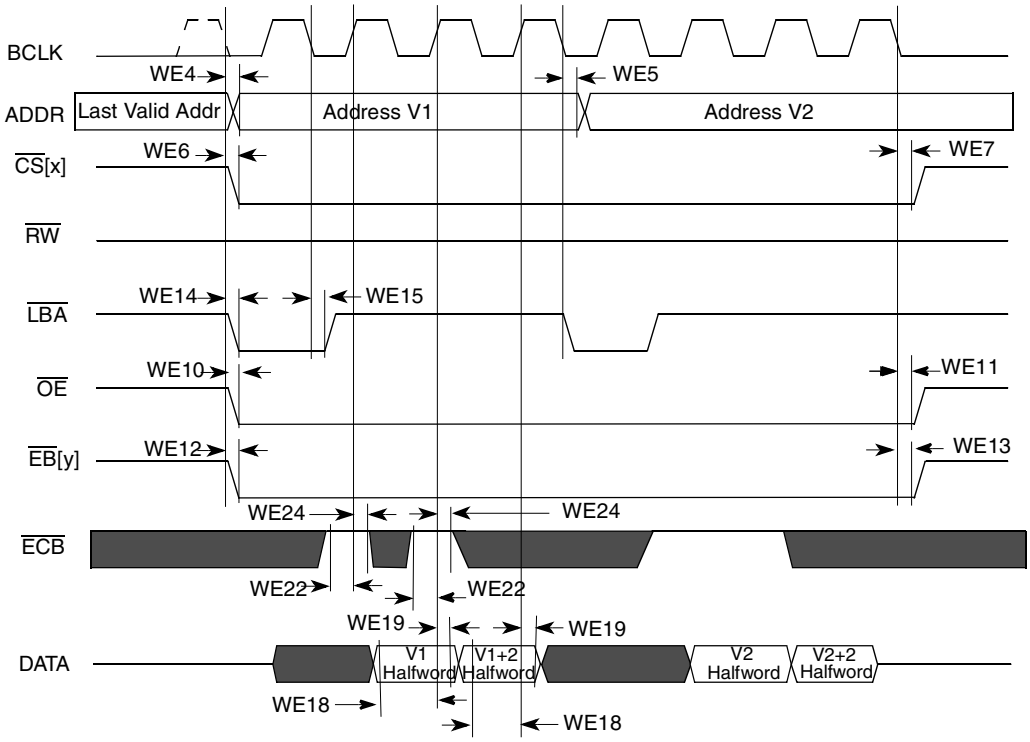


Figure 41. Synchronous Memory Timing Diagram for Two Non-Sequential Read Accesses—WSC=2, SYNC=1, DOL=0

Table 60. ESAI General Timing Requirements (continued)

No.	Characteristics[1 2]	Symbol	Expression[3]	Min.	Max.	Condition	Unit
65	SCKR rising edge to FSR out (bl) high	—	—	— —	17.0 7.0	x ck i ck a	ns
66	SCKR rising edge to FSR out (bl) low	—	—	— —	17.0 7.0	x ck i ck a	ns
67	SCKR rising edge to FSR out (wr) high[5]	—	—	— —	19.0 9.0	x ck i ck a	ns
68	SCKR rising edge to FSR out (wr) low[5]	—	—	— —	19.0 9.0	x ck i ck a	ns
69	SCKR rising edge to FSR out (wl) high	—	—	— —	16.0 6.0	x ck i ck a	ns
70	SCKR rising edge to FSR out (wl) low	—	—	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before SCKR (SCK in synchronous mode) falling edge	—	—	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR falling edge	—	—	3.5 9.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR falling edge[5]	—	—	2.0 12.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR falling edge	—	—	2.0 12.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR falling edge	—	—	2.5 8.5	— —	x ck i ck a	ns
76	Flags input setup before SCKR falling edge	—	—	0.0 19.0	— —	x ck i ck s	ns
77	Flags input hold time after SCKR falling edge	—	—	6.0 0.0	— —	x ck i ck s	ns
78	SCKT rising edge to FST out (bl) high	—	—	— —	18.0 8.0	x ck i ck	ns
79	SCKT rising edge to FST out (bl) low	—	—	— —	20.0 10.0	x ck i ck	ns
80	SCKT rising edge to FST out (wr) high[5]	—	—	— —	20.0 10.0	x ck i ck	ns
81	SCKT rising edge to FST out (wr) low[5]	—	—	— —	22.0 12.0	x ck i ck	ns
82	SCKT rising edge to FST out (wl) high	—	—	— —	19.0 9.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	—	—	— —	20.0 10.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	—	—	— —	22.0 17.0	x ck i ck	ns
85	SCKT rising edge to transmitter #0 drive enable assertion	—	—	— —	17.0 11.0	x ck i ck	ns

3.7.12 Liquid Crystal Display Controller (LCDC) Timing

Figure 65 and Figure 66 show LCDC timing in non-TFT and TFT mode respectively, and Table 71 and Table 72 list the timing parameters used in the associated figures.

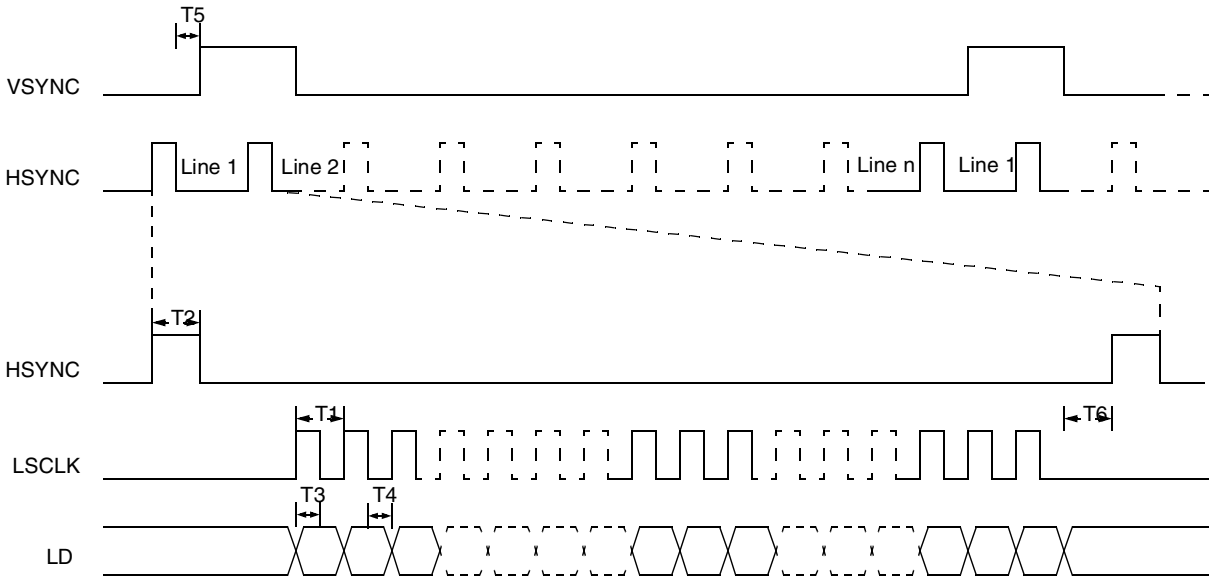


Figure 65. LCDC Non-TFT Mode Timing Diagram

Table 71. LCDC Non-TFT Mode Timing Parameters

ID	Description	Min.	Max.	Unit
T1	Pixel clock period	22.5	1000	ns
T2	HSYNC width	1	—	T[1]
T3	LD setup time	5	—	ns
T4	LD hold time	5	—	ns
T5	Wait between HSYNC and VSYNC rising edge	2	—	T[1]
T6	Wait between last data and HSYNC rising edge	1	—	T[1]

1 T is pixel clock period

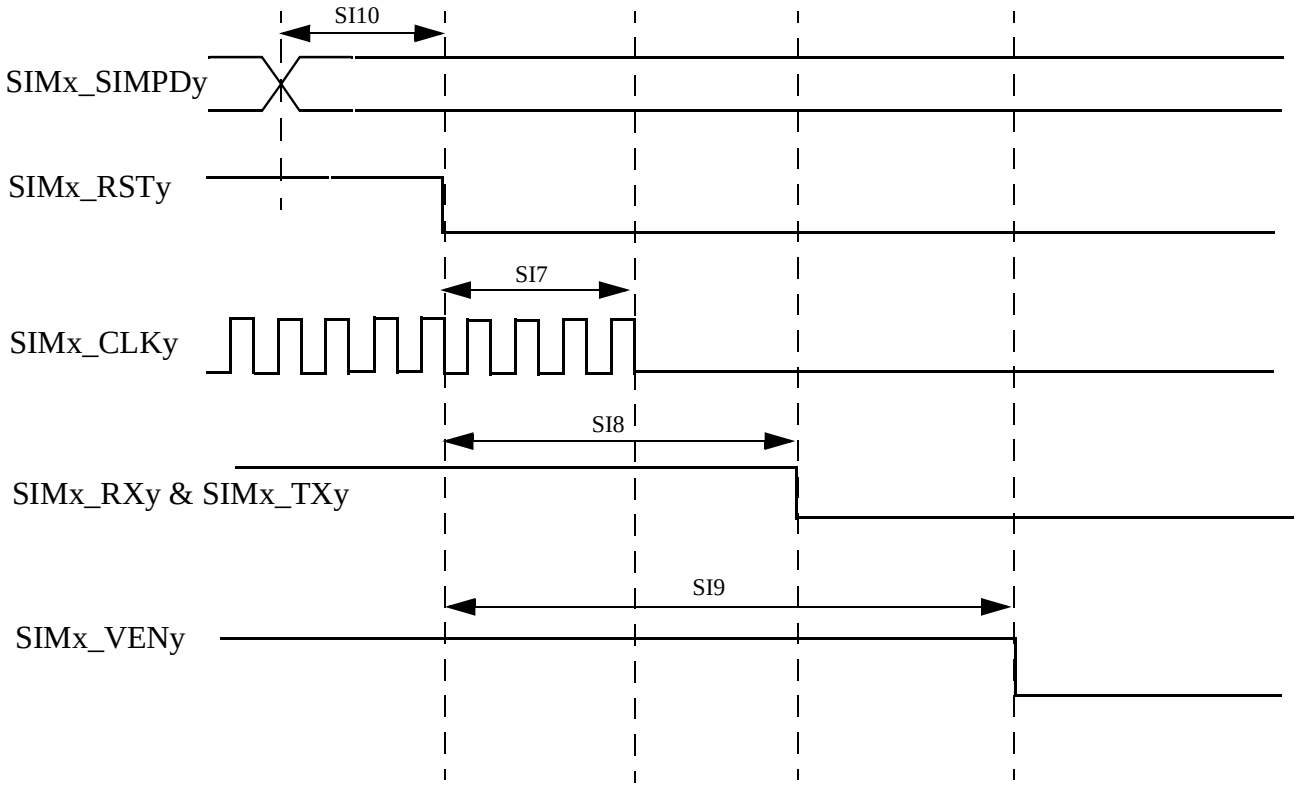


Figure 71. SmartCard Interface Power Down AC Timing

Table 77. Timing Requirements for Power-down Sequence

ID	PARAMETER	SYMBOL	Min.	Max.	Unit
SI7	SIM reset to SIM clock stop	$S_{rst2clk}$	0.9 × 1/Fckil	1.1 × 1/Fckil	ns
SI8	SIM reset to SIM Tx data low	$S_{rst2dat}$	1.8 × 1/Fckil	2.2 × 1/Fckil	ns
SI9	SIM reset to SIM voltage enable low	$S_{rst2ven}$	2.7 × 1/Fckil	3.3 × 1/Fckil	ns
SI10	SIM presence detect to SIM reset low	S_{pd2rst}	0.9 × 1/Fckil	1.1 × 1/Fckil	ns

3.7.15 System JTAG Controller (SJC) Timing

Figure 72 through Figure 75 show respectively the test clock input, boundary scan, test access port, and TRST timings for the SJC. Table 78 describes the SJC timing parameters (SJ1–SJ13) indicated in the figures.

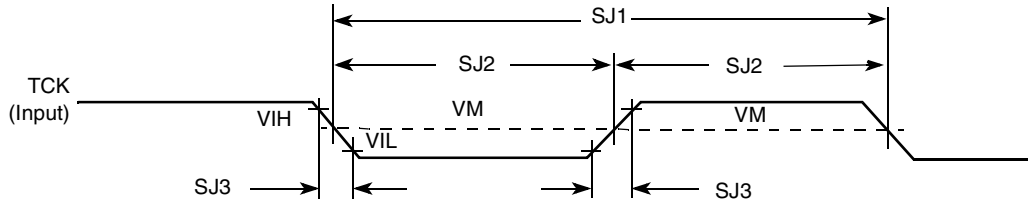


Figure 72. Test Clock Input Timing Diagram

3.7.17.2 SSI Receiver Timing with Internal Clock

Figure 79 shows the timing for the SSI receiver with internal clock. Table 82 describes the timing parameters (SS1–SS51) shown in the figure.

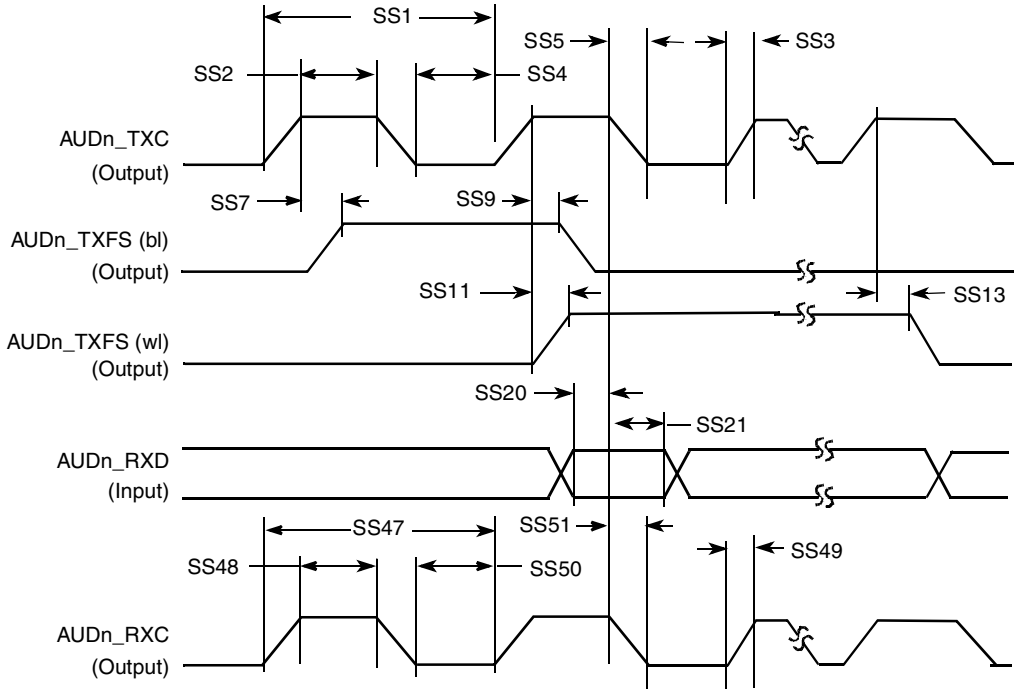


Figure 79. SSI Receiver Internal Clock Timing Diagram

Table 82. SSI Receiver Timing with Internal Clock

ID	Parameter	Min.	Max.	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	10.0	—	ns
SS21	SRXD hold time after (Rx) CK low	0.0	—	ns
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns

Table 82. SSI Receiver Timing with Internal Clock (continued)

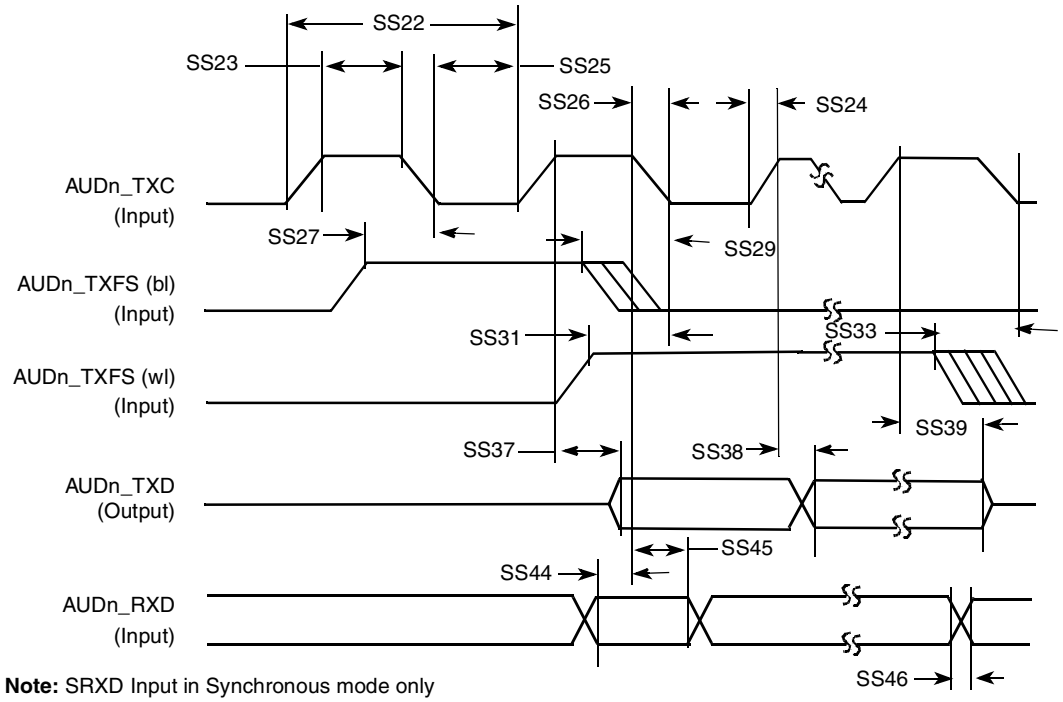
ID	Parameter	Min.	Max.	Unit
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

Note:

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on pads when SSI is being used for a data transfer.
- ”Tx” and “Rx” refer to the transmit and receive sections of the SSI.
- For internal frame sync operation using external clock, the FS timing is the same as that of Tx Data (for example, during AC97 mode of operation).

3.7.17.3 SSI Transmitter Timing with External Clock

Figure 80 shows the timing for the SSI transmitter with external clock. Table 83 describes the timing parameters (SS22-SS46) shown in the figure.



Note: SRXD Input in Synchronous mode only

Figure 80. SSI Transmitter with External Clock Timing Diagram

Table 85. Touchscreen ADC Electrical Specifications (continued)

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power-down current NVCC_ADC QV_{DD}	—	—	—	1 10	uA uA
Touchscreen Interface					
Expected plate resistance	—	100	—	1500	Ω
Switch drivers on resistance	GND and VDD switches	—	—	10	Ω
Conversion Characteristics[3]					
DNL[4]	fin = 1 kHz	—	+/–0.75	—	LSB
INL[4]	fin = 1 kHz	—	+/–2.0	—	LSB
Gain + Offset Error	—	—	—	+/–2	%FS

1 This comprises only the required initial dummy conversion cycle. Additional power-up time depends on the *enadc*, *reset* and *soc* signals applied to the touchscreen controller.

2 This value only includes the ADC and the driver switches, but it does not take into account the current consumption in the touchscreen plate. For example, if the plate resistance is 100 W, the total current consumption is about 33 mA.

3 At avdd = 3.3 V, dvdd = 1.2 V, Tjunction = 50 °C, fclk = 1.75 MHz, any process corner, unless otherwise noted.

4 Value measured with a –0.5 dBFS sinusoidal input signal and computed with the code density test.

3.7.18.2 ADC Timing Diagrams

Figure 82 represents the synchronization between the signals *clk*, *soc*, *eoc*, and the output bits in the usage of the internal ADC. After a conversion cycle *eoc* is asserted, a new conversion begins only when the

assertion of *soc* is detected. Thus, if the *soc* signal is continuously asserted, the ADC undergoes successive conversion cycles and achieves the maximum sampling rate. If *soc* is negated, no conversion is initiated.

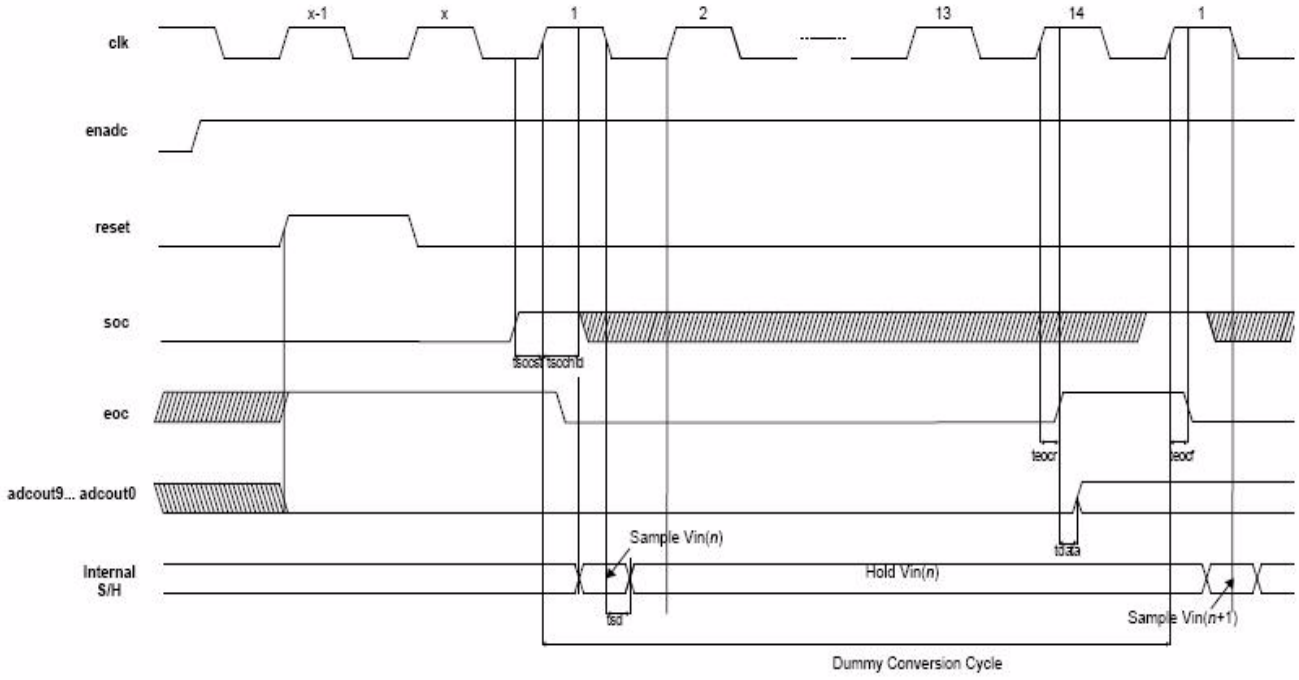


Figure 82. Start-up Sequence

The output data can be read from *adcout11...adcout0*, and is available *tdata* nanoseconds after the rising edge of *eoc*. The *reset* signal and the digital signals controlling the analog switches (*ypsw, xpsw, ynsw, xnsw*) are totally asynchronous.

The following conditions are necessary to guarantee the correct operation of the ADC:

- The input multiplexer selection (*selin11…selin0*) is stable during both the last clock cycle (14^{th}) and the first clock cycle (1^{st}). The best way to guarantee this is to make the input multiplexer selection during clock cycles 2 to 13.
- The references are stable during clock cycle 1 to 13. The best way to guarantee this is to make the reference multiplexer selection (*selrefp* and *selrefn*) before issuing an *soc* pulse and changing it only after an *eoc* pulse has been acquired, during the last clock cycle (14).

3.7.20.1.3 VP_VM Bidirectional Mode Timing

Table 94 defines the VP_VM bidirectional mode signals.

Table 94. Signal Definitions—VP_VM Bidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	• Transmit enable, active low
USB_DAT_VP	Out (Tx) In (Rx)	• Tx VP data when USB_TXOE_B is low • Rx VP data when USB_TXOE_B is high
USB_SE0_VM	Out (Tx) In (Rx)	• Tx VM data when USB_TXOE_B low • Rx VM data when USB_TXOE_B high
USB_RCV	In	• Differential Rx data

Figure 93 shows the USB transmit waveform in VP_VM bidirectional mode diagram.

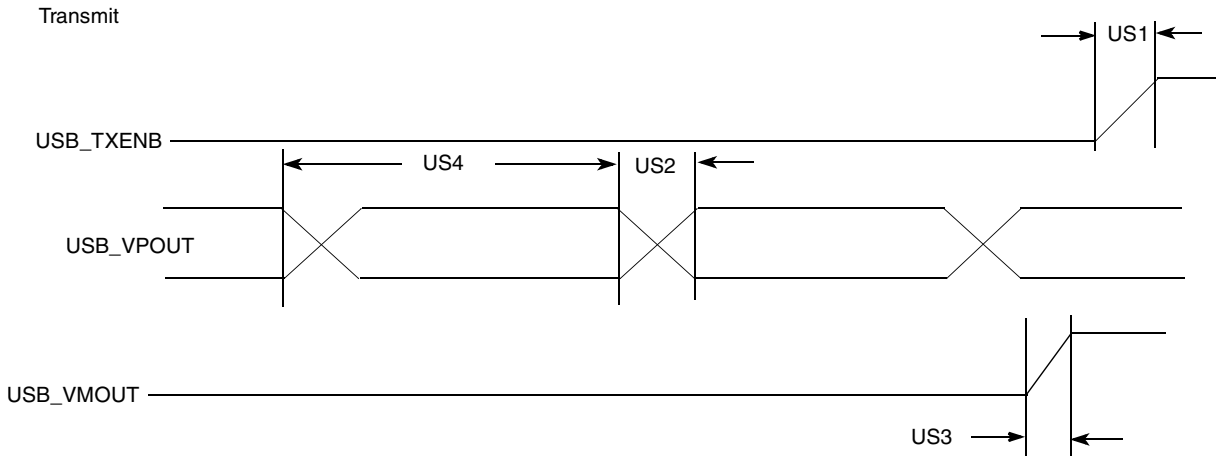


Figure 93. USB Transmit Waveform in VP_VM Bidirectional Mode

Figure 94 shows the USB receive waveform in VP_VM bidirectional mode diagram.

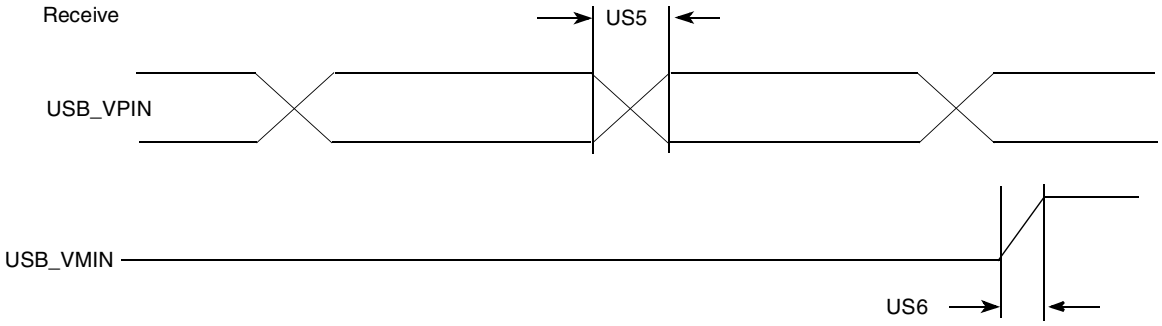


Figure 94. USB Receive Waveform in VP_VM Bidirectional Mode

Table 103. i.MX25 17×17 Package Ball Map (continued)

	T	R	P	N	M	L	K
1	UART2_TXD	KPP_ROW1	KPP_COL0	KPP_COL3	FEC_RDATA0	FEC_MDC	QGND
2	UART1_CTS	UART2_CTS	KPP_ROW3	KPP_COL2	FEC_TX_EN	FEC_MDIO	QGND
3	UART1_RTS	UART2_RTS	KPP_ROW2	KPP_COL1	FEC_RX_DV	FEC_TDATA0	QGND
4	CSPI1_MOSI	CSPI1_SS0	UART2_RXD	KPP_ROW0	FEC_RDATA1	FEC_TX_CLK	QGND
5	QGND	QGND	QGND	NVCC_MISC	QVDD	QGND	QGND
6	QGND	NVCC_LCDC	NVCC_LCDC	NVCC_MISC	QVDD	NVCC_NFC	QVDD
7	QGND	NVCC_LCDC	NVCC_LCDC	NVCC_MISC	QVDD	NVCC_NFC	QVDD
8	QGND	QGND	QVDD	QVDD	QGND	NVCC_NFC	QGND
9	QGND	QGND	QVDD	QGND	QGND	QGND	QGND
10	QGND	QGND	BAT_VDD	TAMPER_A	QGND	QGND	QGND
11	QGND	QGND	MESH_C	TAMPER_B	QGND	QGND	QGND
12	QGND	QGND	MESH_D	QGND	QGND	QGND	QVDD
13	QGND	QGND	QGND	QGND	QGND	QGND	QGND
14	QGND	QGND	QGND	NVCC_CRM	QGND	QGND	QGND
15	QGND	QGND	QGND	QGND	QGND	QGND	QGND
16	QGND	QGND	QGND	QGND	UPLL_GND	UPLL_VDD	USBPHY1_VDDA
17	FUSE_VDD	NVCC_SDIO	GPIO_C	USBPHY1_UPLLVSS	USBPHY1_UPLLVDD	USBPHY1_RREF	USBPHY1_VBUS
18	RESET_B	VSTBY_REQ	GPIO_E	GPIO_B	NC_BGA_M18	USBPHY1_DP	USBPHY1_DM
19	POWER_FAIL	GPIO_F	GPIO_D	GPIO_A	SD1_DATA2	USBPHY1_VSSA	USBPHY1_VDDA_BIAS
20	VSTBY_ACK	EXT_ARMCLK	NC_BGA_P20	SD1_DATA1	SD1_CLK	SD1_DATA0	SD1_CMD

Table 104. 12x12 mm Package Ground, Power Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
USBPHY1_VSSA	K19
USBPHY1_VSSA_BIAS	K18
USBPHY2_VDD	T16
USBPHY2_VSS	W16

[1] NVCC_DRYICE is a supply output. An external capacitor no less than 4 µF must be connected to it. A 4.7 µF capacitor is recommended.

4.7 Signal Contact Assignments—12 x 12 mm, 0.5 mm Pitch

Table 105 lists the 12×12 mm package i.MX25 signal contact assignments.

Table 105. 12x12 mm Package i.MX25 Signal Contact Assignment

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
A0	A20	EMI2	DDR	OUTPUT	Low
A1	A19	EMI2	DDR	OUTPUT	Low
A2	B18	EMI2	DDR	OUTPUT	Low
A3	D17	EMI2	DDR	OUTPUT	Low
A4	A21	EMI2	DDR	OUTPUT	Low
A5	B19	EMI2	DDR	OUTPUT	Low
A6	D18	EMI2	DDR	OUTPUT	Low
A7	B20	EMI2	DDR	OUTPUT	Low
A8	E19	EMI2	DDR	OUTPUT	Low
A9	D19	EMI2	DDR	OUTPUT	Low
A10	B5	EMI1	DDR	OUTPUT	Low
MA10	E17	EMI2	DDR	OUTPUT	Low
A11	C21	EMI2	DDR	OUTPUT	Low
A12	B22	EMI2	DDR	OUTPUT	Low
A13	D21	EMI2	DDR	OUTPUT	Low
A14	A4	EMI1	DDR	OUTPUT	Low
A15	D6	EMI1	DDR	OUTPUT	Low
A16	A5	EMI1	DDR	OUTPUT	Low
A17	E6	EMI1	DDR	OUTPUT	Low
A18	A6	EMI1	DDR	OUTPUT	Low
A19	E7	EMI1	DDR	OUTPUT	Low

Table 105. 12x12 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
D7	L1	NFC	GPIO	INPUT	Keeper
D6	K1	NFC	GPIO	INPUT	Keeper
D5	J1	NFC	GPIO	INPUT	Keeper
D4	H2	NFC	GPIO	INPUT	Keeper
D3	H1	NFC	GPIO	INPUT	Keeper
D2	G1	NFC	GPIO	INPUT	Keeper
D1	F1	NFC	GPIO	INPUT	Keeper
D0	F2	NFC	GPIO	INPUT	Keeper
LD0[2]	AB10	LCDC	GPIO	OUTPUT	Low
LD1[2]	W8	LCDC	GPIO	OUTPUT	Low
LD2[2]	AB9	LCDC	GPIO	OUTPUT	Low
LD3[2]	AA9	LCDC	GPIO	OUTPUT	Low
LD4[2]	AB8	LCDC	GPIO	OUTPUT	Low
LD5[2]	AA8	LCDC	GPIO	OUTPUT	Low
LD6[2]	AB7	LCDC	GPIO	OUTPUT	Low
LD7[2]	AA7	LCDC	GPIO	OUTPUT	Low
LD8[2]	AB6	LCDC	GPIO	OUTPUT	Low
LD9[2]	AA6	LCDC	GPIO	OUTPUT	Low
LD10[2]	AB5	LCDC	GPIO	OUTPUT	Low
LD11[2]	W7	LCDC	GPIO	OUTPUT	Low
LD12[2]	AB4	LCDC	GPIO	OUTPUT	Low
LD13[2]	W6	LCDC	GPIO	OUTPUT	Low
LD14[2]	AB3	LCDC	GPIO	OUTPUT	Low
LD15[2]	AA5	LCDC	GPIO	OUTPUT	Low
HSYNC[2]	AA4	LCDC	GPIO	OUTPUT	Low
VSYNC[2]	W5	LCDC	GPIO	OUTPUT	Low
LSCLK[2]	AB2	LCDC	GPIO	OUTPUT	Low
OE_ACD[2]	AA3	LCDC	GPIO	OUTPUT	Low
CONTRAST	Y2	LCDC	GPIO	OUTPUT	Low
PWM[2]	W4	LCDC	GPIO	INPUT	100 KΩ Pull-Down
CSI_D2	C22	CSI	GPIO	INPUT	Keeper