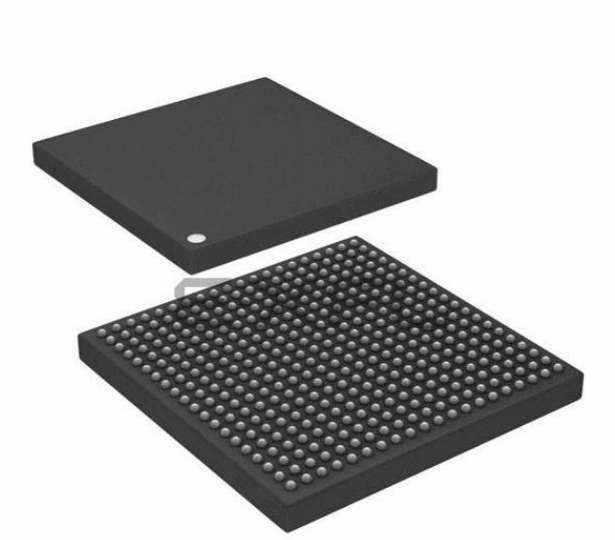

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Boot Security, Cryptography, Secure Fusebox, Secure JTAG, Secure Memory, Tamper Detection
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx258cjm4

Table 4. Signal Considerations (continued)

Signal	Description
MESH_C, MESH_D	Wire-mesh tamper detect pins that can be routed at the PCB board to detect attempted tampering of a protected wire. When security measures are implemented, MESH_C should be pulled-up or connected to NVCC_DRYICE and triggers a tamper event when floating or when connected to MESH_D. MESH_D should be pulled-down or connected to GND and triggers an event when floating or connected to MESH_C. These pins can be left unconnected if the DryIce security features are not being used.
NVCC_DRYICE	This is the DryIce power supply output. The supply source is QVDD when the i.MX25 is in run mode. When i.MX25 is in reduced power mode, the DryIce supply source is the BATT_VDD supply. This pin can be used to power external DryIce components (external tamper detect, wire-mesh tamper detect). In order to guarantee the power-loss protection feature which guarantees that RTC and/or secure keys be maintained after power-off an external capacitor no less than 4 µF must be connected to this supply output pin. A 4.7 µF capacitor is recommended.
OSC_BYP	The 32 kHz oscillator bypass-control pin. If this signal is pulled down, then OSC32K_EXTAL and OSC32K_XTAL analog pins should be tied to the external 32.768 kHz crystal circuit. If on the other hand the signal is pulled up, then the external 32 kHz oscillator output clock must be connected to OSC32K_EXTAL analog pin, and OSC32K_XTAL can be no connect (NC).
OSC32K_EXTAL OSC32K_XTAL	These analog pins are connected to an external 32 kHz CLK circuit depending on the state of OSC_BYP pin (see the description of OSC_BYP under the preceding bullet). The 32 kHz reference CLK is required for normal operation.
POWER_FAIL	An interrupt from PMIC, which should be connected to a low-battery detection circuit. This signal is internally connected to an on-chip 100 kΩ pull-down device. If there is no low-battery detection, then users can tie this pin to GND through a pull-down resistor, or leave the signal as NC. This pin can also be configured to work as a normal GPIO.
REF	External ADC reference voltage. REF may be tied to GND if the user plans to only use the internally generated 2.5 V reference supply.
SJC_MOD	Must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed, but the value should be much smaller than the on-chip 100 kΩ pull-up.
TAMPER_A, TAMPER _B	DryIce external tamper detect pins, active high. If TAMPER_A or TAMPER_B is connected to NVCC_DRYICE, then external tampering is detected. These pins can be left unconnected if the DryIce security features are not being used.
TEST_MODE	For Freescale factory use only. This signal is internally connected to an on-chip pull-down device. Users must either float this signal or tie it to GND.
UPLL_BYPCLK	Primarily for Freescale factory use. There is no internal on-chip pull-up/down on this pin, so it must be externally connected to GND or VDD. Aside from factory use, this pin can also be configured (through muxing) to work as a normal GPIO.
USBPHY1_RREF	Determines the reference current for the USB PHY1 bandgap reference. An external 10 kΩ 1% resistor to GND is required.
USBPHY2_DM USBPHY2_DP	The output impedance of these signals is expected at 10 Ω. It is recommended to also have on-board 33 Ω series resistors (close to the pins).

Table 6. DC Operating Conditions (continued)

Parameter	Symbol	Min.	Typ.	Max.	Units
I/O supply voltage, GPIO CRM,LCDC,JTAG,MISC	NV_{DD_GPIO2}	3.0	3.3	3.6	—
I/O supply voltage DDR (Mobile DDR mode) EMI1, EMI2	NV_{DD_MDDR}	1.75	—	1.95	V
I/O supply voltage DDR (DDR2 mode) EMI1,EMI2	NV_{DD_DDR2}	1.75	—	1.9	V
I/O supply voltage DDR (SDRAM mode) EMI1,EMI2	NV_{DD_SDRAM}	1.75	—	3.6	V
Supply of USBPHY1 (HS) USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD,USBPHY1_VDDA	$V_{DD\_usbphy1}$	3.17	3.3	3.43	V
Supply of USBPHY2 (FS) USBPHY2_VDD	$V_{DD\_usbphy2}$	3.0	3.3	3.6	V
Supply of OSC24M OSC24M_VDD	V_{DD_OSC24M}	3.0	3.3	3.6	V
Supply of PLL MPLL_VDD,UPLL_VDD	V_{DD_PLL}	1.4	—	1.65	V
Supply of touchscreen ADC NVCC_ADC	V_{DD_tsc}	3.0	3.3	3.6	V
External reference of touchscreen ADC Ref	Vref	2.5	V_{DD_tsc}	V_{DD_tsc}	V
Fusebox program supply voltage FUSE_VDD[2]	$FUSEV_{DD}$ (program mode)	3.3 ± 5%	—	3.6	V
Supply output[3] NVCC_DRYICE	$V_{DD\_}$	1.0	—	1.55	V
Operating ambient temperature	T_A	–40	—	85	°C

1 V_{DD_BAT} must always be powered by battery in security application. In non-security case, V_{DD_BAT} can be connected to QV_{DD}.

2 The fusebox read supply is connected to supply of the full speed USBPHY2_VDD. FUSE_VDD is only used for programming. It is recommended that FUSE_VDD be connected to ground when not being used for programming. See Table 7 for current parameters.

3 NVCC_DRYICE is a supply output. An external capacitor no less than 4 µF must be connected to it. A 4.7 µF capacitor is recommended.

[1] Sleep mode differs from stop mode in that the core voltage is reduced to 1 V.

Table 13 shows typical current consumption for the various power supplies under the various power modes.

Table 13. i.MX25 Power Mode Current Consumption

Power Group	Power Supplies	Voltage Setting	Current Consumption for Power Modes[1]			
			Doze	Wait	Stop	Sleep
NVCC_EMI	NVCC_EMI1 NVCC_EMI2	3.0 V	5 µA	3.15 µA	3.51 µA	3.61 µA
NVCC_CRM	NVCC_CRM	3.0 V	1.15 µA	4.31 µA	0.267 µA	0.32 µA
NVCC_ OTHER	NVCC_SDIO NVCC_CSI NVCC_NFC NVCC_JTAG NVCC_LCDC NVCC_MISC	3.0 V	31.2 µA	29.5 µA	31.7 µA	32.1 µA
NVCC_ADC	NVCC_ADC	3.0 V	163 µA	3.25 µA	1.14 µA	0.871 µA
OSC24M	OSC24M_ VDD	3.0 V	906 µA	903 µA	10.2 µA mA	10.5 µA
PLL_VDD	MPLL_VDD UPLL_VDD	1.4 V	6.83 mA	6.83 mA	38.9 µA	39.1 µA
QVDD	QVDD	1.15 V	8.79 mA	11.28 mA	842 µA	665 µA
USBPHY1_ VDDA	USBPHY1_ VDDA	3.17 V	240 µA	240 µA	241 µA	242 µA
USBPHY1_ VDDA_VBIAS	USBPHY1_ VDDA_VBIAS	3.17 V	0.6 µA	1.46 µA	0.328 µA	0.231 µA
USBPHY1_ UPLL_VDD	USBPHY1_ UPLL_VDD	3.17 V	201 µA	201 µA	191 µA	191 µA
USBPHY2	USBPHY2_ VDD	3.0 V	158 µA	0158 µA	164 µA	164 µA

[1] Values are typical, under typical use conditions.

In the reduced power mode, shown in Table 14, the i.MX25 is powered down, while the RTC clock and the secure keys (in secure-use case), remain operational. BAT_VDD is tied to a battery while all other supplies are turned off.

NOTE

In this low-power mode, i.MX25 cannot be woken up with an interrupt; it must be powered back up before it can detect any events.

NOTE

This is to guarantee that POR is stable already at NVCC_CRM/QVDD power domain interface before QVDD is turned on, and POR instantly propagates to QVDD domain after QVDD is turned on.

4. Turn on other NVCCx digital I/O power supplies for not less than 1 ms and not more than 32 ms, after QVDD reaches 90% of 1.2 V.
5. Turn on all other analog power supplies, including USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD, USBPHY1_VDDA, USBPHY2_VDD, NVCC_ADC, OSC24M_VDD, MPPLL_VDD, UPLL_VDD, and FUSEVDD (FUSEVDD is tied to GND if fuses are not programmed) for not less than 1 ms and not more than 32 ms, after NVCCx reaches 90% of 3.3 V.

NOTE

This is to guarantee that analog peripherals can get properly initialized (reset) values from QVDD domain and NVCCx domain.

6. Negate the POR signal for at least 90 µs after all previous steps.

NOTE

- This is to guarantee that both POR logic and clocks are stable inside the i.MX25 chip, before POR is removed.
- The dV/dT should be no faster than 0.25 V/us for all power supplies, to avoid triggering ESD circuit.

In addition, the following power-down sequence is recommended:

1. Turn off power for analog parts, including USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD, USBPHY1_VDDA, USBPHY2_VDD, NVCC_ADC, and FUSEVDD (FUSEVDD is tied to GND if fuses are not programmed).
2. Turn off QVDD.
3. Turn off NVCCx, PLL, OSC, and other powers.

NOTE

The power-down steps can be executed simultaneously, or very shortly one after another.

3.3 Power Characteristics

Table 15 shows values representing maximum current numbers for the i.MX25 under worst case voltage and temperature conditions. These values are derived from the i.MX25 with core clock speed up to 400 MHz. Additionally, no power saving techniques such as clock gating were implemented when measuring these values. Common supplies are bundled according to the i.MX25 power-up sequence requirements. Peak numbers are provided for system designers so that the i.MX25 power supply requirements are satisfied during startup and transient conditions. Freescale recommends that system

Figure 9 and Figure 10 show write 1 and read sequence timing, respectively. Table 34 describes the timing parameters (OW7–OW8) that are shown in the figure.

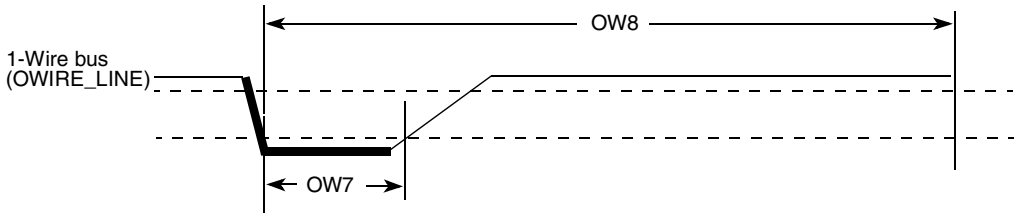

Figure 9. Write 1 Sequence Timing Diagram

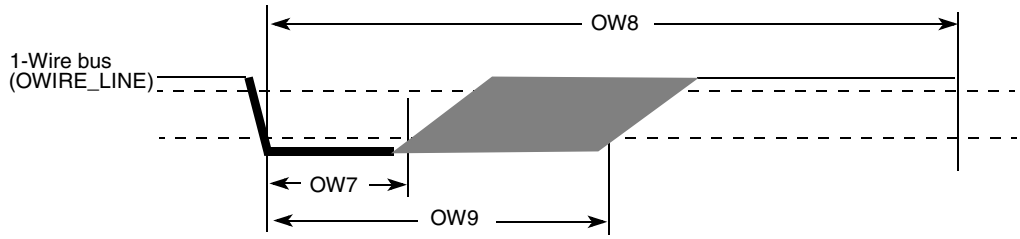

Figure 10. Read Sequence Timing Diagram

Table 34. WR1 /RD Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW7	Write 1 / read low time	t_{LOW1}	1	5	15	µs
OW8	Transmission time slot	t_{SLOT}	60	117	120	µs
OW9	Release time	$t_{RELEASE}$	15	—	45	µs

To meet timing requirements, a number of timing parameters must be controlled. See Table 38 for details on timing parameters for MDMA read and write modes.

Table 38. Timing Parameters for MDMA Read and Write Modes

ATA Parameter	MDMA Read[1] and Write[2] Timing Parameters	Relation	Adjustable Parameter(s)
tm, ti	tm	tm(min.) = ti(min.) = time_m × T – (tskew1 + tskew2 + tskew5)	time_m
td	td, td1	td1(min.) = td(min.) = time_d × T – (tskew1 + tskew2 + tskew6)	time_d
tk	tk	tk(min.) = time_k × T – (tskew1 + tskew2 + tskew6)	time_k
t0	—	t0(min.) = (time_d + time_k) × T	time_d, time_k
tg(read)	tgr	tgr(min.–read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 tgr(min.–drive) = td – te(drive)	time_d
tf(read)	tfr	tfr(min.–drive) =0 k	—
tg(write)	—	tg(min.–write) = time_d × T –(tskew1 + tskew2 + tskew5)	time_d
tf(write)	—	tf(min.–write) = time_k × T – (tskew1 + tskew2 + tskew6)	time_k
tL	—	tL(max.) = (time_d + time_k–2) × T – (tsu + tco + 2 × tbuf + 2 × tcable2)	time_d, time_k[3]
tn, tj	tkjn	tn= tj= tkjn = (max.(time_k,. time_jn) × T – (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

1 See Figure 13.

2 See Figure 14.

3 tk1 in the UDMA figures equals (tk –2 × T).

3.7.2.3 Ultra DMA (UDMA) Mode Timing

UDMA mode timing is more complicated than PIO mode or MDMA mode. In this section, timing diagrams for UDMA in- and out-transfers are provided.

3.7.2.3.1 UDMA In-Transfer Timing

Figure 15 shows the timing for UDMA in-transfer start.

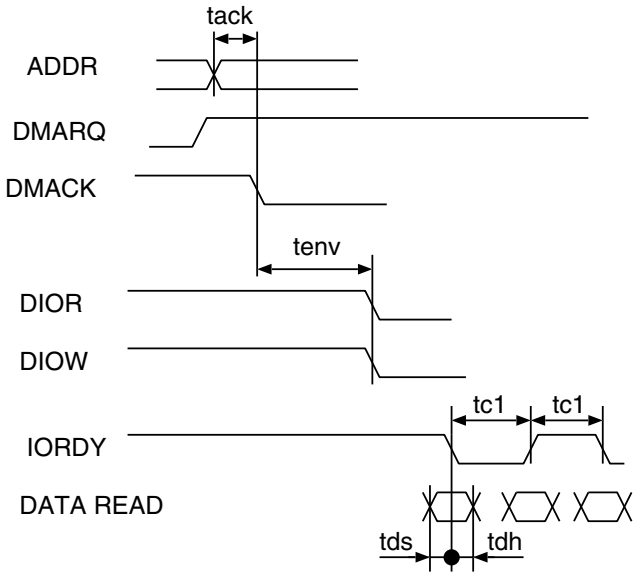

Figure 15. Timing for UDMA In-Transfer Start

Figure 16 shows the timing for host-terminated UDMA in-transfer.

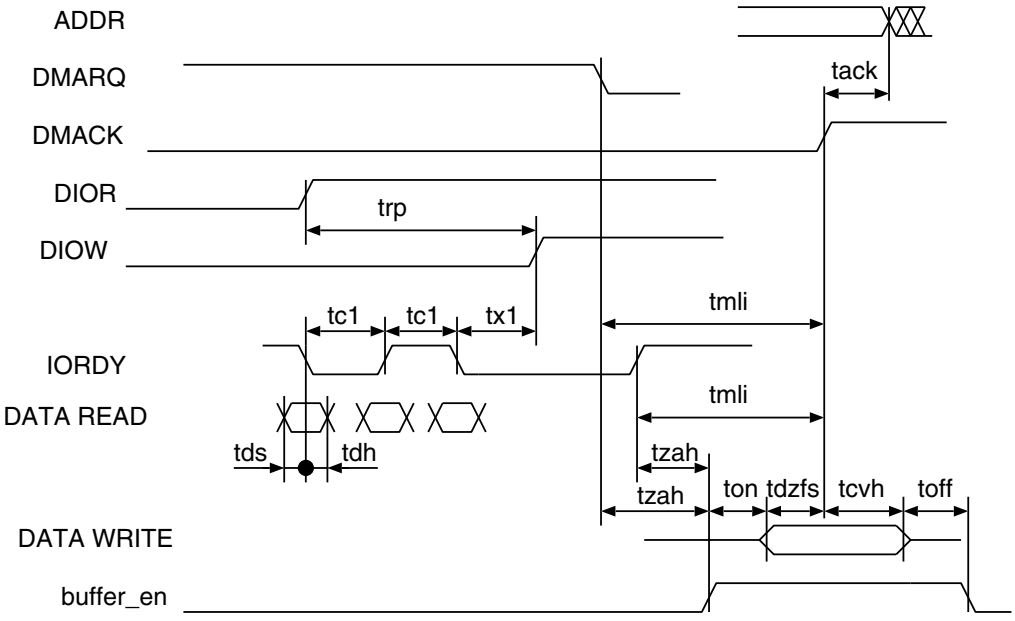

Figure 16. Timing for Host-Terminated UDMA In-Transfer

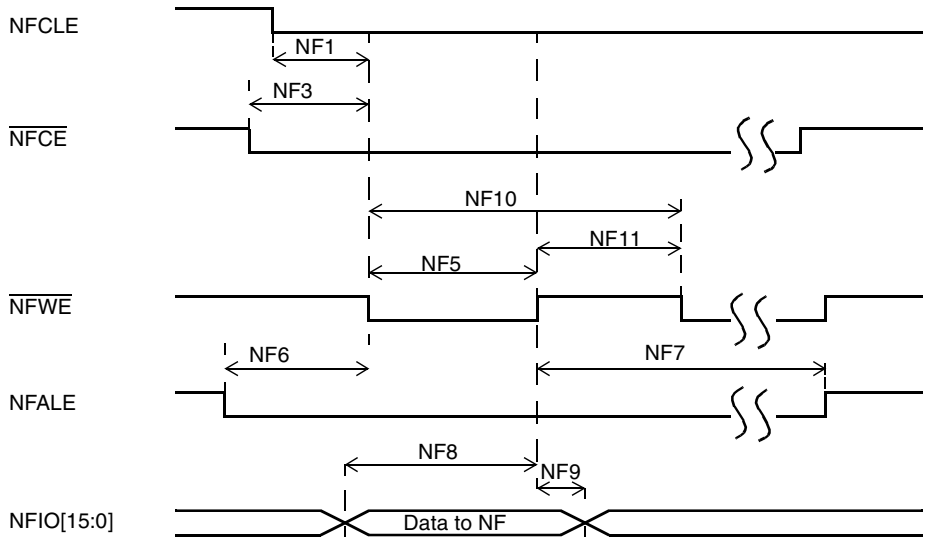

Figure 36. Write Data Latch Cycle Timing Diagram

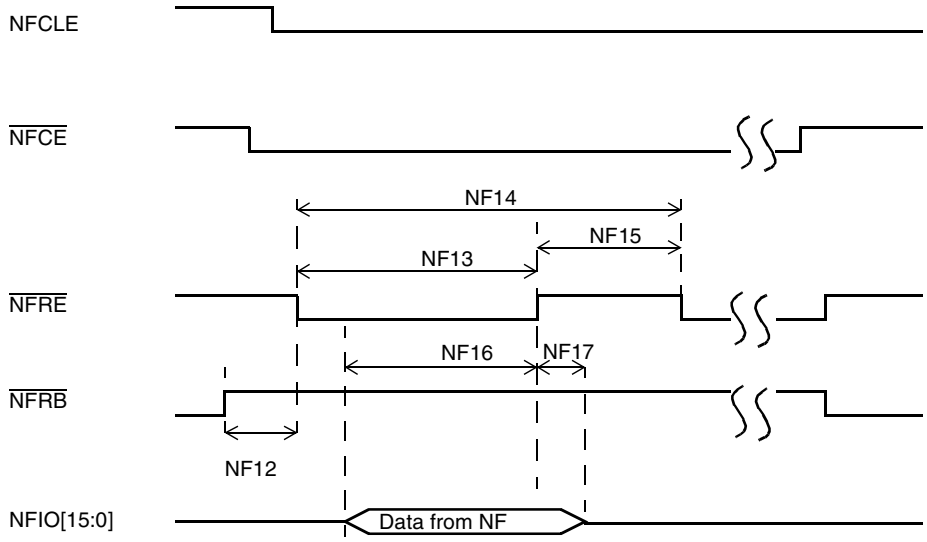

Figure 37. Read Data Latch Cycle Timing Diagram

Table 55. NFC Timing Parameters[1]

ID	Parameter	Symbol	Timing T = NFC Clock Cycle		Example Timing for NFC Clock ≈ 33 MHz T = 30 ns		Unit
			Min.	Max.	Min.	Max.	
NF1	NFCLE setup time	tCLS	T–1.0 ns	—	29	—	ns
NF2	NFCLE hold time	tCLH	T–2.0 ns	—	28	—	ns
NF3	$\overline{\text{NFCE}}$ setup time	tCS	2T–5.0 ns	—	55	—	ns
NF4	$\overline{\text{NFCE}}$ hold time	tCH	7T–5.0 ns	—	205	—	ns

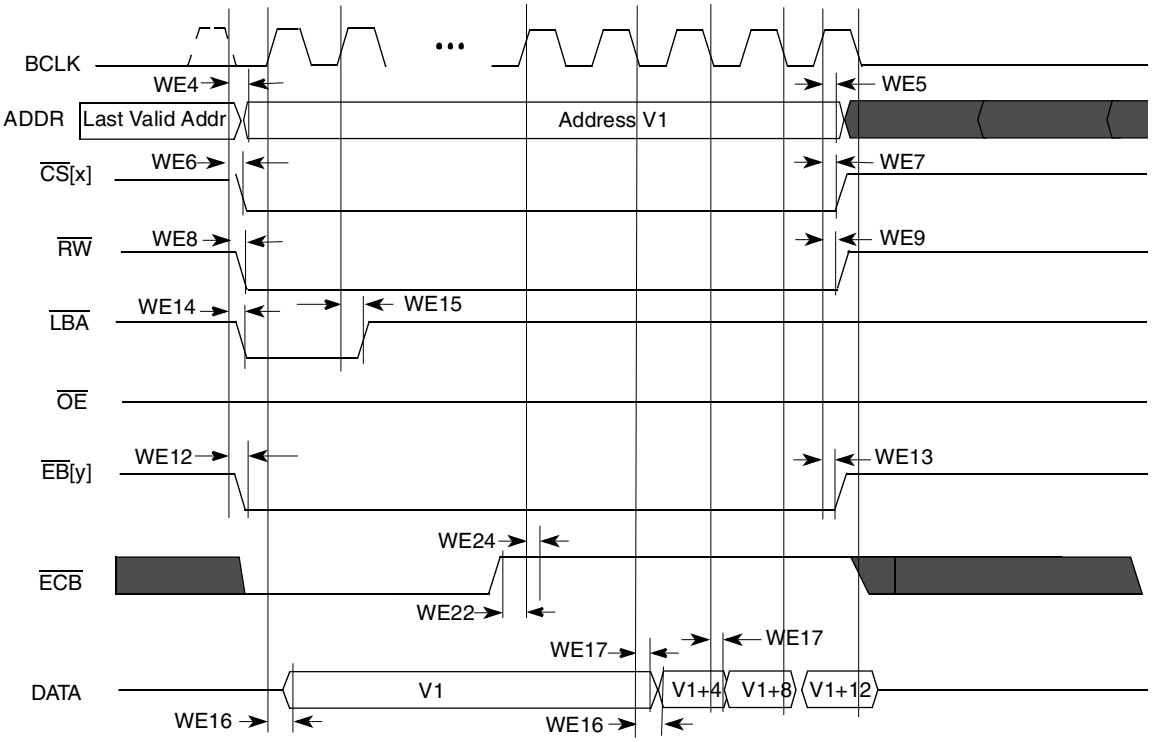

Figure 42. Synchronous Memory TIming Diagram for Burst Write Access—BCS=1, WSC=4, SYNC=1, DOL=0, PSR=1

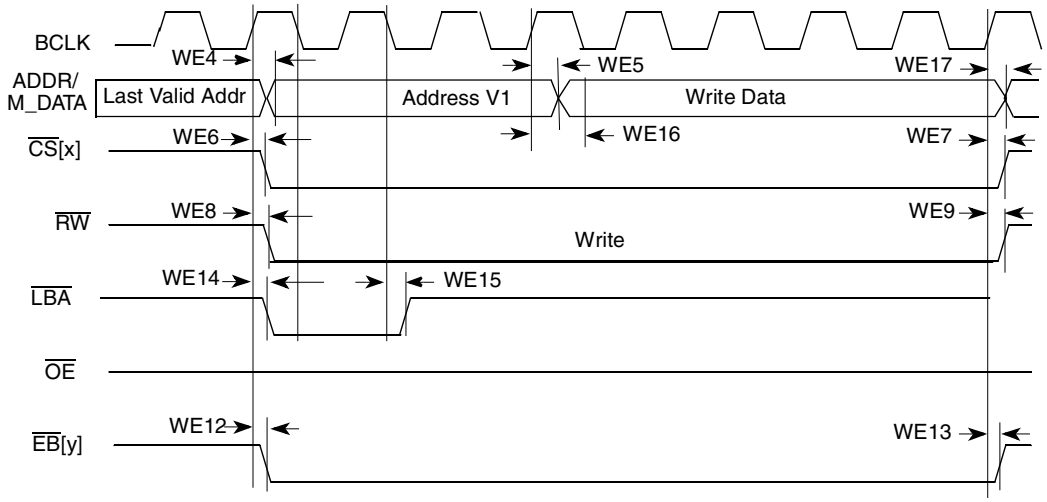

Figure 43. Muxed A/D Mode Timing Diagram for Synchronous Write Access—WSC=7, LBA=1, LBN=1, LAH=1

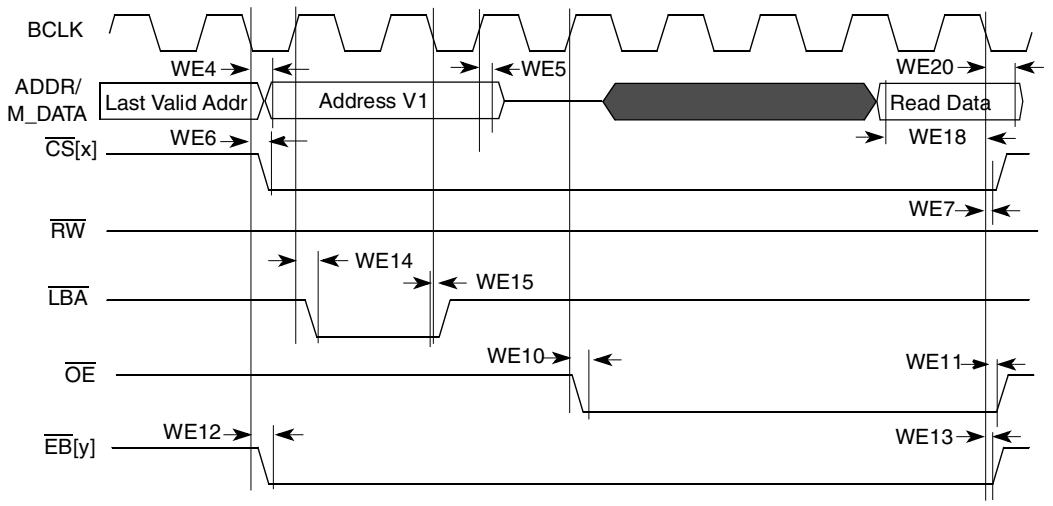

Figure 44. Muxed A/D Mode Timing Diagram for Synchronous Read Access—WSC=7, LBA=1, LBN=1, LAH=1, OEA=7

Figure 45 through Figure 49, and Table 57 help to determine timing parameters relative to chip select (CS) state for asynchronous and DTACK WEIM accesses with corresponding WEIM bit fields and the timing parameters mentioned above.

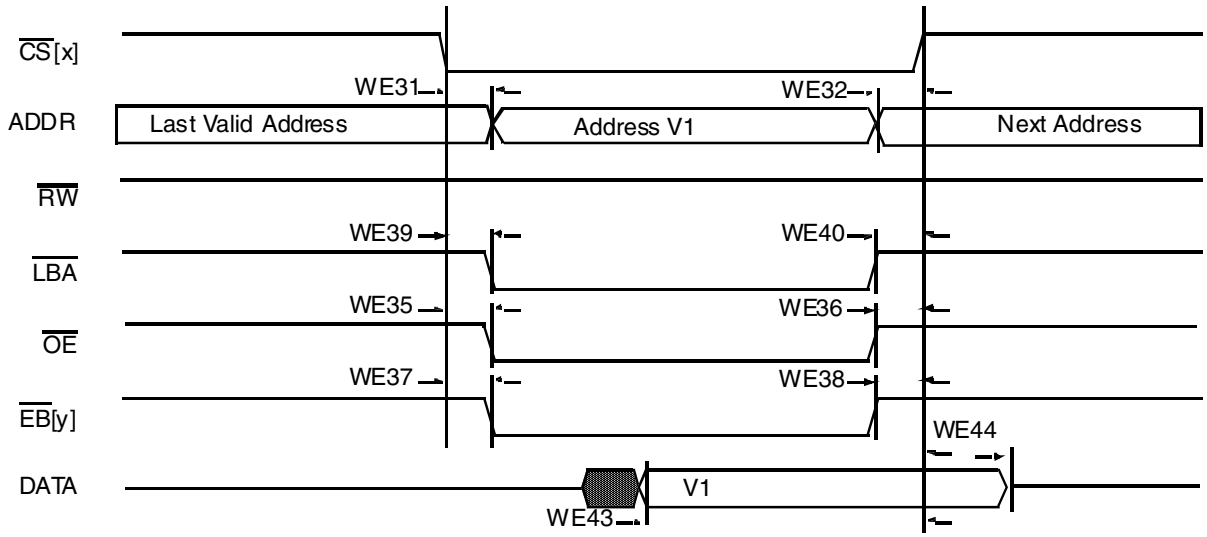

Figure 45. Asynchronous Memory Read Access

Table 57. WEIM Asynchronous Timing Parameters Relative to Chip Select Table (continued)

Ref No.	Parameter	Determination By Synchronous Measured Parameters[1]	Min	Max (If 133 MHz is supported by SoC)	Unit
WE32A(muxed A/D	$\overline{CS}$[x] valid to Address Invalid	WE4 – WE7 + (LBN + LBA + 1 – CSA[2])	–3 + (LBN + LBA + 1 – CSA)	—	ns
WE33	$\overline{CS}$[x] Valid to $\overline{RW}$ Valid	WE8 – WE6 + (RWA – CSA)	—	3 + (RWA – CSA)	ns
WE34	$\overline{RW}$ Invalid to $\overline{CS}$[x] Invalid	WE7 – WE9 + (RWN – CSN)	—	3 – (RWN_CSN)	ns
WE35	$\overline{CS}$[x] Valid to $\overline{OE}$ Valid	WE10 – WE6 + (OEA – CSA)	—	3 + (OEA – CSA)	ns
WE35A (muxed A/D)	$\overline{CS}$[x] Valid to $\overline{OE}$ Valid	WE10 – WE6 + (OEA + LBN + LBA + LAH + 1 – CSA)	–3 + (OEA + LBN + LBA + LAH + 1 – CSA)	3 + (OEA + LBN + LBA + LAH + 1 – CSA)	ns
WE36	$\overline{OE}$ Invalid to $\overline{CS}$[x] Invalid	WE7 – WE11 + (OEN – CSN)	—	3 – (OEN – CSN)	ns
WE37	$\overline{CS}$[x] Valid to $\overline{EB}$[y] Valid (Read access)	WE12 – WE6 + (EBRA – CSA)	—	3 + (EBRA[4] – CSA)	ns
WE38	$\overline{EB}$[y] Invalid to $\overline{CS}$[x] Invalid (Read access)	WE7 – WE13 + (EBRN – CSN)	—	3 – (EBRN[5] – CSN)	ns
WE39	$\overline{CS}$[x] Valid to $\overline{LBA}$ Valid	WE14 – WE6 + (LBA – CSA)	—	3 + (LBA – CSA)	ns
WE40	$\overline{LBA}$ Invalid to $\overline{CS}$[x] Invalid	WE7 – WE15 – CSN	—	3 – CSN	ns
WE40A (muxed A/D)	$\overline{CS}$[x] Valid to $\overline{LBA}$ Invalid	WE14 – WE6 + (LBN + LBA + 1 – CSA)	–3 + (LBN + LBA + 1 – CSA)	3 + (LBN + LBA + 1 – CSA)	ns
WE41	$\overline{CS}$[x] Valid to Output Data Valid	WE16 – WE6 – CSA	—	3 – CSA	ns
WE41A (muxed A/D)	$\overline{CS}$[x] Valid to Output Data Valid	WE16 – WE6 + (LBN + LBA + LAH + 1 – CSA)	—	3 + (LBN + LBA + LAH + 1 – CSA)	ns
WE42	Output Data Invalid to $\overline{CS}$[x] Invalid	WE17 – WE7 – CSN	—	3 – CSN	ns
WE43	Input Data Valid to $\overline{CS}$[x] Invalid	MAXCO – MAXCSO + MAXDI	MAXCO[6] – MAXCSO[7] + MAXDI[8]	—	ns
WE44	$\overline{CS}$[x] Invalid to Input Data invalid	0	0	—	ns
WE45	$\overline{CS}$[x] Valid to $\overline{EB}$[y] Valid (Write access)	WE12 – WE6 + (EBWA – CSA)	—	3 + (EBWA – CSA)	ns
WE46	$\overline{EB}$[y] Invalid to $\overline{CS}$[x] Invalid (Write access)	WE7 – WE13 + (EBWN – CSN)	—	–3 + (EBWN – CSN)	ns
WE47	$\overline{DTACK}$ Valid to $\overline{CS}$[x] Invalid	MAXCO – MAXCSO + MAXDTI	MAXCO[6] – MAXCSO[7] + MAXDTI[9]	—	ns
WE48	$\overline{CS}$[x] Invalid to $\overline{DTACK}$ invalid	0	0	—	ns

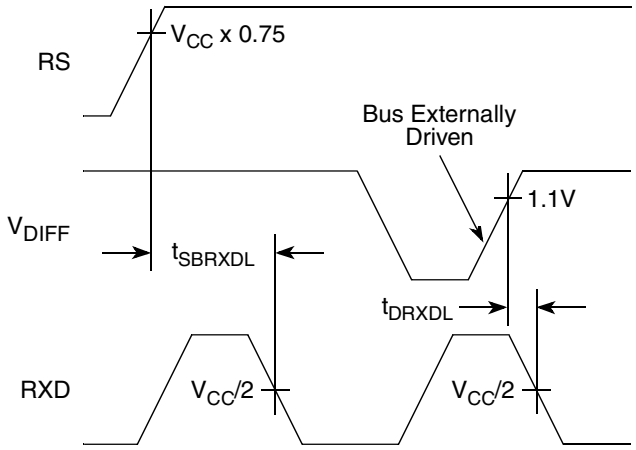

Figure 61. Timing Diagram for FlexCAN Standby Signal

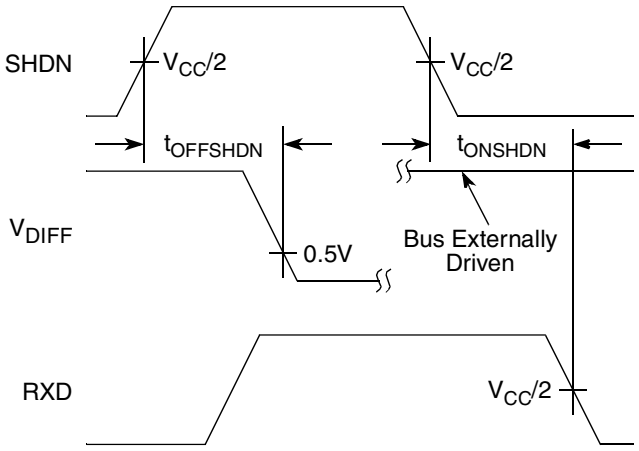

Figure 62. Timing Diagram for FlexCAN Shutdown Signal

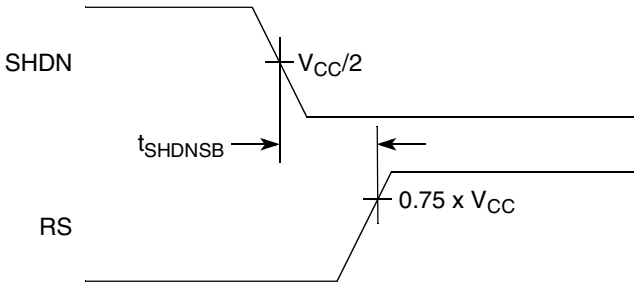

Figure 63. Timing Diagram for FlexCAN Shutdown-to-Standby Signal

Because integer multiples are not possible, taking into account the range of frequencies at which the SoC has to operate, DPLLs work in FOL mode only.

3.7.17.2 SSI Receiver Timing with Internal Clock

Figure 79 shows the timing for the SSI receiver with internal clock. Table 82 describes the timing parameters (SS1–SS51) shown in the figure.

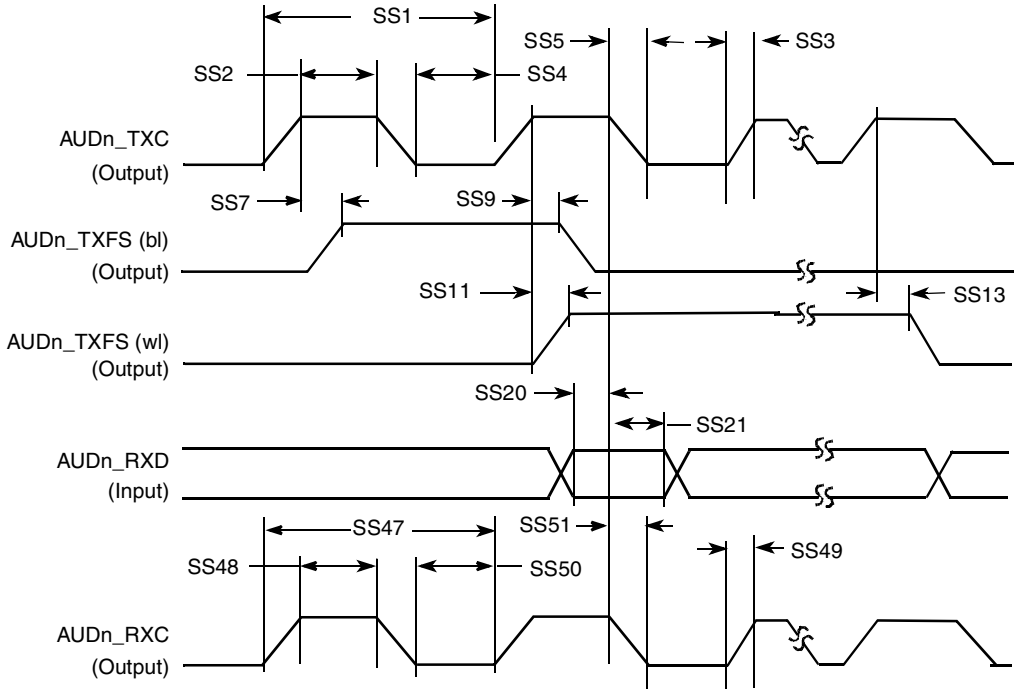

Figure 79. SSI Receiver Internal Clock Timing Diagram

Table 82. SSI Receiver Timing with Internal Clock

ID	Parameter	Min.	Max.	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	10.0	—	ns
SS21	SRXD hold time after (Rx) CK low	0.0	—	ns
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns

3.7.19.1 UART RS-232 Serial Mode Timing

3.7.19.1.1 UART Transmit Timing in RS-232 Serial Mode

Figure 85 shows the UART transmit timing in RS-232 serial mode, showing only 8 data bits and 1 stop bit. Table 86 describes the timing parameter (UA1) shown in the figure.

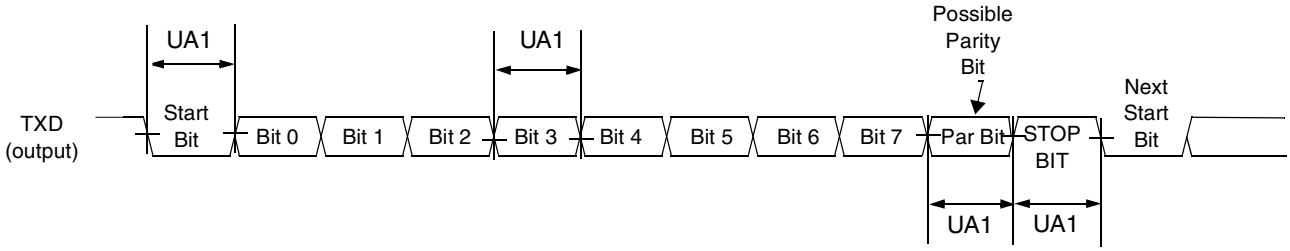

Figure 85. UART RS-232 Serial Mode Transmit Timing Diagram

Table 86. UART RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

3.7.19.1.2 UART Receive Timing in RS-232 Serial Mode

Figure 86 shows the UART receive timing in RS-232 serial mode, showing only 8 data bits and 1 stop bit. Table 87 describes the timing parameter (UA2) shown in the figure.

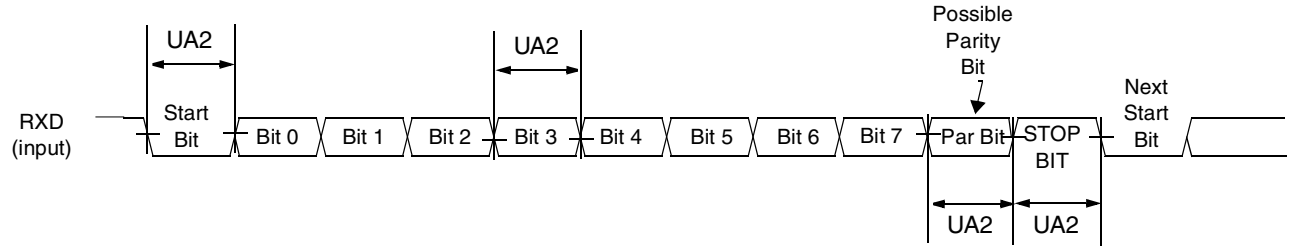

Figure 86. UART RS-232 Serial Mode Receive Timing Diagram

Table 87. UART RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA2	Receive bit time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

Table 97 shows the timing specifications for USB in VP_VM unidirectional mode.

Table 97. USB Timing Specifications in VP_VM Unidirectional Mode

No.	Parameter	Signal	Direction	Min.	Max.	Unit	Conditions/ Reference Signal
US30	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US31	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US32	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US33	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US34	Tx high overlap	USB_SE0_VM	Out	0.0	—	ns	USB_DAT_VP
US35	Tx low overlap	USB_SE0_VM	Out	—	0.0	ns	USB_DAT_VP
US36	Enable delay	USB_DAT_VP USB_SE0_VM	In	—	8.0	ns	USB_TXOE_B
US37	Disable delay	USB_DAT_VP USB_SE0_VM	In	—	10.0	ns	USB_TXOE_B
US38	Rx rise/fall time	USB_VP1	In	—	3.0	ns	35 pF
US39	Rx rise/fall time	USB_VM1	In	—	3.0	ns	35 pF
US40	Rx skew	USB_VP1	Out	–4.0	+4.0	ns	USB_SE0_VM
US41	Rx skew	USB_RCV	Out	–6.0	+2.0	ns	USB_DAT_VP

3.7.20.2 USB Parallel Interface Timing

Table 98 defines the USB parallel interface signals.

Table 98. Signal Definitions for USB Parallel Interface

Name	Direction	Signal Description
USB_Clk	In	Interface clock—All interface signals are synchronous to USB_Clk
USB_Data[7:0]	I/O	Bidirectional data bus, driven low by the link during idle—Bus ownership is determined by the direction
USB_Dir	In	Direction—Control the direction of the data bus
USB_Stp	Out	Stop—The link asserts this signal for one clock cycle to stop the data stream currently on the bus
USB_Nxt	In	Next—The PHY asserts this signal to throttle the data

Figure 97 shows the USB parallel mode transmit/receive waveform. Table 99 describes the timing parameters (USB15–USB17) shown in the figure.

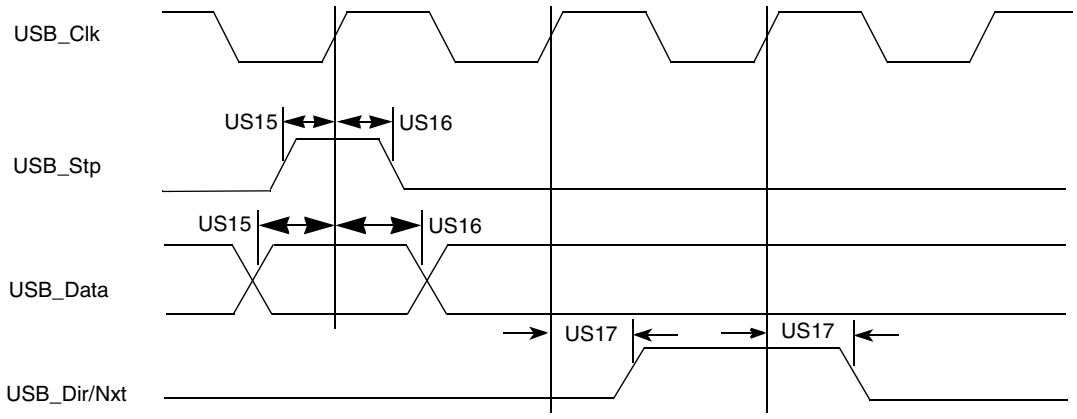

Figure 97. USB Parallel Mode Transmit/Receive Waveform

Table 99. USB Timing Specification in Parallel Mode

ID	Parameter	Min.	Max.	Unit	Conditions/Reference Signal
US15	Setup time (Dir&Nxt in, Data in)	6.0	—	ns	10 pF
US16	Hold time (Dir&Nxt in, Data in)	0.0	—	ns	10 pF
US17	Output delay time (Stp out, Data out	—	9.0	ns	10 pF

4 Package Information and Contact Assignment

4.1 400 MAPBGA—Case 17x17 mm, 0.8 mm Pitch

Figure 98 shows the 17×17 mm i.MX25 production package. The following notes apply to Figure 98:

- All dimensions in millimeters.
- Dimensioning and tolerancing per ASME Y14.5M-1994.
- Maximum solder bump diameter measured parallel to datum A.
- Datum A, the seating plane, is determined by the spherical crowns of the solder bumps.
- Parallelism measurement shall exclude any effect of mark on top surface of package.

Table 101. 17×17 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
LD2[2]	W7	LCDC	GPIO	OUTPUT	Low
LD3[2]	U8	LCDC	GPIO	OUTPUT	Low
LD4[2]	Y6	LCDC	GPIO	OUTPUT	Low
LD5[2]	V7	LCDC	GPIO	OUTPUT	Low
LD6[2]	W6	LCDC	GPIO	OUTPUT	Low
LD7[2]	Y5	LCDC	GPIO	OUTPUT	Low
LD8[2]	V6	LCDC	GPIO	OUTPUT	Low
LD9[2]	W5	LCDC	GPIO	OUTPUT	Low
LD10[2]	Y4	LCDC	GPIO	OUTPUT	Low
LD11[2]	Y3	LCDC	GPIO	OUTPUT	Low
LD12[2]	V5	LCDC	GPIO	OUTPUT	Low
LD13[2]	W4	LCDC	GPIO	OUTPUT	Low
LD14[2]	V4	LCDC	GPIO	OUTPUT	Low
LD15[2]	W3	LCDC	GPIO	OUTPUT	Low
HSYNC[2]	U7	LCDC	GPIO	OUTPUT	Low
VSYNC[2]	U6	LCDC	GPIO	OUTPUT	Low
LSCLK[2]	U5	LCDC	GPIO	OUTPUT	Low
OE_ACD[2]	V3	LCDC	GPIO	OUTPUT	Low
CONTRAST	U4	LCDC	GPIO	OUTPUT	Low
PWM[2]	W2	LCDC	GPIO	INPUT	100 KΩ Pull-Down
CSI_D2	F18	CSI	GPIO	INPUT	Keeper
CSI_D3	E19	CSI	GPIO	INPUT	Keeper
CSI_D4	F19	CSI	GPIO	INPUT	Keeper
CSI_D5	G18	CSI	GPIO	INPUT	Keeper
CSI_D6	E20	CSI	GPIO	INPUT	Keeper
CSI_D7	E18	CSI	GPIO	INPUT	Keeper
CSI_D8	G19	CSI	GPIO	INPUT	Keeper
CSI_D9	F20	CSI	GPIO	INPUT	Keeper
CSI_MCLK[2]	H18	CSI	GPIO	OUTPUT	Low
CSI_VSYNC[2]	G20	CSI	GPIO	INPUT	Keeper
CSI_HSYNC[2]	H19	CSI	GPIO	INPUT	Keeper
CSI_PIXCLK[2]	H20	CSI	GPIO	INPUT	Keeper

Table 102 lists the 17×17 mm package i.MX25 no connect contact assignments.

Table 102. 17×17 mm Package i.MX25 No Connect Contact Assignments

Signal Name	Contact Assignment
NC_BGA_B20	B20
NC_BGA_E17	E17
NC_BGA_H17	H17
NC_BGA_J19	J19
NC_BGA_M18	M18
NC_BGA_P20	P20
NC_BGA_U15	U15
NC_BGA_U16	U16
NC_BGA_V15	V15
NC_BGA_V16	V16
NC_BGA_V17	V17
NC_BGA_W14	W14
NC_BGA_Y2	Y2
NC_BGA_Y14	Y14
NC_BGA_Y17	Y17

4.5 347 MAPBGA—Case 12 x 12 mm, 0.5 mm Pitch

Figure 99 shows the 12×12 mm i.MX25 production package. The following notes apply to Figure 99:

- All dimensions in millimeters.Dimensioning and tolerancing per ASME Y14.5M-1994.
- Maximum solder ball diameter measured parallel to datum A.
- Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
- Parallelism measurement shall exclude any effect of mark on package's top surface.

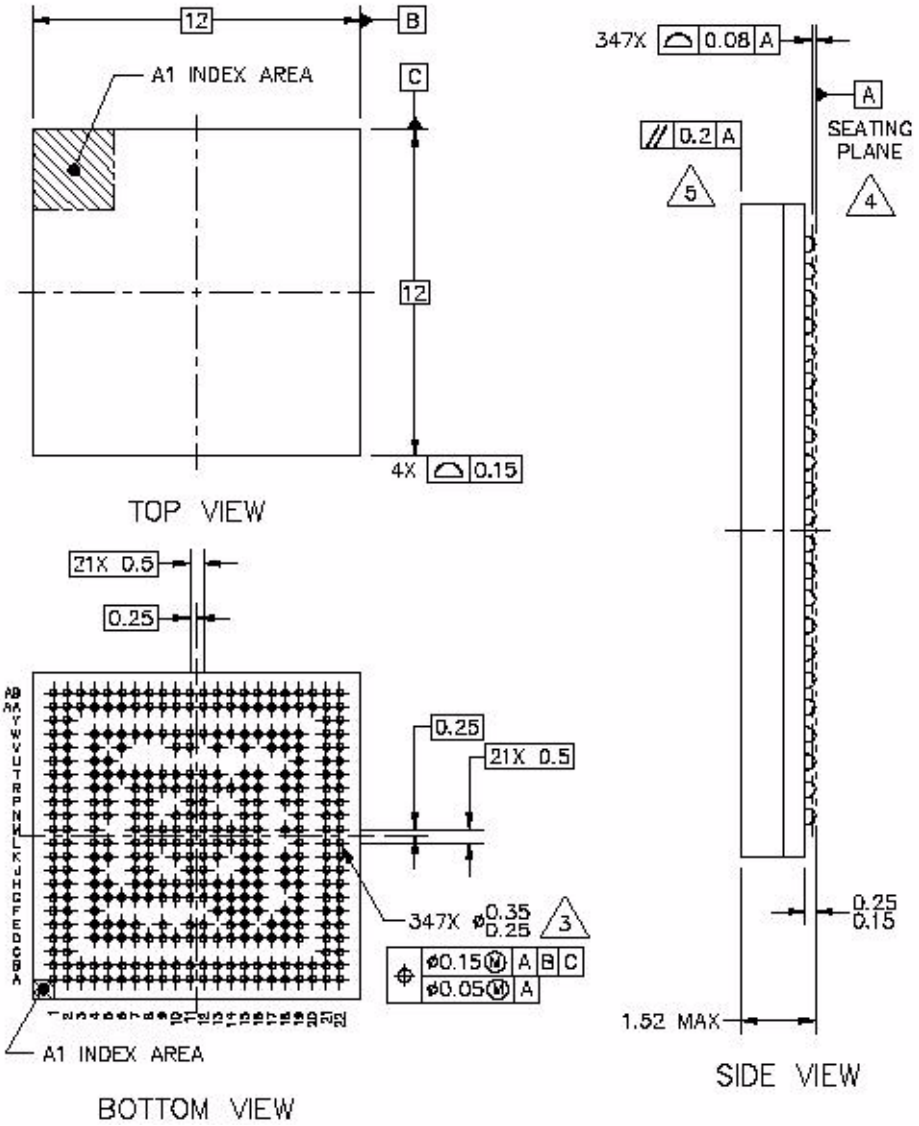

Figure 99. 12×12 mm i.MX25 Production Package

Table 105. 12x12 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
WIPER	AA17	ADC	ANALOG	ANALOG	-
INAUX0	AA15	ADC	ANALOG	ANALOG	-
INAUX1	W14	ADC	ANALOG	ANALOG	-
INAUX2	AB16	ADC	ANALOG	ANALOG	-

1 The state immediately after reset and before ROM firmware or software has executed.

2 During power-on reset this port acts as input for fuse override signal.

3 During power-on reset this port acts as output for diagnostic signal.

Table 106 lists the 12×12 mm package i.MX25 no connect contact assignments.

Table 106. 12×12 mm Package i.MX25 No Connect Contact Assignments

Signal Name	Contact Assignment
NC_BGA_E4	E4
NC_BGA_L4	L4

4.8 i.MX25 12x12 Package Ball Map

Table 107 shows the i.MX25 12×12 package ball map.

Table 107. i.MX25 12×12 Package Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	QGND	EB0	OE	A14	A16	A18	A22	BCLK	DQM1	SD9	SD10	SD7	SD0	SD3	SD5	SDCKE0	SDBA0	CS3	A1	A0	A4	QGND
B	ECB	QGND	LBA	EB1	A10	A20	A24	SD14	SD12	SD11	SD6	SD2	SD4	QGND	SDWE	CAS	CS2	A2	A5	A7	QGND	A12
C	NFRE_B	CS0																			A11	CS1_D2
D	NFCLE	CS5		CS1	RW	A15	A21	A25	SD15	SD8	DQM0	SD1	SDCLK	SDCLK_B	RAS	SDBA1	A3	A6	A9		A13	CSI_D6
E	NFWE_B	NFALE		NC_BGA_E4	CS4	A17	A19		A23		SD13	SDQS1		SDQS0	NVCC_EMI2		MA10	QGND	A8		CSI_D4	CSI_D8
F	D1	D0		NF_CE0									QGND	QGND	NVCC_EMI2	SDCKE1		QGND	CSI_D3		CSI_D7	CSI_MCLK