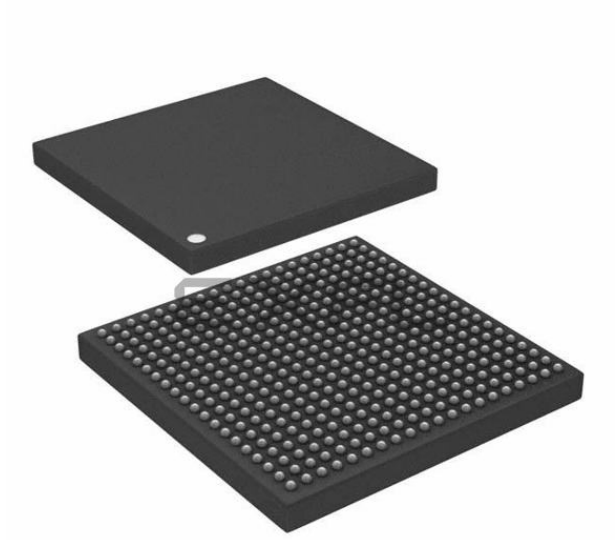

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Boot Security, Cryptography, Secure Fusebox, Secure JTAG, Secure Memory, Tamper Detection
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx258cjm4a

current measurements are taken with customer-specific use-cases to reflect the normal operating conditions in the end system.

Table 15. Power Consumption

Power Supply	Voltage (V)	Max Current (mA)
QVDD	1.52	360
NVCC_EMI1, NVCC_EMI2	1.9	30
NVCC_CRM, NVCC_SDIO, NVCC_CSI, NVCC_NFC, NVCC_JTAG, NVCC_LCDC, NVCC_MISC	3.6	110
MPLL_VDD, UPLL_VDD	1.65	20
USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD, USBPHY1_VDDA, USBPHY2_VDD, OSC24M_VDD, NVCC_ADC	3.3	40
FUSE_VDD[1]	3.6	62
BATT_VDD	1.55	0.030

[1] The FUSE_VDD rail is connected to ground. it only needs a voltage if the system fuse burning is needed.

The method for obtaining the maximum current is as follows:

1. Measure the worst case power consumption on individual rails using directed test on i.MX25.
2. Correlate the worst case power consumption power measurements with the worst case power consumption simulations.
3. Combine common voltage rails based on the power supply sequencing requirements (add the worst case power consumption on each rail within some test cases from several test cases run, to maximize different rails in the power group).
4. Guard the worst case numbers for temperature and process variation.
5. The sum of individual rails is greater than the real world power consumption, since a real system does not typically maximize the power consumption on all peripherals simultaneously.
6. BATT_VDD current is measured when the system is in reduced power mode maintaining the RTC. When the system is in run mode, QVDD is used to supply the DryIce, so this current becomes negligible. See Table 12, for more details on the power modes.

NOTE

The values mentioned above should not be taken as a typical max run data for specific use cases. These values are Absolute MAX data. Freescale recommends that the system current measurements are taken with customer-specific use-cases to reflect normal operating conditions in the end system.

Table 19. DDR2 (SSTL_18) I/O DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Termination voltage[5]	Vtt	—	OVDD/2 – 0.04	OVDD/2	OVDD/2 + 0.04	
Input current[6](no pull-up/down)	IIN	VI = 0 VI = OVDD	—	—	110 60	nA
High-impedance I/O supply current[6]	Icc-ovdd	VI = OVDD or 0	—	—	980	nA
High-impedance core supply current[6]	Icc-vddi	VI = VDD or 0	—	—	1210	nA

1 OVDD = 1.7 V; V_{out} = 1.42 V. (V_{out}-OVDD)/IOH must be less than 21 W for values of V_{out} between OVDD and OVDD-0.28 V.

2 OVDD = 1.7 V; V_{out} = 280 mV. V_{out}/IOL must be less than 21 W for values of V_{out} between 0 V and 280 mV. Simulation circuit for parameters V_{oh} and V_{ol} for I/O cells is below.

3 Vin(dc) specifies the allowable DC excursion of each differential input.

4 Vid(dc) specifies the input differential voltage required for switching. The minimum value is equal to Vih(dc) - Vil(dc).

5 Vtt is expected to track OVDD/2.

6 Minimum condition: BCS model, 1.95 V, and –40 °C. Typical condition: typical model, 1.8 V, and 25 °C. Maximum condition: wcs model, 1.65 V, and 105 °C.

3.5.2 GPIO I/O DC Parameters

Table 20 shows the I/O parameters for GPIO.

Table 20. GPIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
High-level output voltage[1]	Voh	Ioh=–1mA Ioh = Specified Drive	OVDD – 0.15 0.8 × OVDD	—	—	V
Low-level output voltage[1]	Vol	Iol=1mA Iol=Specified Drive	—	—	0.15 0.2 × OVDD	V
High-level output current for slow mode	I Ioh	Voh=0.8 × OVDD Standard Drive High Drive Max. Drive	 –2.0 –4.0 –8.0	—	—	mA
High-level output current for fast mode	I Ioh	Voh=0.8 × OVDD Standard Drive High Drive Max. Drive	 –4.0 –6.0 –8.0	—	—	mA
Low-level output current for slow mode	I Iol	Voh=0.2 × OVDD Standard Drive High Drive Max. Drive	 2.0 4.0 8.0	—	—	mA
Low-level output current for fast mode	I Iol	Voh=0.2 × OVDD Standard Drive High Drive Max. Drive	 4.0 6.0 8.0	—	—	mA
High-level DC input voltage	VIH	—	0.7 × OVDD	—	OVDD	V
Low-level DC input voltage	VIL	—	–0.3 V	—	0.3 × OVDD	V

3.6.1 Slow I/O AC Parameters

Table 21 shows the slow I/O AC parameters.

Table 21. Slow I/O AC Parameters

Parameter	Symbol	Test Voltage	Test Capacitance	Min. Rise/Fall	Typ. Rise/Fall	Max. Rise/Fall	Units
Duty cycle	Fduty	—	—	40	—	60	%
Output pad transition times[1] (max. drive)	tpr	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	0.95/0.84 1.58/1.37 2.70/2.50 3.40/3.20	1.36/1.11 2.19/1.77 1.80/1.40 2.80/2.14	2.06/1.60 3.20/2.47 3.01/2.37 4.63/3.38	ns
Output pad transition times[1] (high drive)	tpr	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	1.60/1.39 2.94/2.51 1.85/1.48 2.93/2.37	2.23/1.79 4.05/3.17 2.90/2.17 4.56/3.40	3.26/2.50 5.72/4.27 4.75/3.43 7.33/5.26	
Output pad transition times[1] (standard drive)	tpr	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	3.07/2.62 5.82/4.95 3.04/2.47 5.37/4.40	4.22/3.30 7.94/6.19 4.73/3.50 7.70/8.10	6.03/4.48 11.28/8.28 3.01/2.36 4.63/3.38	
Output pad propagation delay[1] (max. drive), 50%–50%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	1.92/2.1 2.44/2.53 2.05/2.27 2.71/2.84	2.96/2.96 3.7/3.64 3.32/3.67 4.39/4.51	4.47/4.38 5.54/5.31 5.27/5.85 7.00/7.15	ns
Output pad propagation delay[1] (high drive), 50%–50%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	2.35/2.49 3.31/3.43 2.58/2.69 3.62/3.60	3.58/3.61 4.9/4.786 4.17/4.27 5.86/5.61	5.35/5.24 7.19/6.8 6.64/6.74 9.34/8.76	
Output pad propagation delay[1] (standard drive), 50%–50%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	3.39/3.51 5.28/5.35 3.71/3.68 5.52/5.32	5.03/4.89 7.6/7.14 6.03/5.75 8.80/7.96	7.39/6.95 10.97/9.45 9.64/8.97 13.9/11.3	
Output pad propagation delay[1] (max. drive), 40%–60%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	1.942/2.04 2.378/2.48 2.03/2.28 2.59/2.73	2.923/2.95 3.541/3.53 3.19/3.59 4.10/4.33	4.33/4.3 5.29/5.09 4.97/5.64 6.43/6.77	ns
Output pad propagation delay[1] (high drive), 40%–60%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	2.29/2.44 3.05/3.20 2.45/2.62 3.36/3.39	3.42/3.49 4.46/4.45 3.86/4.07 5.34/5.22	5.05/5.02 6.53/6.3 6.02/6.35 8.40/8.08	
Output pad propagation delay[1] (standard drive), 40%–60%	tpo	3.0–3.6 V 3.0–3.6 V 1.65–1.95 V 1.65–1.95 V	25 pF 50 pF 25 pF 50 pF	3.12/3.26 4.60/4.73 3.43/3.46 4.89/4.79	4.58/4.53 6.61/6.32 5.48/5.34 7.75/7.16	6.69/6.42 9.5/8.32 8.65/8.26 12.2/9.97	

Table 23. Fast I/O AC Parameters for OVDD = 3.0–3.6 V (continued)

Output Pad Propagation Delay[1] (High Drive), 50%–50%	tpo	25 pF 50 pF	1.35/1.42 1.98/2.04	1.95/1.91 2.81/2.68	2.96/2.76 4.16/3.78	ns
Output Pad Propagation Delay[1] (Standard Drive), 50%–50%	tpo	25 pF 50 pF	1.77/1.85 2.70/2.78	2.54/2.48 3.82/3.62	3.80/3.60 5.62/5.10	ns
Output Pad Propagation Delay[1] (Max Drive), 40%–60%	tpo	25 pF 50 pF	1.37/1.50 1.74/1.88	1.94/2.05 2.46/2.55	2.95/3.07 3.71/3.75	ns
Output Pad Propagation Delay[1] (High Drive), 40%–60%	tpo	25 pF 50 pF	1.48/1.61 1.98/2.10	2.11/2.19 2.78/2.81	3.19/3.26 4.14/4.09	ns
Output Pad Propagation Delay[1] (Standard Drive), 40%–60%	tpo	25 pF 50 pF	1.84/1.97 2.58/2.71	2.61/2.67 3.62/3.58	3.95/3.95 5.36/5.15	ns
Output Enable to Output Valid Delay[1] (Max Drive), 50%–50%	tpv	25 pF 50 pF	1.34/1.32 1.81/1.79	1.91/1.81 2.56/2.40	2.92/2.67 3.83/3.47	ns
Output Enable to Output Valid Delay[1] (High Drive), 50%–50%	tpv	25 pF 50 pF	1.48/1.47 2.12/2.1	2.12/2.00 2.98/2.76	3.21/2.92 4.41/3.94	ns
Output Enable to Output Valid Delay[1] (Standard Drive), 50%–50%	tpv	25 pF 50 pF	1.90/1.90 2.85/2.83	2.70/2.60 4.00/3.70	4.07/3.74 5.86/5.24	ns
Output Enable to Output Valid Delay[1] (Max Drive), 40%–60%	tpv	25 pF 50 pF	1.55/1.42 1.93/1.81	2.25/2.08 2.77/2.58	3.50/3.31 4.24/3.99	ns
Output Enable to Output Valid Delay[1] (High Drive), 40%–60%	tpv	25 pF 50 pF	1.67/1.54 2.16/2.03	2.41/2.23 3.08/2.86	3.74/3.51 4.66/4.34	ns
Output Enable to Output Valid Delay[1] (Standard Drive), 40%–60%	tpv	25 pF 50 pF	2.02/1.90 2.76/2.63	2.91/2.71 3.91/3.62	4.48/4.21 5.85/5.39	ns
Output Pad Slew Rate[2] (Max Drive)	tps	25 pF 50 pF	0.96/1.40 0.54/0.83	1.54/2.10 0.85/1.24	2.30/3.00 1.26/1.70	V/ns
Output Pad Slew Rate[2] (High Drive)	tps	25 pF 50 pF	0.76/1.10 0.41/0.64	1.19/1.71 0.63/0.95	1.78/2.39 0.95/1.30	V/ns
Output Pad Slew Rate[2] (Standard Drive)	tps	25 pF 50 pF	0.52/0.78 0.28/0.44	0.80/1.19 0.43/0.64	1.20/1.60 0.63/0.87	V/ns
Output Pad di/dt[3] (Max Drive)	didt	25 pF 50 pF	46 49	108 113	250 262	mA/ns
Output Pad di/dt[3] (High Drive)	didt	25 pF 50 pF	35 37	82 86	197 207	mA/ns
Output Pad di/dt[3] (Standard Drive)	didt	25 pF 50 pF	22 23	52 55	116 121	mA/ns
Input Pad Propagation Delay without Hysteresis, 50%–50%[4]	tpi	1.6pF	0.729/0.458	0.97/0.0649	1.404/0.97	ns
Input Pad Propagation Delay with Hysteresis, 50%–50%[4]	tpi	1.6pF	1.203/0.938	1.172/1.187	1.713/1.535	ns
Input Pad Propagation Delay without Hysteresis, 40%–60%[4]	tpi	1.6pF	0.879/0.977	1.434/1.12	1.854/1.427	ns

Table 25. AC Parameters for Mobile DDR pbijtov18_33_ddr_clk I/O (continued)

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Output pad slew rate[2] (high drive)	tps	25 pF 50 pF	0.30/0.37 0.21/0.25	0.51/0.63 0.36/0.42	091/1.06 0.63/0.67	V/ns
Output pad slew rate[2] (standard drive)	tps	25 pF 50 pF	0.22/0.26 0.13/0.16	0.37/0.44 0.23/0.26	0.65/0.72 0.39/0.40	V/ns
Output pad dI/dt[3] (max. drive)	tdit	25 pF 50 pF	65 70	171 183	426 450	mA/ns
Output pad dI/dt[3] (high drive)	tdit	25 pF 50 pF	31 33	82 87	233 245	mA/ns
Output pad dI/dt[3] (standard drive)	tdit	25 pF 50 pF	16 17	43 46	115 120	mA/ns
Input pad transition times[4]	trfi	1.0 pF	0.07/0.08	0.11/0.13	0.16/0.20	ns
Input pad propagation delay, 50%–50%[4]	tpi	1.0 pF	0.84/0.84	1.40/1.34	2.25/2.16	ns
Input pad propagation delay, 40%–60%[4]	tpi	1.0 pF	1.66/1.66	2.22/2.16	3.06/2.97	ns

1 Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from core is 1 ns (20%–80%).

2 Minimum condition for tps: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

3 Maximum condition for tdit: bcs model, 1.3 V, I/O 1.95 V, and –40 °C.

4 Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.65 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

Table 26 shows the AC requirements for mobile DDR I/O.

Table 26. AC Requirements for Mobile DDR I/O

Parameter	Symbol	Min.	Max.	Units
AC input logic high	VIH(ac)	0.8 × OVDD	OVDD+0.3	V
AC input logic low	VIL(ac)	–0.3	0.2 × OVDD	V
AC differential input voltage	Vid(ac)	0.6 × OVDD	OVDD+0.6	V
AC differential cross point voltage for input	Vix(ac)	0.4 × OVDD	OVDD+0.6	V

Table 27. AC Parameters for SDRAM I/O (continued)

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Output pad slew rate[2] (standard drive)	tps	25 pF 50 pF	0.38/0.41 0.20/0.22	0.59/0.60 0.31/0.32	0.89/0.82 0.47/0.43	V/ns
Output pad dI/dt[3] (max. drive)	tdit	25 pF 50 pF	89 94	198 209	398 421	mA/ns
Output pad dI/dt[3] (high drive)	tdit	25 pF 50 pF	59 62	132 139	265 279	mA/ns
Output pad dI/dt[3] (standard drive)	tdit	25 pF 50 pF	29 31	65 69	132 139	mA/ns
Input pad transition times[4]	trfi	1.0 pF	0.07/0.08	0.11/0.12	0.16/0.20	ns
Input pad propagation delay, 50%–50%[4]	tpi	1.0 pF	0.35/1.17	0.63/1.53	1.16/2.04	ns
Input pad propagation delay, 40%–60%[4]	tpi	—	1.18/1.99	1.45/2.35	1.97/2.85	—

1 Maximum condition for tpr, tpo, tpi, and tpv: wcs model, 1.1 V, I/O 3.0 V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 3.6 V and –40 °C. Input transition time from core is 1 ns (20%–80%).

2 Minimum condition for tps: wcs model, 1.1 V, I/O 3.0 V, and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

3 Maximum condition for tdit: bcs model, 1.3 V, I/O 3.6 V, and –40 °C.

4 Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 3.0 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 3.6 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

Table 28 shows AC parameters for SDRAM pbijtov18_33_ddr_clk I/O.

Table 28. AC Parameters for SDRAM pbijtov18_33_ddr_clk I/O

Parameter	Symbol	Load Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty cycle	Fduty	—	40	50	60	%
Clock frequency[1]	f	—	—	—	133	MHz
Output pad transition times[1] (max. drive)	tpr	25 pF 50 pF	0.82/0.87 1.56/1.67	1.14/1.13 2.13/2.09	1.62/1.50 3.015/2.77	ns
Output pad transition times[1] (high drive)	tpr	25 pF 50 pF	1.23/1.31 2.31/2.47	1.71/1.68 3.22/3.12	2.39/2.22 4.53/4.16	ns
Output pad transition times[1] (standard drive)	tpr	25 pF 50 pF	2.44/2.60 4.65/4.99	3.38/3.27 6.38/6.23	4.73/4.38 9.05/8.23	ns
Output pad propagation delay[1] (max. drive), 50%–50% input signals and crossing of output signals	tpo	15 pF 35 pF	1.50/1.40 1.95/1.85	2.23/2.07 2.81/2.66	3.28/3.04 4.06/3.82	ns
Output pad propagation delay[1] (high drive), 50%–50% input signals and crossing of output signals	tpo	15 pF 35 pF	1.69/1.59 2.35/2.25	2.48/2.32 3.35/3.19	3.63/3.38 4.80/4.56	ns
Output pad propagation delay[1] (standard drive), 50%–50% input signals and crossing of output signals	tpo	15 pF 35 pF	2.26/2.15 3.59/3.49	3.24/3.08 4.98/4.82	4.66/4.42 7.00/6.75	ns
Output pad propagation delay[1] (max. drive), 40%–60% input signals and crossing of output signals	tpo	15 pF 35 pF	1.67/1.57 2.11/2.02	2.39/2.24 2.97/2.82	3.45/3.21 4.23/3.99	ns

3.7.2.2 Multiword DMA (MDMA) Mode Timing

Figure 13 and Figure 14 show the timing for MDMA read and write modes, respectively.

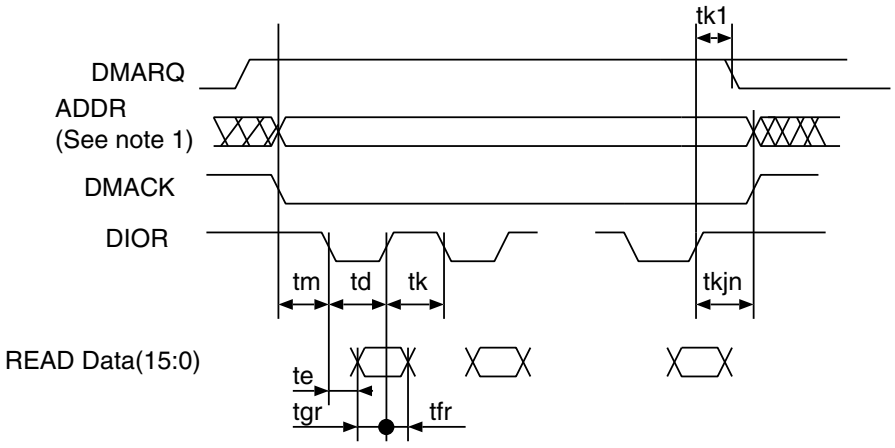

Figure 13. MDMA Read Mode Timing

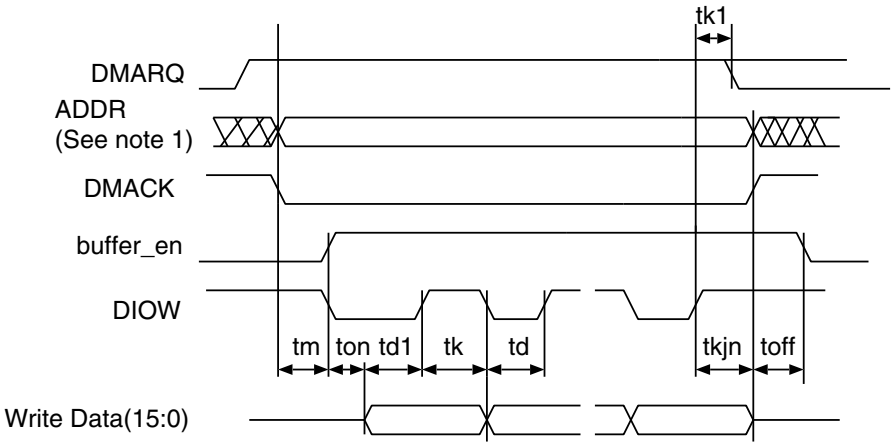

Figure 14. MDMA Write Mode Timing

Table 46. SDRAM Refresh Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD1	SDRAM clock high-level width	tCH	3.4	4.1	ns
SD2	SDRAM clock low-level width	tCL	3.4	4.1	ns
SD3	SDRAM clock cycle time	tCK	7.5	—	ns
SD6	Address setup time	tAS	1.8	—	ns
SD7	Address hold time	tAH	1.8	—	ns
SD10	Precharge cycle period[1]	tRP	1	4	clock
SD11	Auto precharge command period[1]	tRC	2	20	clock

[1] SD10 and SD11 are determined by SDRAM controller register settings.

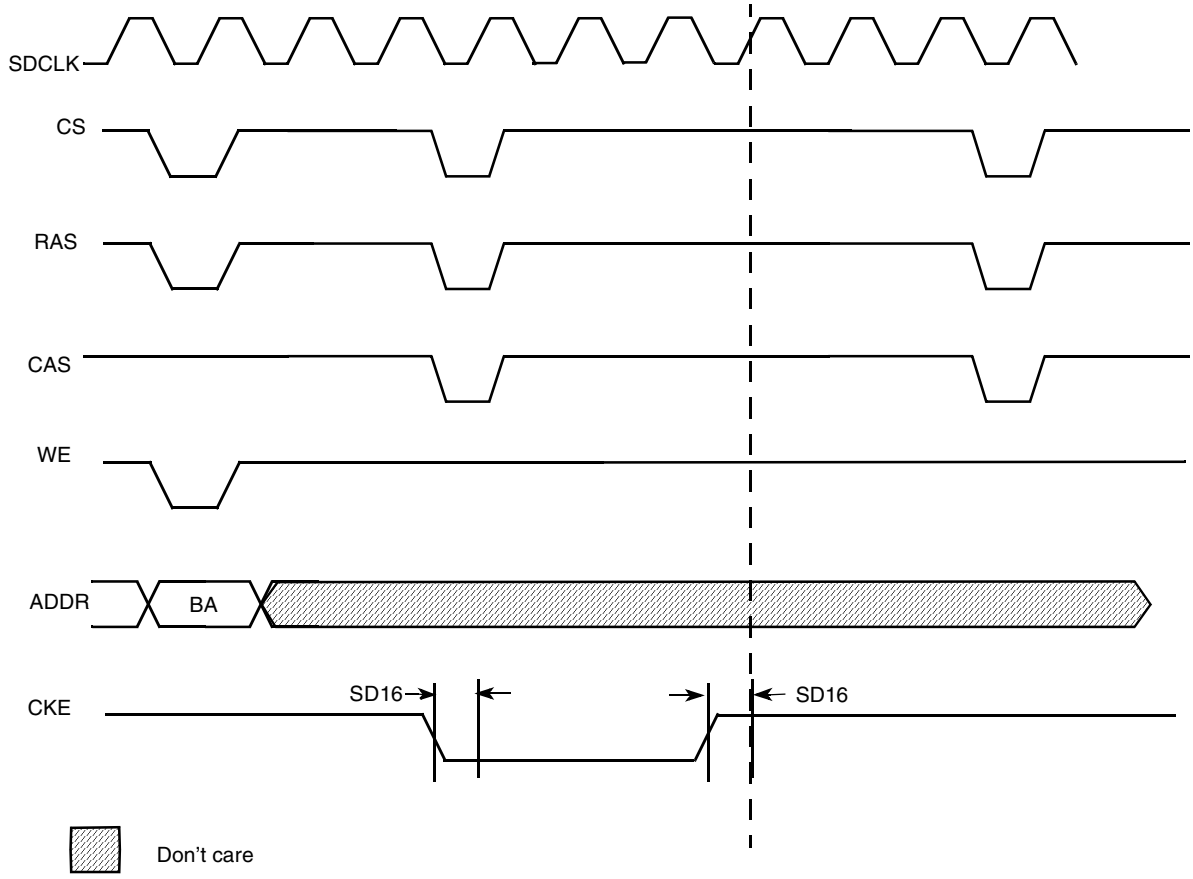

Figure 28. SDRAM Self-Refresh Cycle Timing Diagram

NOTE

The clock continues to run unless CKE is low. Then the clock is stopped in low state.

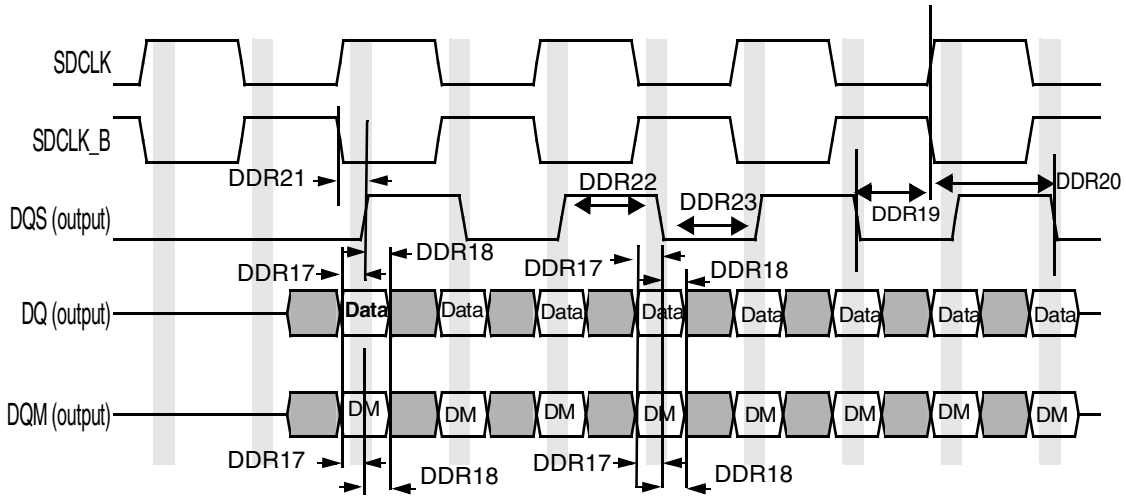

Figure 32. DDR2 SDRAM Write Cycle Timing Diagram

Table 52. DDR2 SDRAM Write Cycle Parameter Table

ID	Parameter	Symbol	DDR2-400		Unit
			Min.	Max.	
DDR17	DQ & DQM setup time to DQS (single-ended strobe)[1]	$t_{DS1(base)}$	0.6	—	ns
DDR18	DQ & DQM hold time to DQS (single-ended strobe)[1]	$t_{DH1(base)}$	0.6	—	ns
DDR19	Write cycle DQS falling edge to SDCLK output setup time	t_{DSS}	0.3	—	tCK
DDR20	Write cycle DQS falling edge to SDCLK output hold time	t_{DSH}	0.3	—	tCK
DDR21	DQS latching rising transitions to associated clock edges	t_{DQSS}	-0.2	0.2	tCK
DDR22	DQS high-level width	t_{DQSH}	0.35	—	tCK
DDR23	DQS low-level width	t_{DQSL}	0.35	—	tCK

[1] These values are for a DQ/DM slew rate of 1 V/ns and a DQS slew rate of 1 V/ns. For additional values use Table 53, “DtDS1, DtDH1 Derating Values for DDR2-400, DDR2-533.”

Table 53. ΔtDS1, ΔtDH1 Derating Values for DDR2-400, DDR2-533[1,2,3]

	DQS Single-Ended Slew Rate																	
	2.0 V/ns		1.5 V/ns		1.0 V/ns		0.9 V/ns		0.8 V/ns		0.7 V/ns		0.6 V/ns		0.5 Vns		0.4 V/ns	
	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1

[1] For the value of parameters WE4–WE21, see column BCD = 0 in Table 56.
[2] $\overline{CS}$ Assertion. This bit field determines when the $\overline{CS}$ signal is asserted during read/write cycles.
[3] $\overline{CS}$ Negation. This bit field determines when the $\overline{CS}$ signal is negated during read/write cycles.
[4] $\overline{BE}$ Assertion. This bit field determines when the $\overline{BE}$ signal is asserted during read cycles.
[5] $\overline{BE}$ Negation. This bit field determines when the $\overline{BE}$ signal is negated during read cycles.
[6] Output maximum delay from internal driving ADDR/control FFs to chip outputs.
[7] Output maximum delay from $\overline{CS}$[x] internal driving FFs to $\overline{CS}$[x] out.
[8] DATA maximum delay from chip input data to its internal FF.
[9] DTACK maximum delay from chip dtack input to its internal FF.

NOTE

All configuration parameters (CSA, CSN, EBWA, EBWN, LBA, LBN, LAH, OEN, OEA, EBRA, and EBRN) are in cycle units.

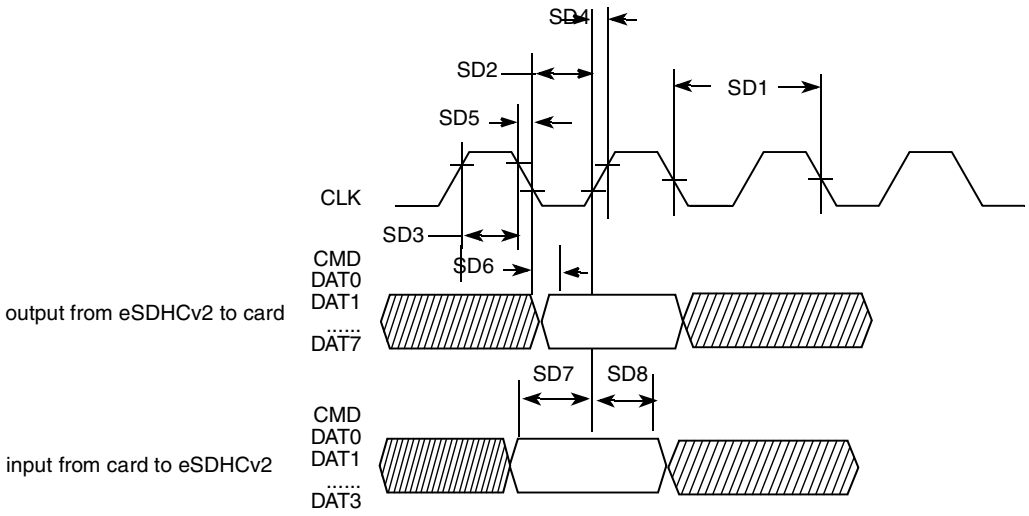

Figure 54. eSDHCv2 Timing

Table 61. eSDHCv2 Interface Timing Specification

ID	Parameter	Symbols	Min.	Max.	Unit
Card Input Clock					
SD1	Clock frequency (low speed)	f_{PP}[1]	0	400	kHz
	Clock frequency (SD/SDIO full speed/high speed)	f_{PP}[2]	0	25/50	MHz
	Clock frequency (MMC full speed/high speed)	f_{PP}[3]	0	20/52	MHz
	Clock frequency (identification mode)	f_{OD}	100	400	kHz
SD2	Clock low time	t_{WL}	6.5	—	ns
SD3	Clock high time	t_{WH}	6.5	—	ns
SD4	Clock rise time	t_{TLH}	—	3	ns
SD5	Clock fall time	t_{THL}	—	3	ns
eSDHC Output / Card Inputs CMD, DAT (Reference to CLK)					
SD6	eSDHC output delay	t_{OD}	–3	3	ns
eSDHC Input / Card Outputs CMD, DAT (Reference to CLK)					
SD7	eSDHC input setup time	t_{ISU}	2.5	—	ns
SD8	eSDHC input hold time	t_{IH}[4]	2.5	—	ns

1 In low-speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal-speed mode for SD/SDIO card, clock frequency can be any value between 0 ~ 25 MHz. In high speed mode, clock frequency can be any value between 0 ~ 50 MHz.

3 In normal-speed mode for MMC card, clock frequency can be any value between 0 ~ 20 MHz. In high speed mode, clock frequency can be any value between 0 ~ 52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

3.7.9 Fast Ethernet Controller (FEC) Timing

The FEC is designed to support both 10- and 100-Mbps Ethernet networks compliant with the IEEE 802.3 standard. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports 10/100 Mbps MII (18 pins altogether), 10/100 Mbps RMII (ten pins, including serial management interface) and the 10-Mbps-only 7-Wire interface (which uses seven of the MII pins), for connection to an external Ethernet transceiver. All signals are compatible with transceivers operating at a voltage of 3.3 V.

The following subsections describe the timing for MII and RMII modes.

3.7.9.1 FEC MII Mode Timing

The following subsections describe MII receive, transmit, asynchronous inputs, and serial management signal timings.

3.7.9.1.4 MII Receive Signal Timing (FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER, and FEC_RX_CLK)

The receiver functions correctly up to an FEC_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the FEC_RX_CLK frequency.

Figure 55 shows MII receive signal timings. Table 62 describes the timing parameters (M1–M4) shown in the figure.

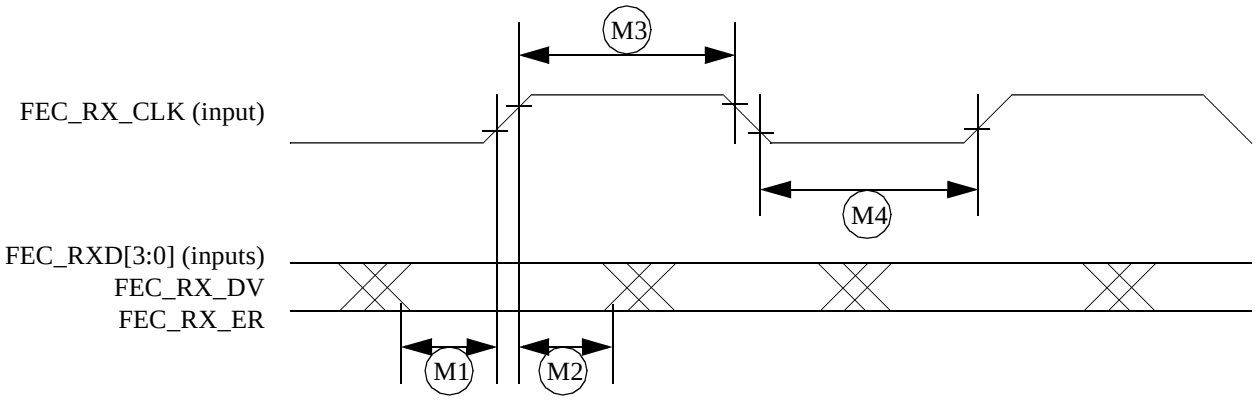

Figure 55. MII Receive Signal Timing Diagram

Table 62. MII Receive Signal Timing

ID	Characteristic[1]	Min.	Max.	Unit
M1	FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER to FEC_RX_CLK setup	5	—	ns
M2	FEC_RX_CLK to FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER hold	5	—	ns
M3	FEC_RX_CLK pulse width high	35%	65%	FEC_RX_CLK period
M4	FEC_RX_CLK pulse width low	35%	65%	FEC_RX_CLK period

[1] FEC_RX_DV, FEC_RX_CLK, and FEC_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

3.7.12 Liquid Crystal Display Controller (LCDC) Timing

Figure 65 and Figure 66 show LCDC timing in non-TFT and TFT mode respectively, and Table 71 and Table 72 list the timing parameters used in the associated figures.

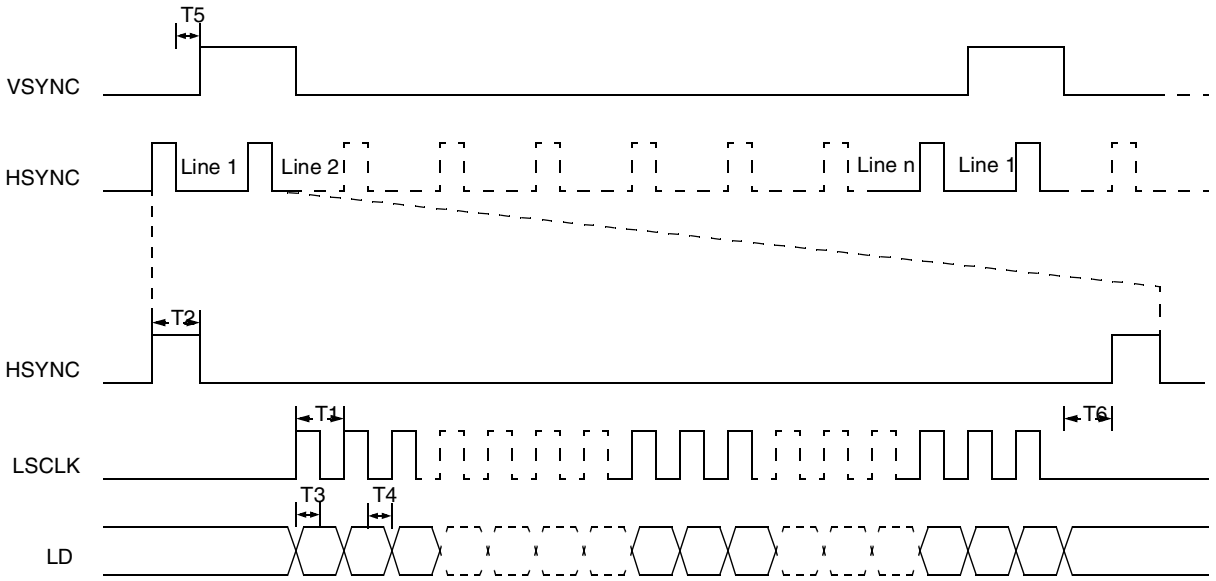

Figure 65. LCDC Non-TFT Mode Timing Diagram

Table 71. LCDC Non-TFT Mode Timing Parameters

ID	Description	Min.	Max.	Unit
T1	Pixel clock period	22.5	1000	ns
T2	HSYNC width	1	—	T[1]
T3	LD setup time	5	—	ns
T4	LD hold time	5	—	ns
T5	Wait between HSYNC and VSYNC rising edge	2	—	T[1]
T6	Wait between last data and HSYNC rising edge	1	—	T[1]

1 T is pixel clock period

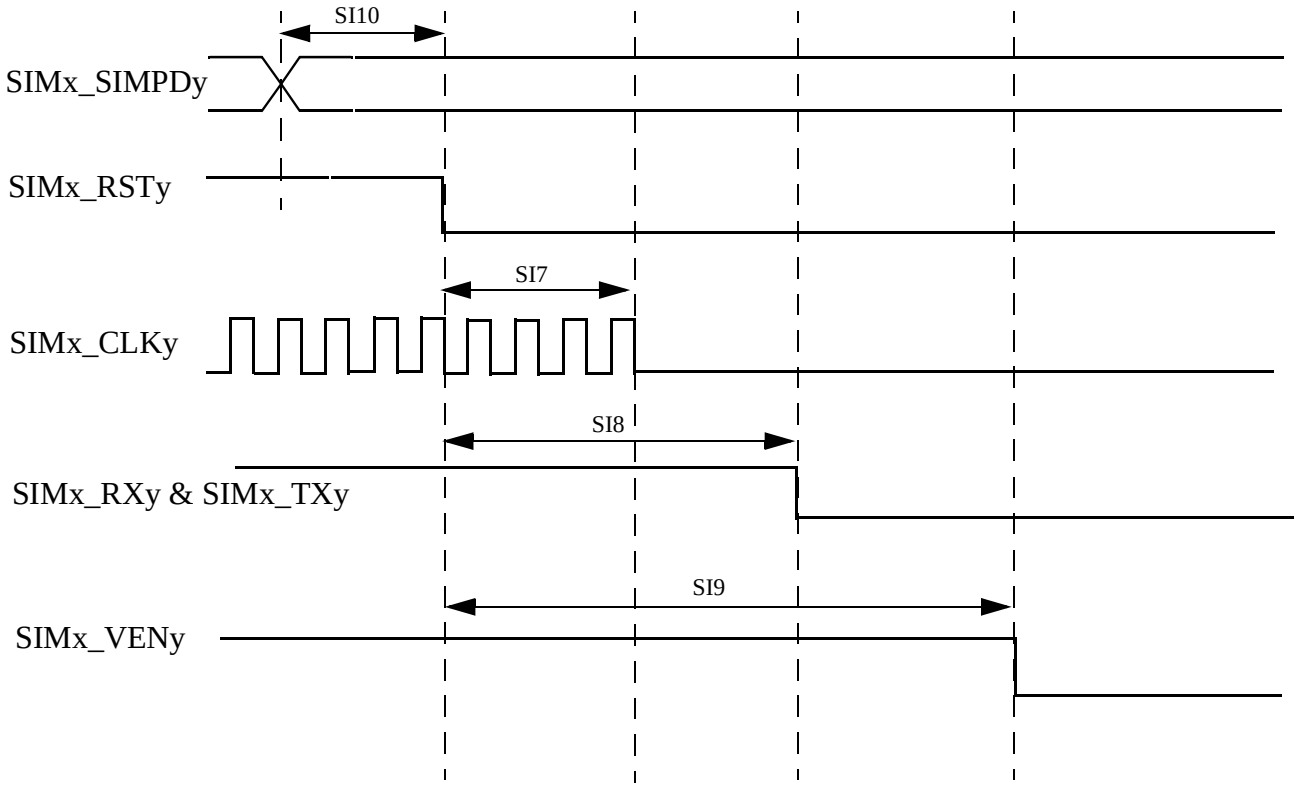

Figure 71. SmartCard Interface Power Down AC Timing

Table 77. Timing Requirements for Power-down Sequence

ID	PARAMETER	SYMBOL	Min.	Max.	Unit
SI7	SIM reset to SIM clock stop	$S_{rst2clk}$	0.9 × 1/Fckil	1.1 × 1/Fckil	ns
SI8	SIM reset to SIM Tx data low	$S_{rst2dat}$	1.8 × 1/Fckil	2.2 × 1/Fckil	ns
SI9	SIM reset to SIM voltage enable low	$S_{rst2ven}$	2.7 × 1/Fckil	3.3 × 1/Fckil	ns
SI10	SIM presence detect to SIM reset low	S_{pd2rst}	0.9 × 1/Fckil	1.1 × 1/Fckil	ns

3.7.15 System JTAG Controller (SJC) Timing

Figure 72 through Figure 75 show respectively the test clock input, boundary scan, test access port, and TRST timings for the SJC. Table 78 describes the SJC timing parameters (SJ1–SJ13) indicated in the figures.

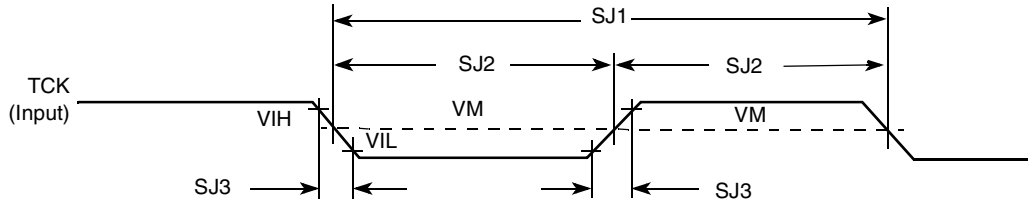

Figure 72. Test Clock Input Timing Diagram

3.7.19.2 UART Infrared (IrDA) Mode Timing

The following subsections describe the UART transmit and receive timing in IrDA mode.

3.7.19.2.3 UART IrDA Mode Transmit Timing

Figure 87 depicts the UART transmit timing in IrDA mode, showing only 8 data bits and 1 stop bit. Table 88 describes the timing parameters (UA3–UA4) shown in the figure.

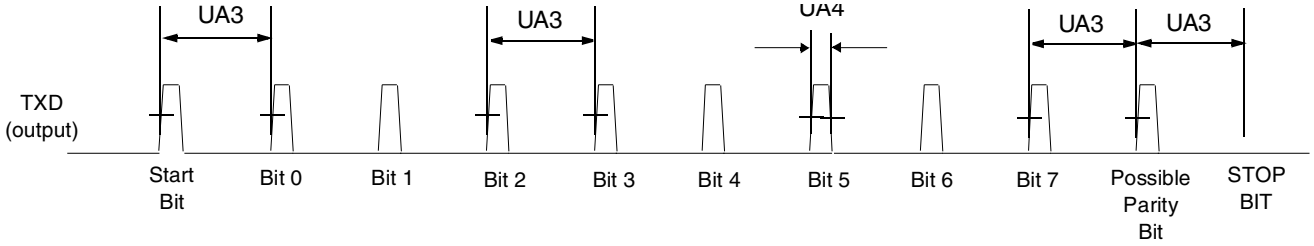

Figure 87. UART IrDA Mode Transmit Timing Diagram

Table 88. UART IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA3	Transmit bit time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR pulse duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16) \times (1/F_{baud\_rate}) + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

3.7.19.2.4 UART IrDA Mode Receive Timing

Figure 88 shows the UART receive timing for IrDA mode, for a format of 8 data bits and 1 stop bit. Table 89 describes the timing parameters (UA5–UA6) shown in the figure.

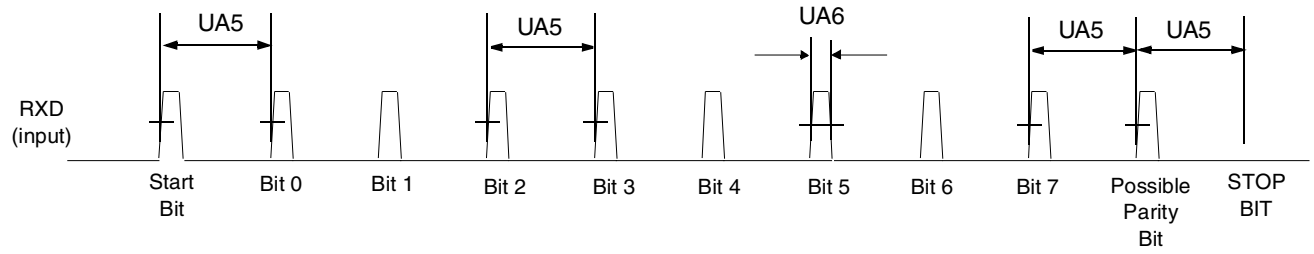

Figure 88. UART IrDA Mode Receive Timing Diagram

Table 89. UART IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
UA5	Receive bit time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR pulse duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

Figure 90 shows the USB receive waveform in DAT_SE0 bidirectional mode diagram.

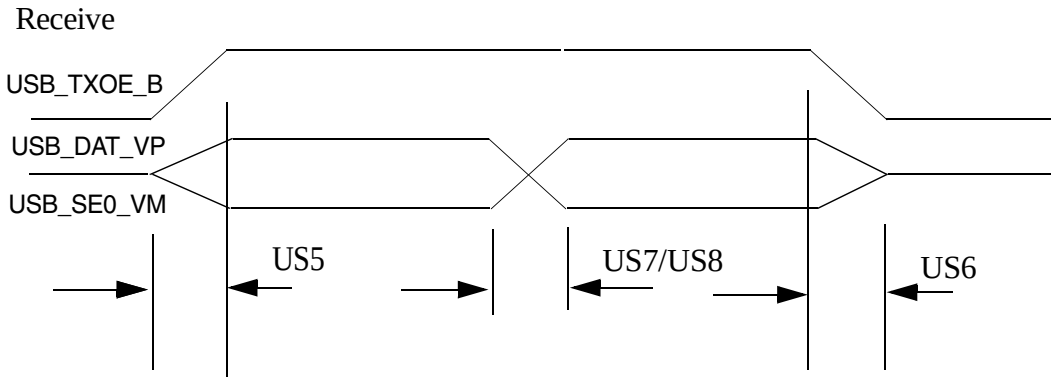

Figure 90. USB Receive Waveform in DAT_SE0 Bidirectional Mode

Table 91 shows the OTG port timing specification in DAT_SE0 bidirectional mode.

Table 91. OTG Port Timing Specification in DAT_SE0 Bidirectional Mode

No.	Parameter	Signal Name	Direction	Min.	Max.	Unit	Conditions/ Reference Signal
US1	Tx rise/fall time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US2	Tx rise/fall time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US3	Tx rise/fall time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US4	Tx duty cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US5	Enable Delay	USB_DAT_VP USB_SE0_VM	In	—	8.0	ns	USB_TXOE_B
US6	Disable Delay	USB_DAT_VP USB_SE0_VM	In	—	10.0	ns	USB_TXOE_B
US7	Rx rise/fall time	USB_DAT_VP	In	—	3.0	ns	35 pF
US8	Rx rise/fall time	USB_SE0_VM	In	—	3.0	ns	35 pF

3.7.20.1.2 DAT_SE0 Unidirectional Mode Timing

Table 92 defines the DAT_SE0 unidirectional mode signals.

Table 92. Signal Definitions—DAT_SE0 Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	Tx data when USB_TXOE_B is low
USB_SE0_VM	Out	SE0 drive when USB_TXOE_B is low
USB_VP1	In	Buffered data on DP when USB_TXOE_B is high
USB_VM1	In	Buffered data on DM when USB_TXOE_B is high
USB_RCV	In	Differential Rx data when USB_TXOE_B is high

Figure 95 shows the USB transmit waveform in VP_VM unidirectional mode diagram.

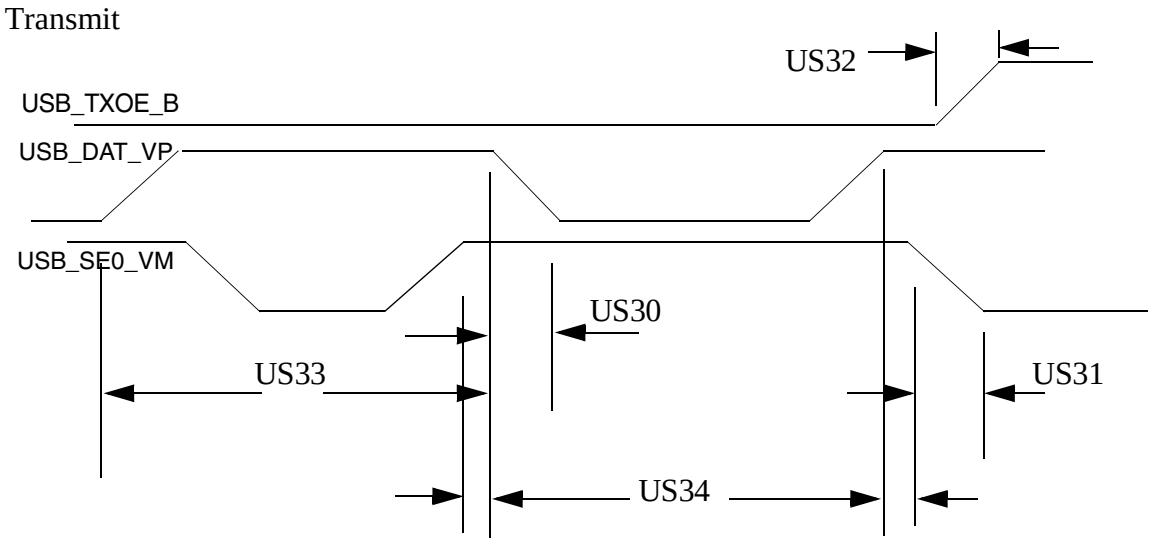

Figure 95. USB Transmit Waveform in VP_VM Unidirectional Mode

Figure 96 shows the USB receive waveform in VP_VM unidirectional mode diagram.

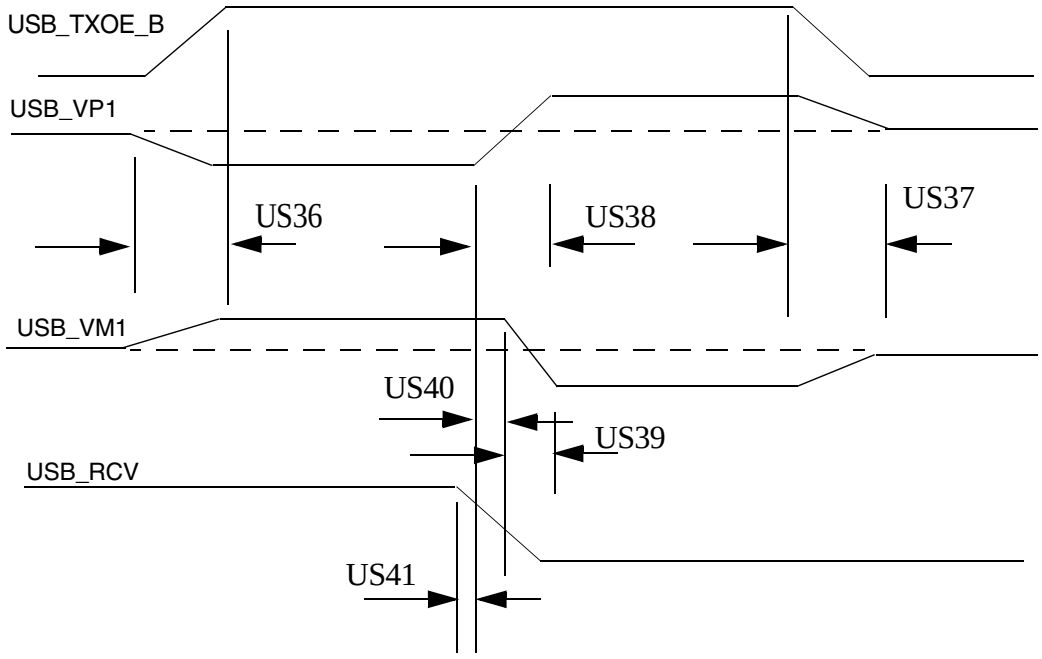

Figure 96. USB Receive Waveform in VP_VM Unidirectional Mode

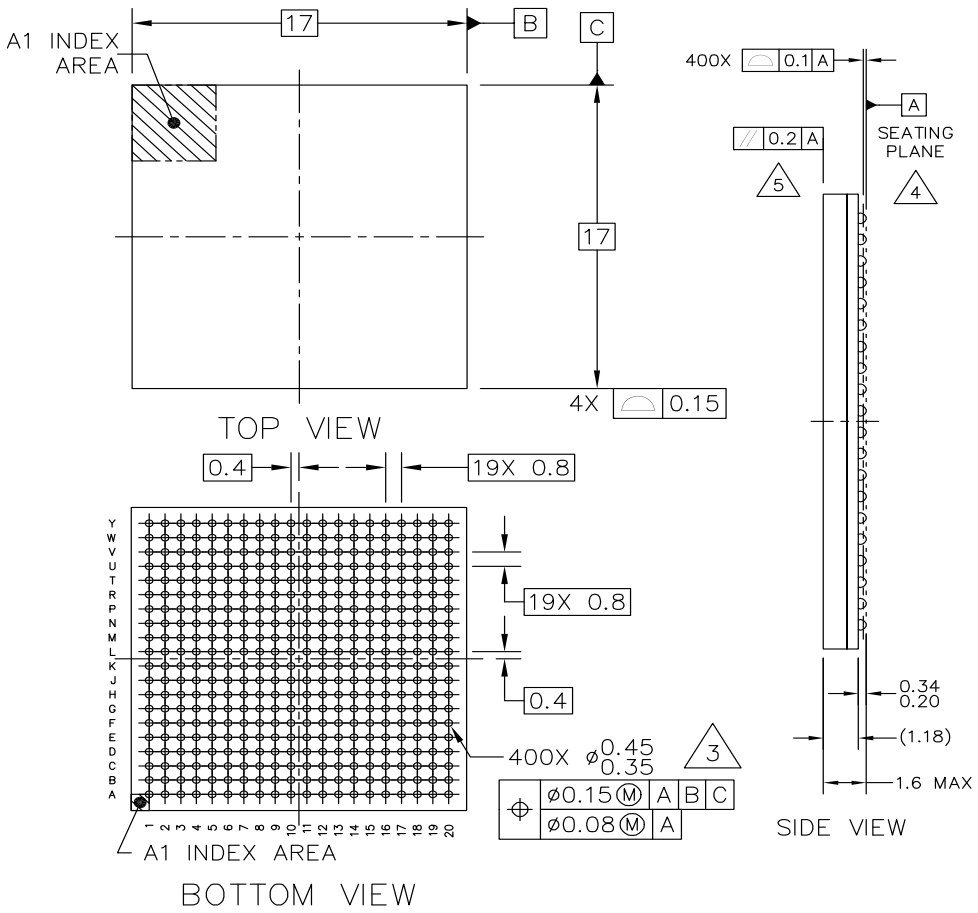

Figure 98. 17×17 i.MX25 Production Package

4.2 Ground, Power, Sense, and Reference Contact Assignments Case 17x17 mm, 0.8 mm Pitch

Table 100 shows the 17×17 mm package ground, power, sense, and reference contact assignments.

Table 100. 17×17 mm Package Ground, Power Sense, and Reference Contact Assignments

Contact Name	Contact Assignment
BATT_VDD	P10
FUSE_VDD	T17
MPLL_GND	U17
MPLL_VDD	U18
NGND_ADC	Y13
NVCC_ADC	W13
NVCC_CRM	N14
NVCC_CSI	J13, J14

Table 105. 12x12 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
WIPER	AA17	ADC	ANALOG	ANALOG	-
INAUX0	AA15	ADC	ANALOG	ANALOG	-
INAUX1	W14	ADC	ANALOG	ANALOG	-
INAUX2	AB16	ADC	ANALOG	ANALOG	-

1 The state immediately after reset and before ROM firmware or software has executed.

2 During power-on reset this port acts as input for fuse override signal.

3 During power-on reset this port acts as output for diagnostic signal.

Table 106 lists the 12×12 mm package i.MX25 no connect contact assignments.

Table 106. 12×12 mm Package i.MX25 No Connect Contact Assignments

Signal Name	Contact Assignment
NC_BGA_E4	E4
NC_BGA_L4	L4

4.8 i.MX25 12x12 Package Ball Map

Table 107 shows the i.MX25 12×12 package ball map.

Table 107. i.MX25 12×12 Package Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	QGND	EB0	OE	A14	A16	A18	A22	BCLK	DQM1	SD9	SD10	SD7	SD0	SD3	SD5	SDCKE0	SDBA0	CS3	A1	A0	A4	QGND
B	ECB	QGND	LBA	EB1	A10	A20	A24	SD14	SD12	SD11	SD6	SD2	SD4	QGND	SDWE	CAS	CS2	A2	A5	A7	QGND	A12
C	NFRE_B	CS0																			A11	CS1_D2
D	NFCLE	CS5		CS1	RW	A15	A21	A25	SD15	SD8	DQM0	SD1	SDCLK	SDCLK_B	RAS	SDBA1	A3	A6	A9		A13	CSI_D6
E	NFWE_B	NFALE		NC_BGA_E4	CS4	A17	A19		A23		SD13	SDQS1		SDQS0	NVCC_EMI2		MA10	QGND	A8		CSI_D4	CSI_D8
F	D1	D0		NF_CE0									QGND	QGND	NVCC_EMI2	SDCKE1		QGND	CSI_D3		CSI_D7	CSI_MCLK

Table 108. Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 7	12/2010	• Updated the first paragraph of Section 3.2.3, “SRTC DryIce Power-Up/Down Sequence.” • Updated Table 4, "Signal Considerations," on page 9 for NVCC_DRYICE signal. • Updated the third note for Table 6, "DC Operating Conditions," on page 11. • Added Table 9, "Recommended External Crystal Specifications," on page 13. • Added Table 10, "Recommended External Reference Clock Specifications," on page 13. • Added a note for the line NVCC_DRYICE in Table 100, "17×17 mm Package Ground, Power Sense, and Reference Contact Assignments," on page 125. • Updated Table 101, "17×17 mm Package i.MX25 Signal Contact Assignment," on page 127. • Added a note for the line NVCC_DRYICE in Table 104, "12x12 mm Package Ground, Power Sense, and Reference Contact Assignments," on page 139. • Removed records for UPLL_BYPCLK, USBPHY2_DP, USBPHY1RREF, USBPHY1_DM, USBPHY1_DP, USBPHY1_UID, USBPHY1_VBUS, and USBPHY2_DM contacts from Table 104, "12x12 mm Package Ground, Power Sense, and Reference Contact Assignments," on page 139. • Updated Table 105, "12x12 mm Package i.MX25 Signal Contact Assignment," on page 140.
Rev. 6	09/2010	• Added Section 3.2.3, “SRTC DryIce Power-Up/Down Sequence.”
Rev. 5	08/2010	• Updated Table 56, "WEIM Bus Timing Parameters," on page 69 to include new row for WE19. • Updated Table 6, "DC Operating Conditions," on page 11 to include Min and Max values of FUSE_VDD.
Rev. 4	06/2010	• Updated Table 1, “Ordering Information,” to include new part numbers.
Rev. 3	03/2010	• Updated Table 1, “Ordering Information,” to include new part numbers. • Added Table 2, “i.MX25 Parts Functional Differences.” • Added Section 3.3, “Power Characteristics.” • Added Section 4.5, “347 MAPBGA—Case 12 x 12 mm, 0.5 mm Pitch.” • Added Section 4.6, “Ground, Power, Sense, and Reference Contact Assignments Case 12x12 mm, 0.5 mm Pitch.” • Added Section 4.7, “Signal Contact Assignments—12 x 12 mm, 0.5 mm Pitch. • Added Section 4.8, “i.MX25 12x12 Package Ball Map.”
Rev. 2	12/2009	• Updated Table 1, “Ordering Information,” to include new part numbers.
Rev. 1	10/2009	• Updated Table 1, “Ordering Information,” to include new part numbers. • Updated DRYICE description in Table 3, “i.MX25 Digital and Analog Modules.” • Updated REF signal description in Table 4, “Signal Considerations.” • Updated ESD damage immunity values in Table 5, “DC Absolute Maximum Ratings.” • Updated values in Table 13, “i.MX25 Power Mode Current Consumption.” • Added a note on timing in Section 3.2.1, “Power-Up Sequence.” • Added Table 14, “iMX25 Reduced Power Mode Current Consumption.” • Updated Table 55, “NFC Timing Parameters.” • Updated values in Table 56, “WEIM Bus Timing Parameters. • Updated Table 85, “Touchscreen ADC Electrical Specifications.”
Rev. 0	6/2009	Initial release.