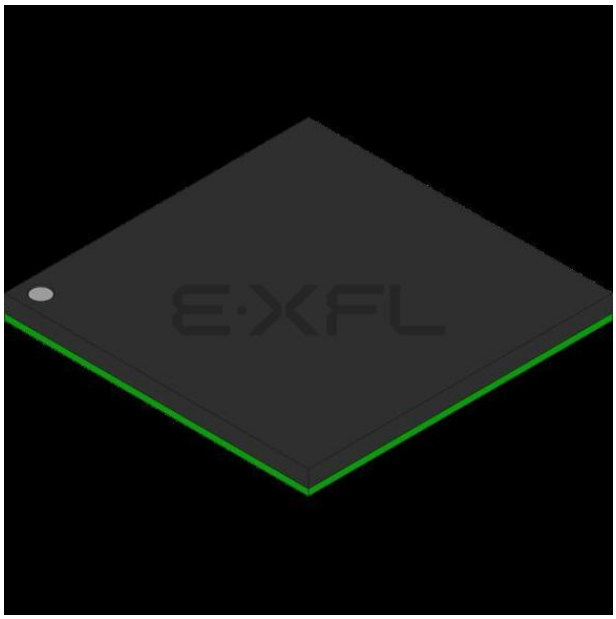

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	LPDDR, DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.0V, 2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Boot Security, Cryptography, Secure Fusebox, Secure JTAG, Secure Memory, Tamper Detection
Package / Case	400-LFBGA
Supplier Device Package	400-MAPBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx258cvm4

1.1 Ordering Information

Table 1 provides ordering information for the i.MX25.

Table 1. Ordering Information

Description	Part Number	Silicon Version	Projected Temperature Range (°C)	Package	Ballmap
i.MX253	MCIMX253DVM4	1.1	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257DVM4	1.1	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX253	MCIMX253CVM4	1.1	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257CVM4	1.1	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX258	MCIMX258CVM4	1.1	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX253	MCIMX253DJM4	1.1	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257DJM4	1.1	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX253	MCIMX253CJM4	1.1	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257CJM4	1.1	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX258	MCIMX258CJM4	1.1	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX253	MCIMX253DJM4A	1.2	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257DJM4A	1.2	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257DJM4AR2	1.2	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX253	MCIMX253CJM4A	1.2	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257CJM4A	1.2	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX258	MCIMX258CJM4A	1.2	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257CJN4A	1.2	–40 to +85	12 x 12mm, 0.5mm pitch, MAPBGA-347	Table 107

Table 3. i.MX25 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
I^2C(3)	I^2C module	Connectivity peripherals	Inter-IC Communication (I^2C) is an industry-standard, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. I^2C is suitable for applications requiring occasional communications over a short distance between many devices. The interface operates up to 100 kbps with maximum bus loading and timing. The I^2C system is a true multiple-master bus, including arbitration and collision detection that prevents data corruption if multiple devices attempt to control the bus simultaneously. This feature supports complex applications with multiprocessor control and can be used for rapid testing and alignment of end products through external connections to an assembly-line computer.
IIM	IC Identification Module	Security	The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, and various control signals requiring a fixed value.
IOMUX	I/O multiplexer	Pins	Each I/O multiplexer provides a flexible, scalable multiplexing solution: • Up to eight output sources multiplexed per pin • Up to four destinations for each input pin • Unselected input paths are held at constant level for reduced power consumption
KPP	Keypad port	Connectivity peripherals	KPP can be used for either keypad matrix scanning or general purpose I/O.
LCDC	LCD Controller	Multimedia peripherals	LCDC provides display data for external gray-scale or color LCD panels. LCDC is capable of supporting black-and-white, gray-scale, passive-matrix color (passive color or CSTN), and active-matrix color (active color or TFT) LCD panels.
MAX	ARM platform multilayer AHB crossbar switch	ARM platform	MAX concurrently supports up to five simultaneous connections between master ports and slave ports. MAX allows for concurrent transactions to occur from any master port to any slave port.
PWM(4)	Pulse width modulation	Connectivity peripherals	The Pulse-Width Modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. The PWM uses 16-bit resolution and a 4x16 data FIFO to generate sound.
SDMA	Smart DMA engine	System control	The SDMA provides DMA capabilities inside the processor. It is a shared module that implements 32 DMA channels.
SIM(2)	Subscriber identity module interface	Connectivity peripherals	The SIM is an asynchronous interface designed to facilitate communication with SIM cards or pre-paid phone cards. This module was designed based on the ISO7816 standard; however, the module does require an external companion controller to allow communication to certain smart cards or to pass certain certifications, such as EMV. The SIM supports only 11 and 12ETU cards and can communicate at the default rate, which is obtained at Fi/Di=372/1. An external companion controller is required to support cards aligned on 10.8 or 11.8ETU and to support other rates, such as those obtained at Fi/Di=372/2 and Fi/Di=372/4.
SJC	Secure JTAG interface	System control peripherals	The System JTAG Controller (SJC) provides debug and test control with maximum security.

Table 3. i.MX25 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SLCD	Smart LCD controller	Multimedia peripherals	The SLCDC module transfers data from the display memory buffer to the external display device.
SPBA	Shared peripheral bus arbiter	System control	The SPBA controls access to the shared peripherals. It supports shared peripheral ownership and access rights to an owned peripheral.
SSI(2)	I2S/SSI/AC97 interface	Connectivity peripherals	The SSI is a full-duplex serial port that allows the processor to communicate with a variety of serial protocols, including the Freescale Semiconductor SPI standard and the inter-IC sound bus standard (I2S). The SSIs interface to the AUDMUX for flexible audio routing.
TSC (and ADC)	Touchscreen controller (and A/D converter)	Multimedia peripherals	The touchscreen controller and associated Analog-to-Digital Converter (ADC) together provide a resistive touchscreen solution. The module implements simultaneous touchscreen control and auxiliary ADC operation for temperature, voltage, and other measurement functions.
UART(5)	UART interface	Connectivity peripherals	Each of the UART modules supports the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, one or two stop bits, programmable parity (even, odd, or none) • Programmable baud rates up to 4 MHz. This is a higher maximum baud rate than the 1.875 MHz specified by the TIA/EIA-232-F standard and previous Freescale UART modules. 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA-1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOTG USBHOST	High-speed USB on-the-go	Connectivity peripherals	The USB module provides high-performance USB On-The-Go (OTG) and host functionality (up to 480 Mbps), compliant with the USB 2.0 specification, the OTG supplement, and the ULPI 1.0 Low Pin Count specification. The module has DMA capabilities for handling data transfer between internal buffers and system memory. An OTG HS PHY and HOST FS PHY are also integrated.

2.1 Special Signal Considerations

Special signal considerations are listed in Table 4. The package contact assignment is found in Section 4, "Package Information and Contact Assignment." Signal descriptions are provided in the reference manual.

Table 4. Signal Considerations

Signal	Description
BAT_VDD	DryIce backup power supply input.
CLK0	Clock-out pin; renders the internal clock visible to users for debugging. The clock source is controllable through CRM registers. This pin can also be configured (through muxing) to work as a normal GPIO.
CLK_SEL	Used to select the ARM clock source from MPLL out or from external EXT_ARMCLK. In normal operation, CLK_SEL should be connected to GND.
EXT_ARMCLK	Primarily for Freescale factory use. There is no internal on-chip pull-up/down on this pin, so it must be externally connected to GND or VDD. Aside from factory use, this pin can also be configured (through muxing) to work as a normal GPIO.

[1] Sleep mode differs from stop mode in that the core voltage is reduced to 1 V.

Table 13 shows typical current consumption for the various power supplies under the various power modes.

Table 13. i.MX25 Power Mode Current Consumption

Power Group	Power Supplies	Voltage Setting	Current Consumption for Power Modes[1]			
			Doze	Wait	Stop	Sleep
NVCC_EMI	NVCC_EMI1 NVCC_EMI2	3.0 V	5 µA	3.15 µA	3.51 µA	3.61 µA
NVCC_CRM	NVCC_CRM	3.0 V	1.15 µA	4.31 µA	0.267 µA	0.32 µA
NVCC_ OTHER	NVCC_SDIO NVCC_CSI NVCC_NFC NVCC_JTAG NVCC_LCDC NVCC_MISC	3.0 V	31.2 µA	29.5 µA	31.7 µA	32.1 µA
NVCC_ADC	NVCC_ADC	3.0 V	163 µA	3.25 µA	1.14 µA	0.871 µA
OSC24M	OSC24M_ VDD	3.0 V	906 µA	903 µA	10.2 µA mA	10.5 µA
PLL_VDD	MPLL_VDD UPLL_VDD	1.4 V	6.83 mA	6.83 mA	38.9 µA	39.1 µA
QVDD	QVDD	1.15 V	8.79 mA	11.28 mA	842 µA	665 µA
USBPHY1_ VDDA	USBPHY1_ VDDA	3.17 V	240 µA	240 µA	241 µA	242 µA
USBPHY1_ VDDA_VBIAS	USBPHY1_ VDDA_VBIAS	3.17 V	0.6 µA	1.46 µA	0.328 µA	0.231 µA
USBPHY1_ UPLL_VDD	USBPHY1_ UPLL_VDD	3.17 V	201 µA	201 µA	191 µA	191 µA
USBPHY2	USBPHY2_ VDD	3.0 V	158 µA	0158 µA	164 µA	164 µA

[1] Values are typical, under typical use conditions.

In the reduced power mode, shown in Table 14, the i.MX25 is powered down, while the RTC clock and the secure keys (in secure-use case), remain operational. BAT_VDD is tied to a battery while all other supplies are turned off.

NOTE

In this low-power mode, i.MX25 cannot be woken up with an interrupt; it must be powered back up before it can detect any events.

NOTE

- The user is advised to connect FUSEVDD to GND except when fuses are programmed, to prevent unintentional blowing of fuses.
- Other power-up sequences may be possible; however, the above sequence has been verified and is recommended.
- There is a 1 ms minimum time between supplies coming up, and a 1 ms minimum time between POR_B assert and de-assert.
- The dV/dT should be no faster than 0.25 V/µs for all power supplies, to avoid triggering ESD circuit.

Figure 2 shows the power-up sequence diagram. After POR_B is asserted, Core VDD and NVDDx can be powered up. After Core VDD and NVDDx are stable, the analog supplies can be powered up.

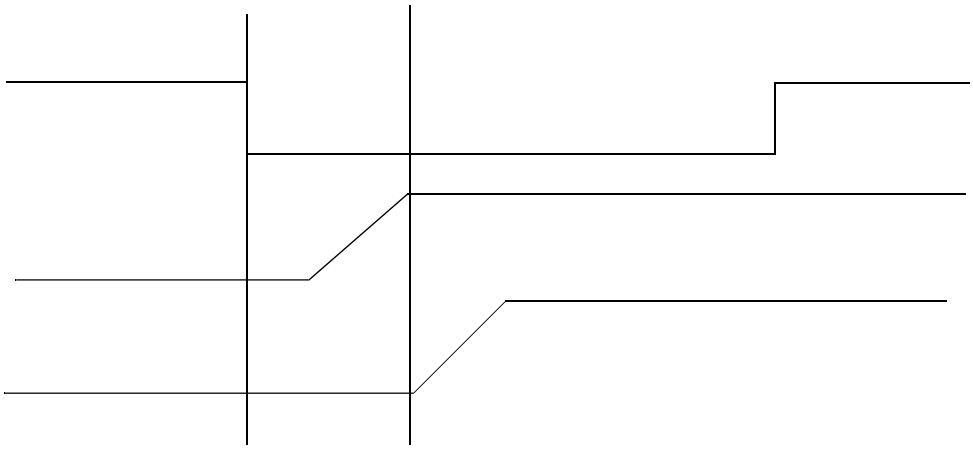

Figure 2. Power-Up Sequence Diagram

3.2.2 Power-Down Sequence

There are no special requirements for the power-down sequence. All power supplies can be shut down at the same time.

3.2.3 SRTC DryIce Power-Up/Down Sequence

In order to guarantee DryIce power-loss protection, including retention of SRTC time data during power down, users must do the following:

- Place a proper capacitor on the NVCC_DRYICE output pin, and
- Implement the below power-up/down sequence

1. Assert power on reset (POR).
2. Turn on NVCC_CRM.
3. Turn on QVDD digital logic domain supplies for not less than 1 ms and not more than 32 ms, after NVCC_CRM reaches 90% of 3.3 V.

Table 20. GPIO DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input hysteresis	VHYS	OVDD = 3.3 V OVDD = 1.8V	370 290	—	420 320	mV
Schmitt trigger VT+[1]	VT+	—	0.5 × OVDD	—	—	V
Schmitt trigger VT–[1]	VT–	—	—	—	0.5 × OVDD	V
Pull-up resistor (22 kΩ PU)	Rpu	Vi=0	18.5	22	25.6	kΩ
Pull-up resistor (47 kΩ PU)	Rpu	Vi=0	41	47	55	kΩ
Pull-up resistor (100 kΩ PU)	Rpu	Vi=0	85	100	120	kΩ
Pull-down resistor (100 kΩ PD)	Rpd	VI = OVDD	85	100	120	kΩ
Input current (no pull-up/down)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	—	—	100 60 77 50	nA
Input current (22 kΩ PU)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	117 0.0001 64 0.0001	—	184 0.0001 104 0.0001	µA
Input current (47 kΩ PU)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	54 0.0001 30 0.0001	—	88 0.0001 49 0.0001	µA
Input current (100 kΩ PU)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	25 0.0001 14 0.0001	—	42 0.0001 23 0.0001	µA
Input current (100 kΩ PD)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	25 0.0001 14 0.0001	—	42 0.001 23 0.0001	µA
High-impedance I/O supply current	Icc–ovdd	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	—	—	688 688 560 560	nA
High-impedance core supply current	Icc–vddi	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	—	—	490 490 410 410	nA

[1] Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

3.6 AC Electrical Characteristics

This section provides the AC parameters for slow and fast I/O.

Table 22. Fast I/O AC Parameters for OVDD = 1.65–1.95 V (continued)

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Output pad dI/dt[3] (max. drive)	tdit	25 pF 50 pF	7 7	43 46	112 118	mA/ns
Output pad dI/dt[3] (high drive)	tdit	25 pF 50 pF	11 12	31 33	81 85	mA/ns
Output pad dI/dt[3] (standard drive)	tdit	25 pF 50 pF	9 10	27 28	71 74	mA/ns
Input pad propagation delay without hysteresis, 50%–50%[4]	tpi	1.6 pF	0.74/1	1.1/1.5	1.75/2.16	ns
Input pad propagation delay with hysteresis, 50%–50%[4]	tpi	1.6 pF	1.75/1.63	2.67/2.22	2.92/3	ns
Input pad propagation delay without hysteresis, 40%–60%[4]	tpi	1.6 pF	1.82/1.55	2.28/1.87	2.95/2.54	ns
Input pad propagation delay with hysteresis, 40%–60%[4]	tpi	1.6 pF	2.4/2.6	3/3.07	3.77/3.71	ns
Input pad transition times without hysteresis[4]	trfi	1.6 pF	0.16/0.12	0.30/0.18	0.33/0.29	ns
Input pad transition times with hysteresis[4]	trfi	1.6 pF	0.16/0.13	0.30/0.18	0.33/0.29	ns
Maximum input transition times[5]	trm	—	—	—	25	ns

1 Maximum condition for tpr, tpo, and tpv: wcs model, 1.1 V, I/O 1.65 V, and 105 °C. Minimum condition for tpr, tpo, and tpv: bcs model, 1.3 V, I/O 1.95 V, and –40 °C. Input transition time from core is 1 ns (20%–80%).

2 Minimum condition for tps: wcs model, 1.1 V, I/O 1.65 V and 105 °C. tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

3 Maximum condition for tdit: bcs model, 1.3 V, I/O 1.95 V and –40 °C.

4 Maximum condition for tpi and trfi: wcs model, 1.1 V, I/O 1.65 V and 105 °C. Minimum condition for tpi and trfi: bcs model, 1.3 V, I/O 1.95 V and –40 °C. Input transition time from pad is 5 ns (20%–80%).

5 Hysteresis mode is recommended for input with transition time greater than 25 ns.

Table 23 shows the fast I/O AC parameters for OVDD = 3.0–3.6 V.

Table 23. Fast I/O AC Parameters for OVDD = 3.0–3.6 V

Parameter	Symbol	Test Condition	Min. Rise/Fall	Typ.	Max. Rise/Fall	Units
Duty Cycle	Fduty		40		60	%
Output Pad Transition Times[1] (Max Drive)	tpr	25 pF 50 pF	0.80/0.70 1.40/1.60	1.12/2.51 1.60/2.39	1.64/1.32 2.84/2.10	ns
Output Pad Transition Times[1] (High Drive)	tpr	25 pF 50 pF	1.00/0.90 1.95/1.66	1.43/1.16 2.66/2.09	2.05/1.60 3.70/2.80	ns
Output Pad Transition Times[1] (Standard Drive)	tpr	25 pF 50 pF	1.50/1.30 2.90/2.50	2.09/1.67 3.40/3.09	3.00/2.30 5.56/4.12	ns
Output Pad Propagation Delay[1] (Max Drive), 50%–50%	tpo	25 pF 50 pF	1.20/1.28 1.67/1.75	1.74/1.73 2.39/2.32	2.67/2.52 3.58/3.33	ns

Figure 9 and Figure 10 show write 1 and read sequence timing, respectively. Table 34 describes the timing parameters (OW7–OW8) that are shown in the figure.

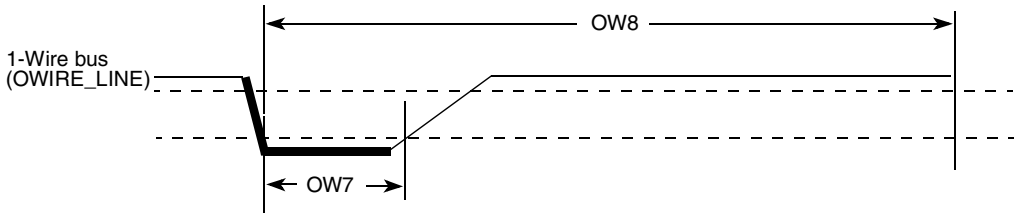

Figure 9. Write 1 Sequence Timing Diagram

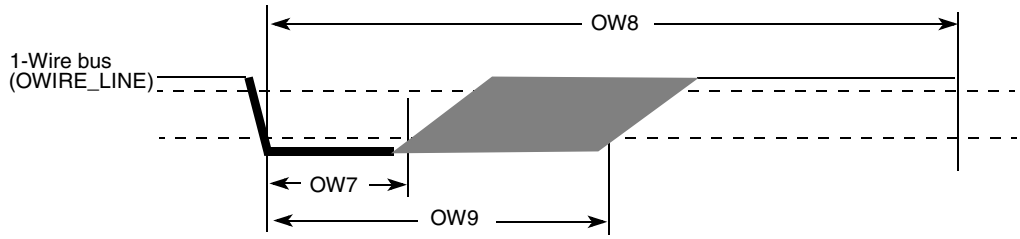

Figure 10. Read Sequence Timing Diagram

Table 34. WR1 /RD Timing Parameters

ID	Parameter	Symbol	Min.	Typ.	Max.	Units
OW7	Write 1 / read low time	t_{LOW1}	1	5	15	µs
OW8	Transmission time slot	t_{SLOT}	60	117	120	µs
OW9	Release time	$t_{RELEASE}$	15	—	45	µs

3.7.2.2 Multiword DMA (MDMA) Mode Timing

Figure 13 and Figure 14 show the timing for MDMA read and write modes, respectively.

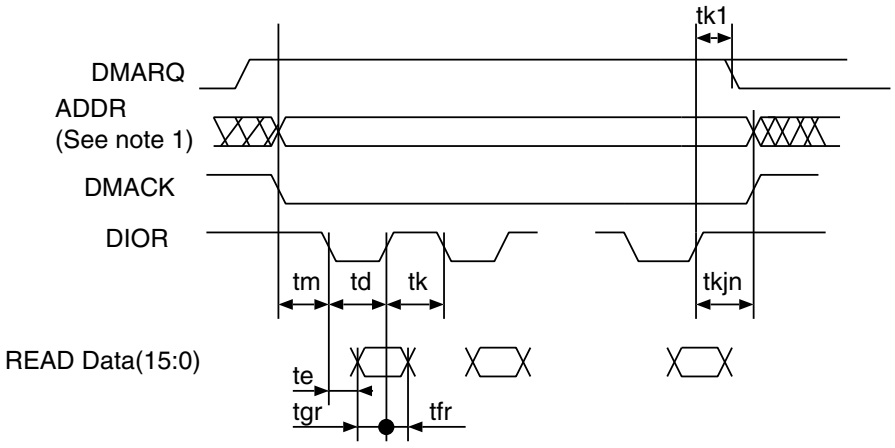

Figure 13. MDMA Read Mode Timing

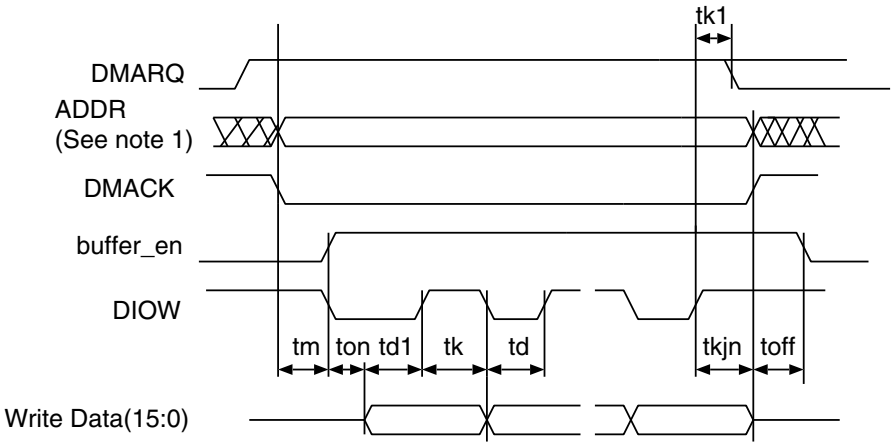

Figure 14. MDMA Write Mode Timing

Table 41. CSI Gated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI VSYNC to HSYNC time	tV2H	67.5	—	ns
P2	CSI HSYNC setup time	tHsu	1	—	ns
P3	CSI DATA setup time	tDsu	1	—	ns
P4	CSI DATA hold time	tDh	1.2	—	ns
P5	CSI pixel clock high time	tCLKh	10	—	ns
P6	CSI pixel clock low time	tCLKl	10	—	ns
P7	CSI pixel clock frequency	fCLK	—	48 ± 10%	MHz

3.7.4.2 Ungated Clock Mode Timing

Figure 22 shows the ungated clock mode timings of CSI, and Table 42 describes the timing parameters (P1–P6) that are shown in the figure. In ungated mode the VSYNC and PIXCLK signals are used, and the HSYNC signal is ignored.

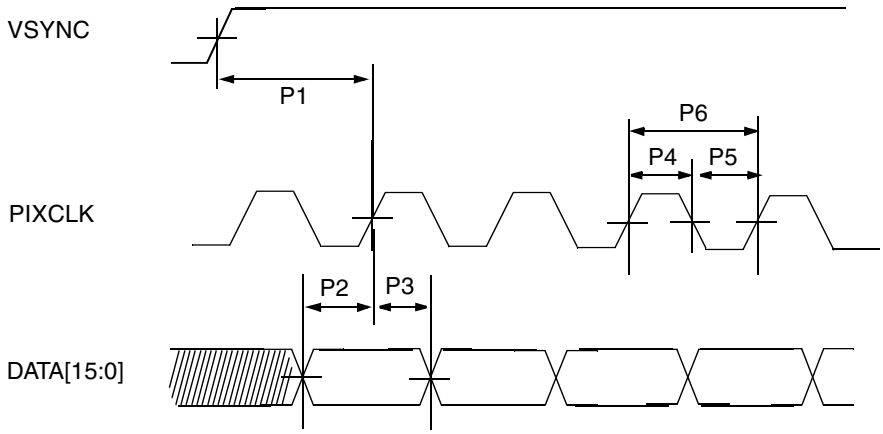

Figure 22. CSI Ungated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

Table 42. CSI Ungated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI VSYNC to pixel clock time	tVSYNC	67.5	—	ns
P2	CSI DATA setup time	tDsu	1	—	ns
P3	CSI DATA hold time	tDh	1.2	—	ns
P4	CSI pixel clock high time	tCLKh	10	—	ns
P5	CSI pixel clock low time	tCLKl	10	—	ns
P6	CSI pixel clock frequency	fCLK	—	48 ± 10%	MHz

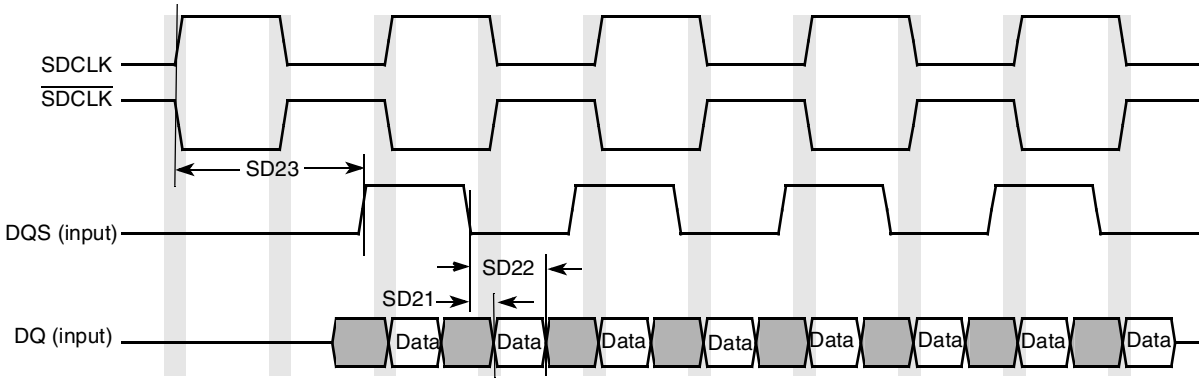

Figure 30. Mobile DDR SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 49. Mobile DDR SDRAM Read Cycle Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Unit
SD21	DQS – DQ Skew (defines the data valid window in read cycles related to DQS)	tDQSQ	—	0.85	ns
SD22	DQS DQ HOLD time from DQS	tQH	2.3	—	ns
SD23	DQS output access time from SDCLK posedge	tDQSCK	—	6.7	ns

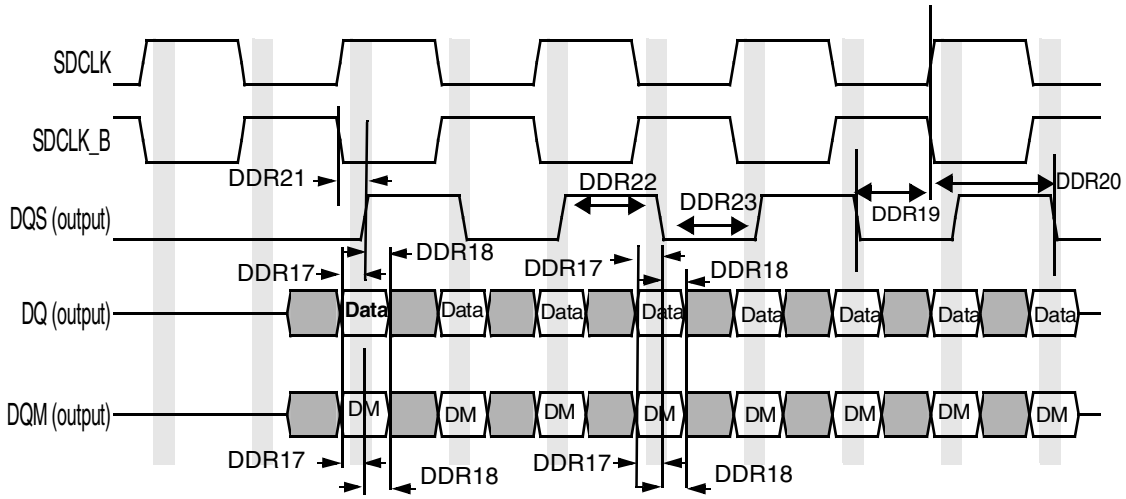

Figure 32. DDR2 SDRAM Write Cycle Timing Diagram

Table 52. DDR2 SDRAM Write Cycle Parameter Table

ID	Parameter	Symbol	DDR2-400		Unit
			Min.	Max.	
DDR17	DQ & DQM setup time to DQS (single-ended strobe)[1]	$t_{DS1(base)}$	0.6	—	ns
DDR18	DQ & DQM hold time to DQS (single-ended strobe)[1]	$t_{DH1(base)}$	0.6	—	ns
DDR19	Write cycle DQS falling edge to SDCLK output setup time	t_{DSS}	0.3	—	tCK
DDR20	Write cycle DQS falling edge to SDCLK output hold time	t_{DSH}	0.3	—	tCK
DDR21	DQS latching rising transitions to associated clock edges	t_{DQSS}	-0.2	0.2	tCK
DDR22	DQS high-level width	t_{DQSH}	0.35	—	tCK
DDR23	DQS low-level width	t_{DQSL}	0.35	—	tCK

[1] These values are for a DQ/DM slew rate of 1 V/ns and a DQS slew rate of 1 V/ns. For additional values use Table 53, “DtDS1, DtDH1 Derating Values for DDR2-400, DDR2-533.”

Table 53. ΔtDS1, ΔtDH1 Derating Values for DDR2-400, DDR2-533[1,2,3]

	DQS Single-Ended Slew Rate																	
	2.0 V/ns		1.5 V/ns		1.0 V/ns		0.9 V/ns		0.8 V/ns		0.7 V/ns		0.6 V/ns		0.5 Vns		0.4 V/ns	
	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1

Table 57. WEIM Asynchronous Timing Parameters Relative to Chip Select Table (continued)

Ref No.	Parameter	Determination By Synchronous Measured Parameters[1]	Min	Max (If 133 MHz is supported by SoC)	Unit
WE32A(muxed A/D	$\overline{CS}$[x] valid to Address Invalid	WE4 – WE7 + (LBN + LBA + 1 – CSA[2])	–3 + (LBN + LBA + 1 – CSA)	—	ns
WE33	$\overline{CS}$[x] Valid to $\overline{RW}$ Valid	WE8 – WE6 + (RWA – CSA)	—	3 + (RWA – CSA)	ns
WE34	$\overline{RW}$ Invalid to $\overline{CS}$[x] Invalid	WE7 – WE9 + (RWN – CSN)	—	3 – (RWN_CSN)	ns
WE35	$\overline{CS}$[x] Valid to $\overline{OE}$ Valid	WE10 – WE6 + (OEA – CSA)	—	3 + (OEA – CSA)	ns
WE35A (muxed A/D)	$\overline{CS}$[x] Valid to $\overline{OE}$ Valid	WE10 – WE6 + (OEA + LBN + LBA + LAH + 1 – CSA)	–3 + (OEA + LBN + LBA + LAH + 1 – CSA)	3 + (OEA + LBN + LBA + LAH + 1 – CSA)	ns
WE36	$\overline{OE}$ Invalid to $\overline{CS}$[x] Invalid	WE7 – WE11 + (OEN – CSN)	—	3 – (OEN – CSN)	ns
WE37	$\overline{CS}$[x] Valid to $\overline{EB}$[y] Valid (Read access)	WE12 – WE6 + (EBRA – CSA)	—	3 + (EBRA[4] – CSA)	ns
WE38	$\overline{EB}$[y] Invalid to $\overline{CS}$[x] Invalid (Read access)	WE7 – WE13 + (EBRN – CSN)	—	3 – (EBRN[5] – CSN)	ns
WE39	$\overline{CS}$[x] Valid to $\overline{LBA}$ Valid	WE14 – WE6 + (LBA – CSA)	—	3 + (LBA – CSA)	ns
WE40	$\overline{LBA}$ Invalid to $\overline{CS}$[x] Invalid	WE7 – WE15 – CSN	—	3 – CSN	ns
WE40A (muxed A/D)	$\overline{CS}$[x] Valid to $\overline{LBA}$ Invalid	WE14 – WE6 + (LBN + LBA + 1 – CSA)	–3 + (LBN + LBA + 1 – CSA)	3 + (LBN + LBA + 1 – CSA)	ns
WE41	$\overline{CS}$[x] Valid to Output Data Valid	WE16 – WE6 – CSA	—	3 – CSA	ns
WE41A (muxed A/D)	$\overline{CS}$[x] Valid to Output Data Valid	WE16 – WE6 + (LBN + LBA + LAH + 1 – CSA)	—	3 + (LBN + LBA + LAH + 1 – CSA)	ns
WE42	Output Data Invalid to $\overline{CS}$[x] Invalid	WE17 – WE7 – CSN	—	3 – CSN	ns
WE43	Input Data Valid to $\overline{CS}$[x] Invalid	MAXCO – MAXCSO + MAXDI	MAXCO[6] – MAXCSO[7] + MAXDI[8]	—	ns
WE44	$\overline{CS}$[x] Invalid to Input Data invalid	0	0	—	ns
WE45	$\overline{CS}$[x] Valid to $\overline{EB}$[y] Valid (Write access)	WE12 – WE6 + (EBWA – CSA)	—	3 + (EBWA – CSA)	ns
WE46	$\overline{EB}$[y] Invalid to $\overline{CS}$[x] Invalid (Write access)	WE7 – WE13 + (EBWN – CSN)	—	–3 + (EBWN – CSN)	ns
WE47	$\overline{DTACK}$ Valid to $\overline{CS}$[x] Invalid	MAXCO – MAXCSO + MAXDTI	MAXCO[6] – MAXCSO[7] + MAXDTI[9]	—	ns
WE48	$\overline{CS}$[x] Invalid to $\overline{DTACK}$ invalid	0	0	—	ns

3.7.17.4 SSI Receiver Timing with External Clock

Figure 81 shows the timing for SSI receiver with external clock. Table 84 describes the timing parameters (SS22–SS41) used in the figure.

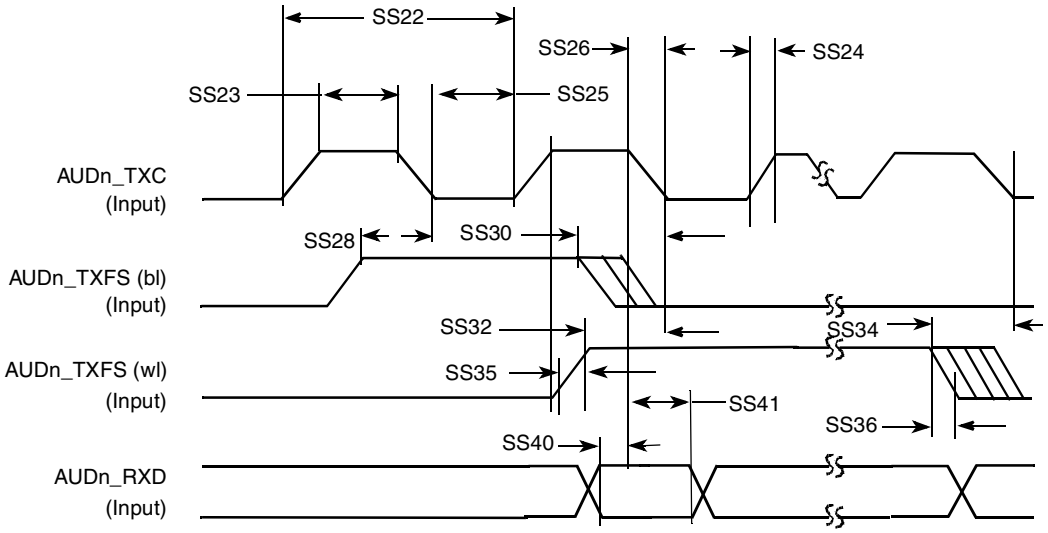

Figure 81. SSI Receiver with External Clock Timing Diagram

Table 84. SSI Receiver Timing with External Clock

ID	Parameter	Min.	Max.	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	FS (bl) low/high setup before (Tx) CK falling	–10.0	15.0	ns
SS30	FS (bl) low/high setup before (Tx) CK falling	10.0	—	ns
SS32	FS (wl) low/high setup before (Tx) CK falling	–10.0	15.0	ns
SS34	FS (wl) low/high setup before (Tx) CK falling	10.0	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10.0	—	ns
SS41	SRXD hold time after (Rx) CK low	2.0	—	ns

Note:

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on pads when SSI is being used for data transfer.

Table 101. 17×17 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
SD3	D14	EMI1	DDR	INPUT	Keeper
SD4	D13	EMI1	DDR	INPUT	Keeper
SD5	A13	EMI1	DDR	INPUT	Keeper
SD6	D12	EMI1	DDR	INPUT	Keeper
SD7	A10	EMI1	DDR	INPUT	Keeper
SD8	B9	EMI1	DDR	INPUT	Keeper
SD9	D10	EMI1	DDR	INPUT	Keeper
SD10	B10	EMI1	DDR	INPUT	Keeper
SD11	C10	EMI1	DDR	INPUT	Keeper
SD12	C9	EMI1	DDR	INPUT	Keeper
SD13	A9	EMI1	DDR	INPUT	Keeper
SD14	D9	EMI1	DDR	INPUT	Keeper
SD15	A8	EMI1	DDR	INPUT	Keeper
SDBA1	A16	EMI2	DDR	OUTPUT	Low
SDBA0	B15	EMI2	DDR	OUTPUT	Low
DQM0	C12	EMI1	DDR	OUTPUT	High
DQM1	C8	EMI1	DDR	OUTPUT	High
RAS	C14	EMI2	DDR	OUTPUT	High
CAS	C16	EMI2	DDR	OUTPUT	High
SDWE	A15	EMI2	DDR	OUTPUT	High
SDCKE0	D15	EMI2	DDR	OUTPUT	High
SDCKE1	C15	EMI2	DDR	OUTPUT	High
SDCLK	B14	EMI2	DDR	OUTPUT	Low
SDCLK_B	A14	EMI2	DDR	OUTPUT	High
SDQS0	B12	EMI2	DDR	INPUT	Keeper
SDQS1	B8	EMI2	DDR	INPUT	Keeper
EB0	B3	EMI1	DDR	OUTPUT	High
EB1	C5	EMI1	DDR	OUTPUT	High
OE	D6	EMI1	DDR	OUTPUT	High
CS0	C3	EMI1	DDR	OUTPUT	High
CS1	D3	EMI1	DDR	OUTPUT	High
CS2	B16	EMI2	DDR	OUTPUT	High

4.5 347 MAPBGA—Case 12 x 12 mm, 0.5 mm Pitch

Figure 99 shows the 12×12 mm i.MX25 production package. The following notes apply to Figure 99:

- All dimensions in millimeters.Dimensioning and tolerancing per ASME Y14.5M-1994.
- Maximum solder ball diameter measured parallel to datum A.
- Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
- Parallelism measurement shall exclude any effect of mark on package's top surface.

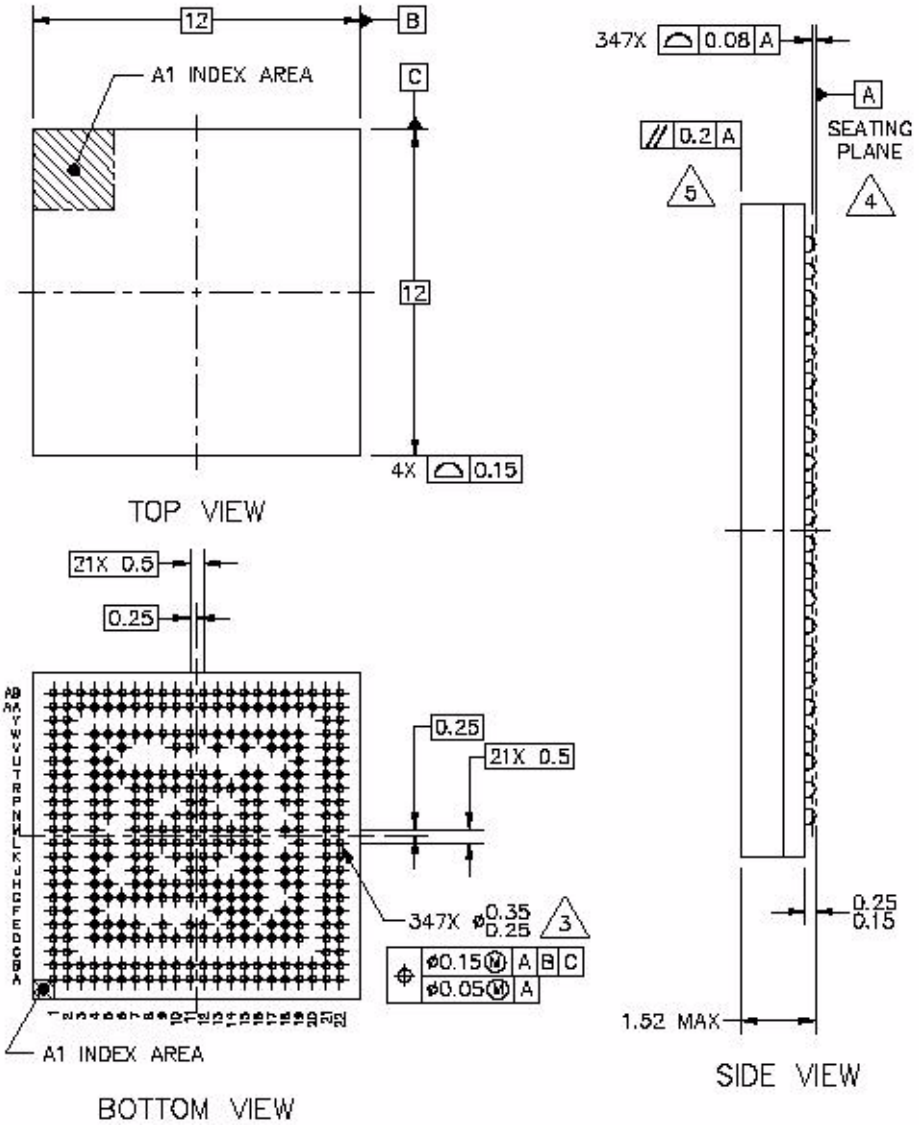

Figure 99. 12×12 mm i.MX25 Production Package

4.6 Ground, Power, Sense, and Reference Contact Assignments Case 12x12 mm, 0.5 mm Pitch

Table 104 shows the 12×12 mm package ground, power, sense, and reference contact assignment.

Table 104. 12x12 mm Package Ground, Power Sense, and Reference Contact Assignments

Contact Name	Contact Assignment
BATT_VDD	AA10
FUSE_VDD	P18
MPLL_GND	V17
MPLL_VDD	W19
NGND_ADC	N15
NVCC_ADC	P15
NVCC_CRM	P16
NVCC_CSI	J15, J16
NVCC_DRYICE[1]	R14
NVCC_EMI1	G8, G9, G10, H8, H9, H10
NVCC_EMI2	E15, F15, G15, G16, H15, H16
NVCC_JTAG	W10
NVCC_LCDC	R8, R9, T8
NVCC_MISC	P7, P8, R7, T7
NVCC_NFC	J7, J8, K7, K8
NVCC_SDIO	N19
OSC24M_GND	T15
OSC24M_VDD	V15
QGND	A1, A22, B2, B14, B21, E18, F13, F14, F18, G6, G11, G12, G14, H11, H12, H14, J12, K10, K11, K12, K13, L7, L8, L9, L10, L11, L12, L13, L14, L15, L16, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, N10, N11, N12, N13, P11, P12, R11, R12, R18, T5, T6, T11, T12, T18, V18, V19, W2, W9, Y21, AA2, AA21, AB1, AB18, AB21, AB22, J11
QVDD	G7, G13, H7, H13, H18, J18, N7, N8, R10, R15, R16, T9, T10, V10,
REF	AA14
UPLL_GND	N16
UPLL_VDD	M18
USBPHY1_UPLLVDD	L21
USBPHY1_UPLLVSS	M19
USBPHY1_VDDA	K15, K16
USBPHY1_VDDA_BIAS	L22

Table 105. 12x12 mm Package i.MX25 Signal Contact Assignment (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuration after Reset[1]
SDCLK_B	D14	EMI2	DDR	OUTPUT	High
SDQS0	E14	EMI2	DDR	INPUT	Keeper
SDQS1	E12	EMI2	DDR	INPUT	Keeper
EB0	A2	EMI1	DDR	OUTPUT	High
EB1	B4	EMI1	DDR	OUTPUT	High
OE	A3	EMI1	DDR	OUTPUT	High
CS0	C2	EMI1	DDR	OUTPUT	High
CS1	D4	EMI1	DDR	OUTPUT	High
CS2	B17	EMI2	DDR	OUTPUT	High
CS3	A18	EMI2	DDR	OUTPUT	High
CS4	E5	EMI1	GPIO	OUTPUT	High
CS5	D2	EMI1	GPIO	OUTPUT	High
NF_CE0	F4	NFC	GPIO	OUTPUT	High
ECB	B1	EMI1	GPIO	INPUT	100 KΩ Pull-Up
LBA	B3	EMI1	DDR	OUTPUT	High
BCLK	A8	EMI1	DDR	OUTPUT	Low
RW	D5	EMI1	DDR	OUTPUT	High
NFWE_B	E1	NFC	GPIO	OUTPUT	High
NFRE_B	C1	NFC	GPIO	OUTPUT	High
NFALE	E2	NFC	GPIO	OUTPUT	Low
NFCLE	D1	NFC	GPIO	OUTPUT	Low
NFWP_B	G4	NFC	GPIO	OUTPUT	High
NFRB	G5	NFC	GPIO	INPUT	100 KΩ Pull-Up
D15	K2	NFC	GPIO	INPUT	Keeper
D14	K4	NFC	GPIO	INPUT	Keeper
D13	J2	NFC	GPIO	INPUT	Keeper
D12	J4	NFC	GPIO	INPUT	Keeper
D11	K5	NFC	GPIO	INPUT	-
D10	H4	NFC	GPIO	INPUT	Keeper
D9	H5	NFC	GPIO	INPUT	Keeper
D8	G2	NFC	GPIO	INPUT	Keeper

Table 107. i.MX25 12×12 Package Ball Map (continued)

	AB	AA	Y	W	V	U	T	R	
1	QGND	CSPI1_MOSI	CSPI1_SCLK	UART1_RTS	UART2_RXD	KPP_ROW2	KPP_COL0	FEC_TX_EN	1
2	LSCLK	QGND	CONTRAST	QGND	CSPI1_SS0	UART1_RXD	UART2_RTS	KPP_ROW0	2
3	LD14	OE_ACD							3
4	LD12	HSYNC		PWM	CSPI1_MISO	CSPI1_SS1	UART2_TXD	KPP_ROW1	4
5	LD10	LD15		VSYNC		CSPI1_RDY	QGND	UART1_CTS	5
6	LD8	LD9		LD13	UART1_TXD		QGND		6
7	LD6	LD7		LD11			NVCC_MISC	NVCC_MISC	7
8	LD4	LD5		LD1			NVCC_LCDC	NVCC_LCDC	8
9	LD2	LD3		QGND			QVDD	NVCC_LCDC	9
10	LD0	BAT_VDD		NVCC_JTAG	QVDD		QVDD	QVDD	10
11	SJC_MOD	TDO		DE_B	TAMPER_A		QGND	QGND	11
12	OSC32K_XTAL	TMS		TDI			QGND	QGND	12
13	OSC32K_EXTAL	TCK		RTCK	TAMPER_B		MESH_C	MESH_D	13
14	TRSTB	REF		INAUX1				NVCC_DRYICE	14
15	OSC_BYP	INAUX0		YN	OSC24M_VDD		OSC24M_GND	QVDD	15
16	INAUX2	XN		USBPHY2_VSS			USBPHY2_VDD	QVDD	16
17	YP	WIPER		USBPHY2_DP	MPLL_GND				17
18	QGND	XP		USBPHY2_DM	QGND		QGND	QGND	18
19	OSC24M_EXTAL	TEST_MODE		MPLL_VDD	QGND	RESET_B	POWER_FAIL	GPIO_F	19
20	OSC24M_XTAL	CLK_SEL							20
21	QGND	QGND	QGND	BOOT_MODE1	POR_B	UPLL_BYPCLK	VSTBY_REQ	GPIO_E	21
22	QGND	BOOT_MODE0	CLKO	VSTBY_ACK	EXT_ARMCLK	GPIO_C	GPIO_A	SD1_DATA1	22

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