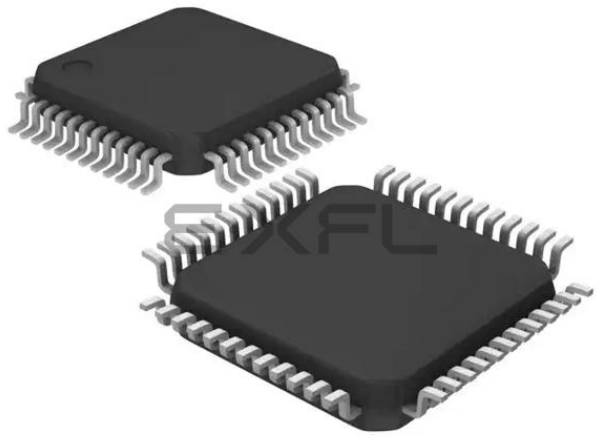

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Details	
Product Status	Not For New Designs
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SCI, SPI
Peripherals	LCD, LVD, PWM
Number of I/O	39
Program Memory Size	18KB (18K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.9K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08lg16clf

Freescale Semiconductor, Inc.
Data Sheet Addendum

Document Number: MC9S08LG32AD
Rev. 0, 04/2015

Addendum to Rev. 9 of the MC9S08LG32 Series Covers: MC9S08LG32 and MC9S08LG16

This addendum identifies changes to Rev. 9 of the MC9S08LG32 Series data sheet (covering MC9S08LG32 and MC9S08LG16). The changes described in this addendum have not been implemented in the specified pages.

1 Add min values for I_{IC} (DC injection current)

Location:	Table 8. DC Characteristics, Page 14

In Table 8, “DC Characteristics,” add min values for I_{IC} (row number 14) as follows:

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
14	D	DC injection current [5, 6, 7] $V_{IN} < V_{SS}$ (min) $V_{IN} > V_{DD}$ (max)	Single pin limit	I_{IC}	**-0.2**	—	2	mA
			Total MCU limit, includes sum of all stressed pins		**-5**	—	25	mA

2 Change the max value of t_{LPO} (low power oscillator period)

Location:	Table 14. Control Timing, Page 29

In Table 14, “Control Timing,” change the max value of t_{LPO} (row number 2) from 1300 to 1500 µs.

Freescale Semiconductor
Data Sheet: Technical Data

Document Number: MC9S08LG32
Rev. 9 , 09/2011

MC9S08LG32 Series
Covers: MC9S08LG32 and MC9S08LG16

MC9S08LG32


80-LQFP
Case 917A
14 mm × 14 mm


64-LQFP
Case 840F
10 mm × 10 mm


48-LQFP
Case 932
7 mm × 7mm

Features

- 8-bit HCS08 Central Processor Unit (CPU)
  - Up to 40 MHz CPU at 5.5 V to 2.7 V across temperature range of –40 °C to 85 °C and –40 °C to 105 °C
  - HCS08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - 32 KB or 18 KB dual array flash; read/program/erase over full operating voltage and temperature
  - 1984 byte random access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
  - Two low-power stop modes (stop2 and stop3)
  - Reduced-power wait mode
  - Peripheral clock gating register can disable clocks to unused modules, thereby reducing currents
  - Low power On-Chip crystal oscillator (XOSC) that can be used in low-power modes to provide accurate clock source to real time counter and LCD controller
  - 100 µs typical wakeup time from stop3 mode
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports bus frequencies from 1 MHz to 20 MHz.
- System Protection
  - COP reset with option to run from dedicated 1 kHz internal clock or bus clock
  - Low-voltage warning with interrupt
  - Low-voltage detection with reset
  - Illegal opcode detection with reset
  - Illegal address detection with reset
  - Flash and RAM protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging and plus two more breakpoints in On-Chip debug module
  - On-Chip in-circuit emulator (ICE) debug module containing three comparators and nine trigger modes; eight deep FIFO for storing change-of-flow addresses and event-only data; debug module supports both tag and force breakpoints
- Peripherals
  - **LCD** — Up to 4 × 41 or 8 × 37 LCD driver with internal charge pump.
  - **ADC** — Up to 16-channel, 12-bit resolution, 2.5 µs conversion time, automatic compare function, temperature sensor, internal bandgap reference channel, runs in stop3 and can wake up the system, fully functional from 5.5 V to 2.7 V
  - **SCI** — Full duplex non-return to zero (NRZ), LIN master extended break generation, LIN slave extended break detection, wakeup on active edge
  - **SPI** — Full-duplex or single-wire bidirectional, double-buffered transmit and receive, master or slave mode, MSB-first or LSB-first shifting
  - **IIC** — With up to 100 kbps with maximum bus loading, multi-master operation, programmable slave address, interrupt driven byte-by-byte data transfer, supports broadcast mode and 10-bit addressing
  - **TPMx** — One 6 channel and one 2 channel, selectable input capture, output compare, or buffered edge or center-aligned PWM on each channel
  - **MTIM** — 8-bit counter with match register,, four clock sources with prescaler dividers, can be used for periodic wakeup
  - **RTC** — 8-bit modulus counter with binary or decimal based prescaler, three clock sources including one external source, can be used for time base, calendar, or task scheduling functions
  - **KBI** — One keyboard control module capable of supporting 8 × 8 keyboard matrix
  - **IRQ** — External pin for wakeup from low-power modes
- Input/Output
  - 39, 53, or 69 GPIOs
  - 8 KBI and 1 IRQ interrupt with selectable polarity
  - Hysteresis and configurable pullup device on all input pins, configurable slew rate and drive strength on all output pins.
- Package Options
  - 48-pin LQFP, 64-pin LQFP, and 80-pin LQFP

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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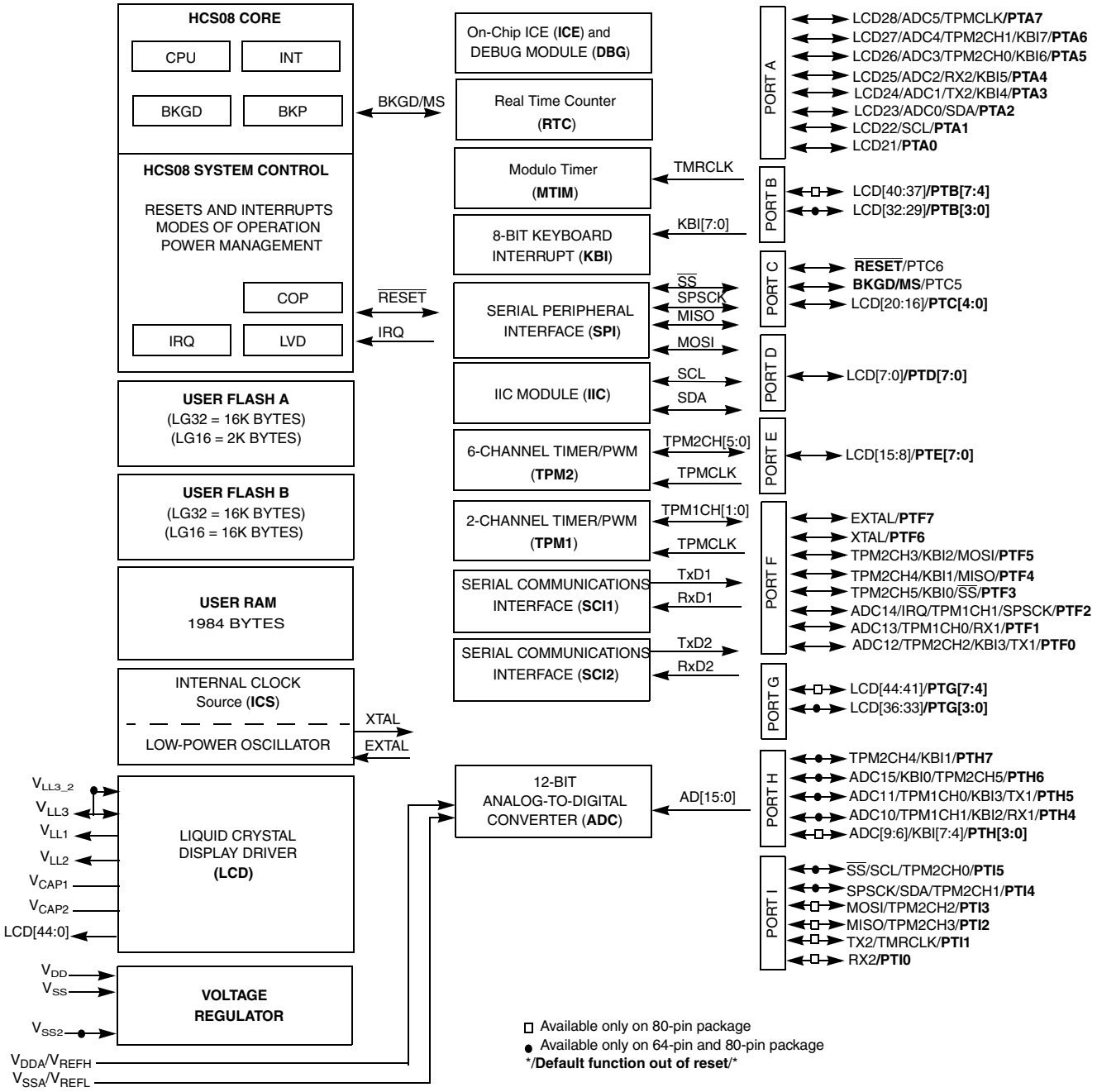


Figure 1. MC9S08LG32 Series Block Diagram

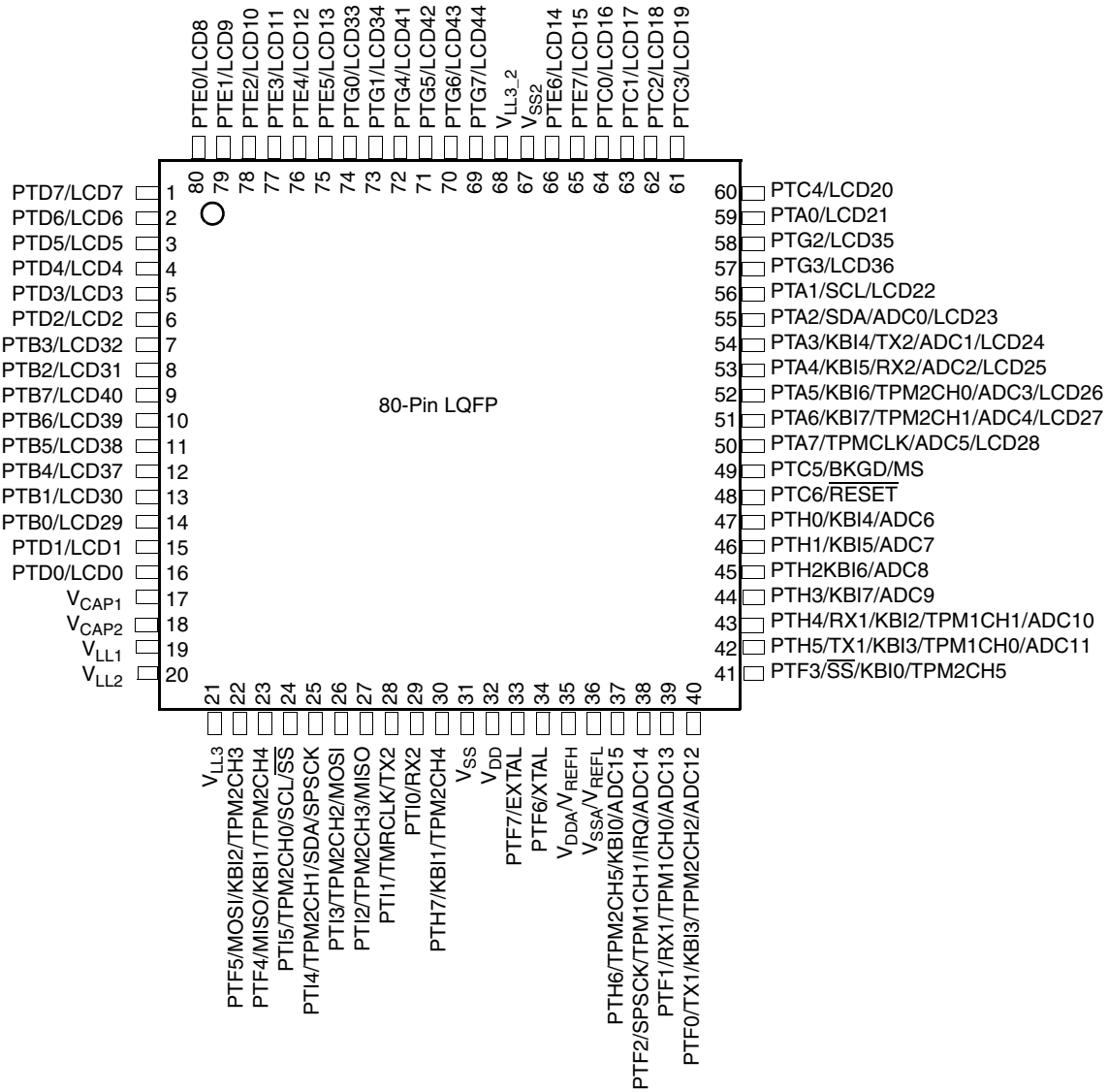


Figure 2. 80-Pin LQFP

NOTE

V_{REFH}/V_{REFL} are internally connected to V_{DDA}/V_{SSA}.

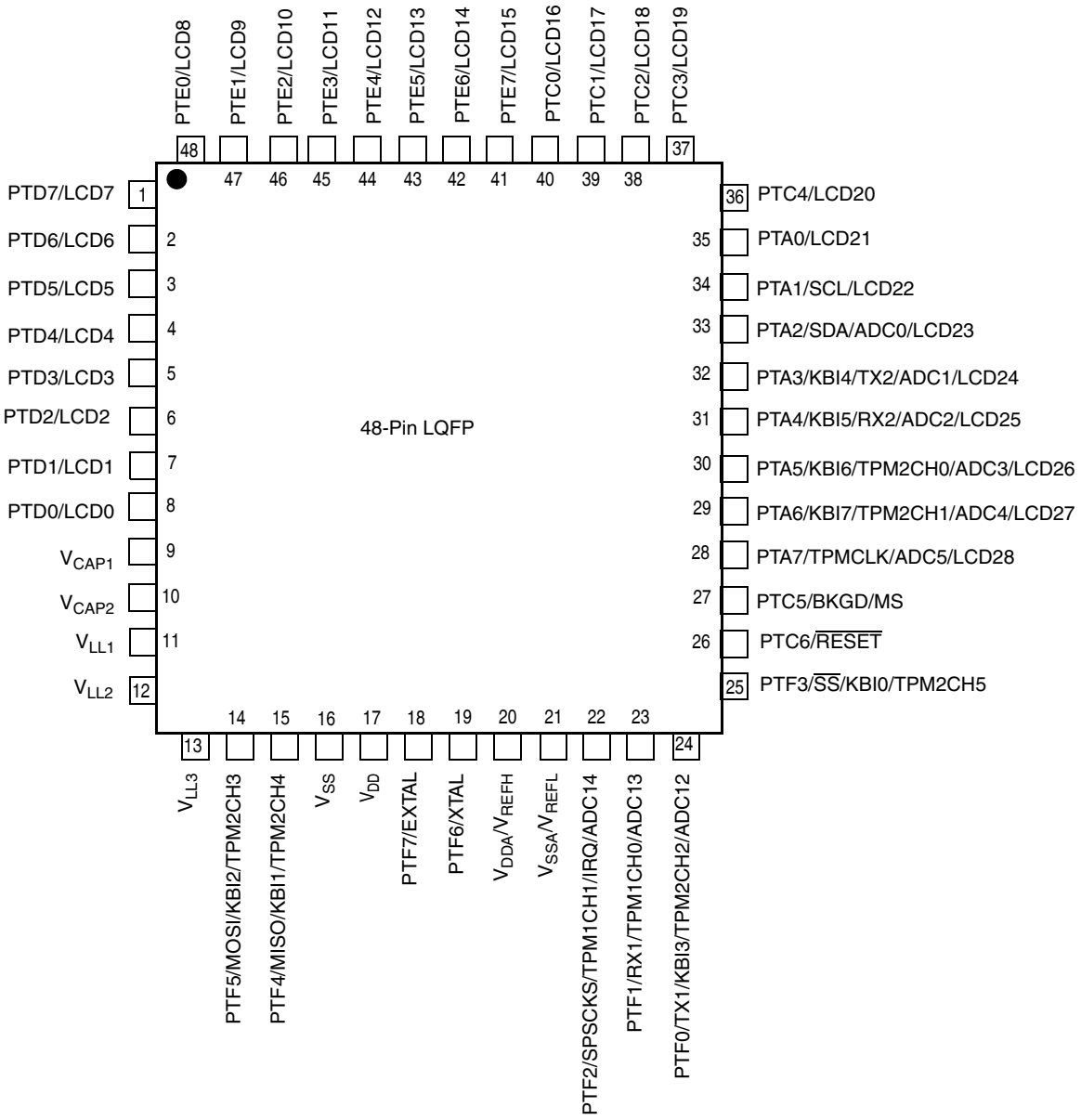


Figure 4. 48-Pin LQFP

NOTE

V_{REFH}/V_{REFL} are internally connected to V_{DDA}/V_{SSA}.

Table 2. Pin Availability by Package Pin-Count (continued)

Packages			<-- Lowest **Priority** --> Highest				
80	**64**	**48**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
39	31	23	PTF1	RX1	TPM1CH0	ADC13	—
40	32	24	PTF0	TX1	KBI3	TPM2CH2	ADC12
41	33	25	PTF3	$\overline{SS}$	KBI0	TPM2CH5	—
42	34	—	PTH5	TX1	KBI3	TPM1CH0	ADC11
43	35	—	PTH4	RX1	KBI2	TPM1CH1	ADC10
44	—	—	PTH3	KBI7	ADC9	—	—
45	—	—	PTH2	KBI6	ADC8	—	—
46	—	—	PTH1	KBI5	ADC7	—	—
47	—	—	PTH0	KBI4	ADC6	—	—
48	36	26	PTC6	$\overline{RESET}$	—	—	—
49	37	27	PTC5	BKGD/MS	—	—	—
50	38	28	PTA7	TPMCLK	ADC5	LCD28	—
51	39	29	PTA6	KBI7	TPM2CH1	ADC4	LCD27
52	40	30	PTA5	KBI6	TPM2CH0	ADC3	LCD26
53	41	31	PTA4	KBI5	RX2	ADC2	LCD25
54	42	32	PTA3	KBI4	TX2	ADC1	LCD24
55	43	33	PTA2	SDA	ADC0	LCD23	—
56	44	34	PTA1	SCL	LCD22	—	—
57	45	—	PTG3	LCD36	—	—	—
58	46	—	PTG2	LCD35	—	—	—
59	47	35	PTA0	LCD21	—	—	—
60	48	36	PTC4	LCD20	—	—	—
61	49	37	PTC3	LCD19	—	—	—
62	50	38	PTC2	LCD18	—	—	—
63	51	39	PTC1	LCD17	—	—	—
64	52	40	PTC0	LCD16	—	—	—
65	53	41	PTE7	LCD15	—	—	—
66	54	42	PTE6	LCD14	—	—	—
67	55	—	V_{SS2}	—	—	—	—
68	56	—	V_{LL3_2}	—	—	—	—
69	—	—	PTG7	LCD44	—	—	—
70	—	—	PTG6	LCD43	—	—	—
71	—	—	PTG5	LCD42	—	—	—
72	—	—	PTG4	LCD41	—	—	—
73	57	—	PTG1	LCD34	—	—	—
74	58	—	PTG0	LCD33	—	—	—
75	59	43	PTE5	LCD13	—	—	—
76	60	44	PTE4	LCD12	—	—	—

Table 8. DC Characteristics (continued)

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
14	D	DC injection current [5, 6, 7] $V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	Single pin limit	I_{IC}	—	—	2	mA
			Total MCU limit, includes sum of all stressed pins		—	—	25	mA
15	C	Input Capacitance, all non-supply pins		C_{In}	—	—	8	pF
16	C	RAM retention voltage		V_{RAM}	2	—	—	V
17	P	POR rearm voltage		V_{POR}	0.9	1.4	2.0	V
18	D	POR rearm time		t_{POR}	10	—	—	µs
19	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising		V_{LVD1}	 3.9 4.0	 4.0 4.1	 4.1 4.2	V
20	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising		V_{LVD0}	 2.48 2.54	 2.56 2.62	 2.64 2.70	V
21	P	Low-voltage warning threshold — high range 1 V_{DD} falling V_{DD} rising		V_{LVW3}	 4.5 4.6	 4.6 4.7	 4.7 4.8	V
22	P	Low-voltage warning threshold — high range 0 V_{DD} falling V_{DD} rising		V_{LVW2}	 4.2 4.3	 4.3 4.4	 4.4 4.5	V
23	P	Low-voltage warning threshold — low range 1 V_{DD} falling V_{DD} rising		V_{LVW1}	 2.84 2.90	 2.92 2.98	 3.00 3.06	V
24	P	Low-voltage warning threshold — low range 0 V_{DD} falling V_{DD} rising		V_{LVW0}	 2.66 2.72	 2.74 2.80	 2.82 2.88	V
25	P	Low-voltage inhibit reset/recover hysteresis 5 V 3 V		V_{hys}	—	 100 60	—	mV

1 Typical values are measured at 25 °C. Characterized, not tested

2 Measured with $V_{In} = V_{DD}$ or V_{SS}.

3 Measured with $V_{In} = V_{SS}$.

4 Measured with $V_{In} = V_{DD}$.

5 All functional non-supply pins, except for PTC6 are internally clamped to V_{SS} and V_{DD}.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. For instance, if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

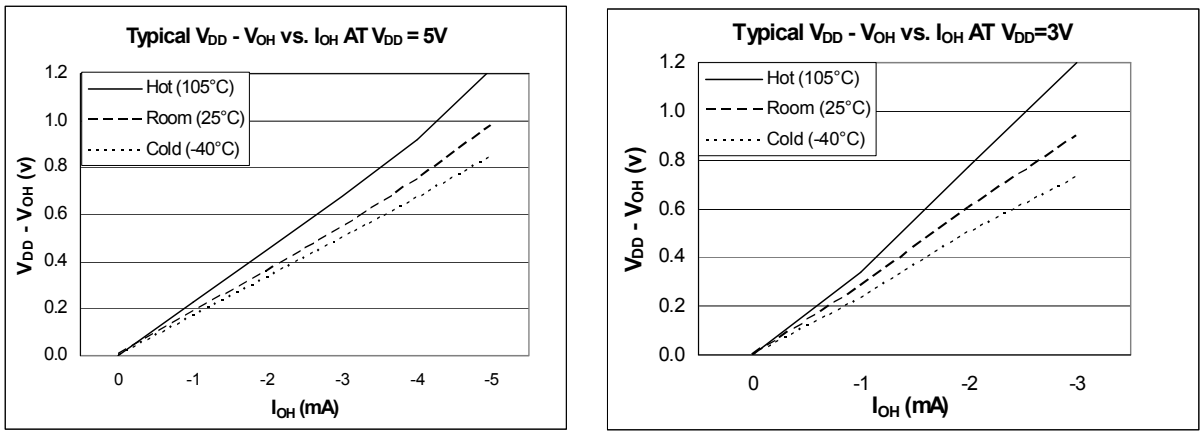


Figure 8. Typical High-side Drive (source) characteristics – Low Drive (PTxDSn = 0)

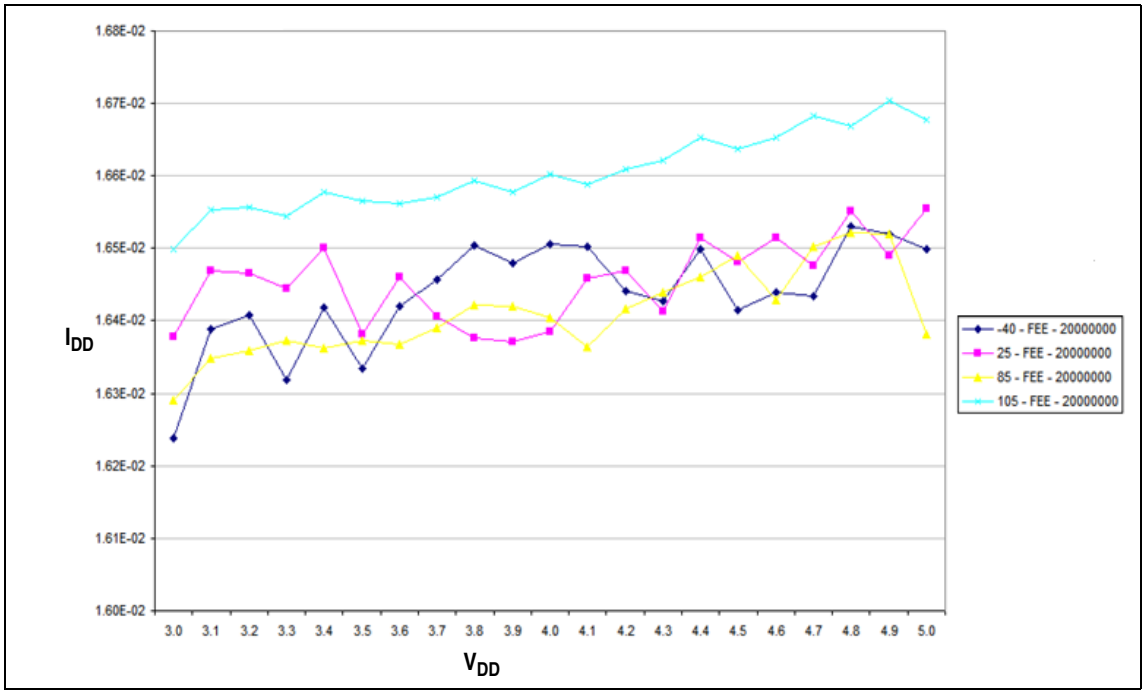


Figure 12. Typical Run I_{DD} for FEE Mode at 20 MHz

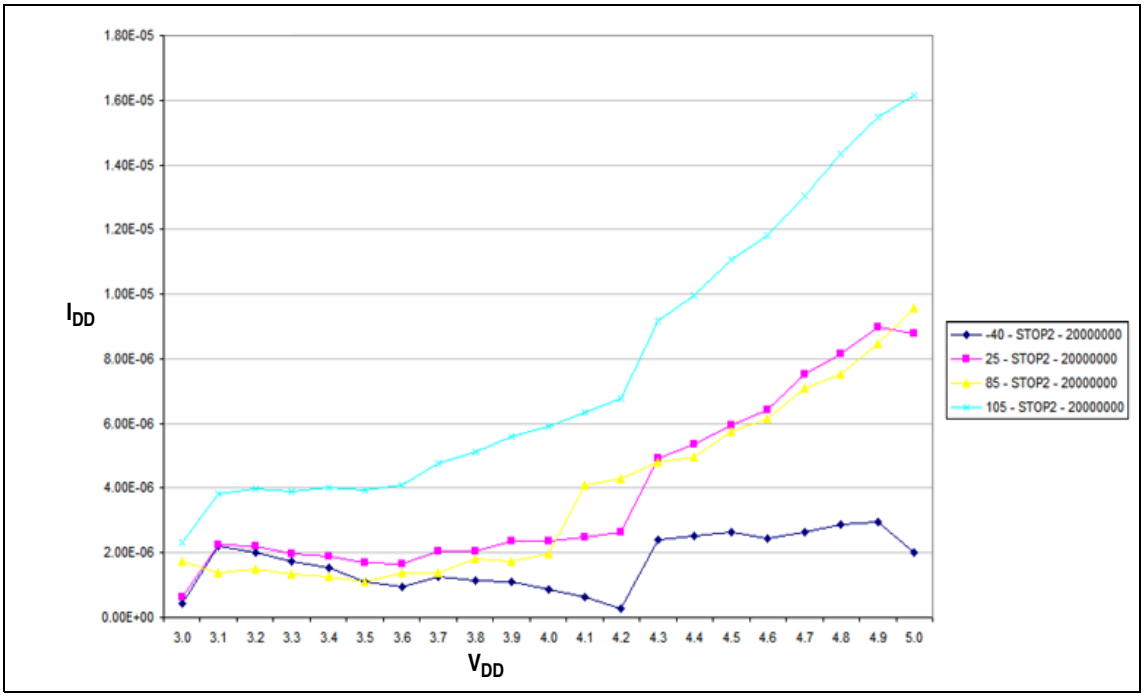


Figure 13. Typical Stop2 I_{DD}

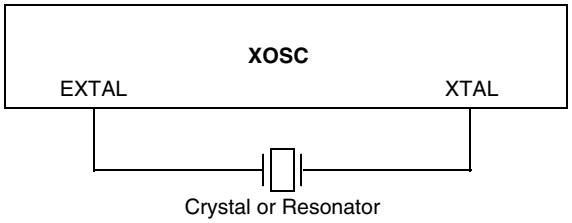


Figure 16. Typical Crystal or Resonator Circuit: Low Range/Low Power

2.9 Internal Clock Source (ICS) Characteristics

Table 11. ICS Frequency Specifications (Temperature Range = –40 °C to 105 °C Ambient)

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
1	P	Average internal reference frequency — factory trimmed at VDD = 5.0 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	C	Average internal reference frequency — user trimmed		f_{int_t}	31.25	—	39.0625	kHz
3	C	Internal reference start-up time		t_{IRST}	—	60	100	µs
4	P	DCO output frequency range — trimmed[2]	Low range (DRS = 00)	f_{dco_t}	16	—	20	MHz
	P		Mid range (DRS = 01)		32	—	40	
5	P	DCO output frequency[2] Reference = 32768 Hz and DMX32 = 1	Low range (DRS = 00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DRS = 01)		—	39.85	—	
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)[3]		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)[3]		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	P	Total deviation of trimmed DCO output frequency over voltage and temperature		Δf_{dco_t}	—	–1.0 to +0.5	±2	$\%f_{dco}$
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 °C to 70 °C[3]		Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	C	FLL acquisition time[3, 4]		$t_{Acquire}$	—	—	1	mS
11	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[5]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This parameter is characterized and not tested on each device.

4 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

5 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in the crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

Table 12. 12-bit ADC Operating Conditions (continued)

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Input Resistance	—	R_{ADIN}	—	5	7	kΩ	—
Analog Source Resistance	12-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
	10-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz		 — —	 — —	 5 10		
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC Conversion Clock Freq.	High Speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low Power (ADLPC = 1)		0.4	—	4.0		

1 Typical values assume V_{DDAD} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

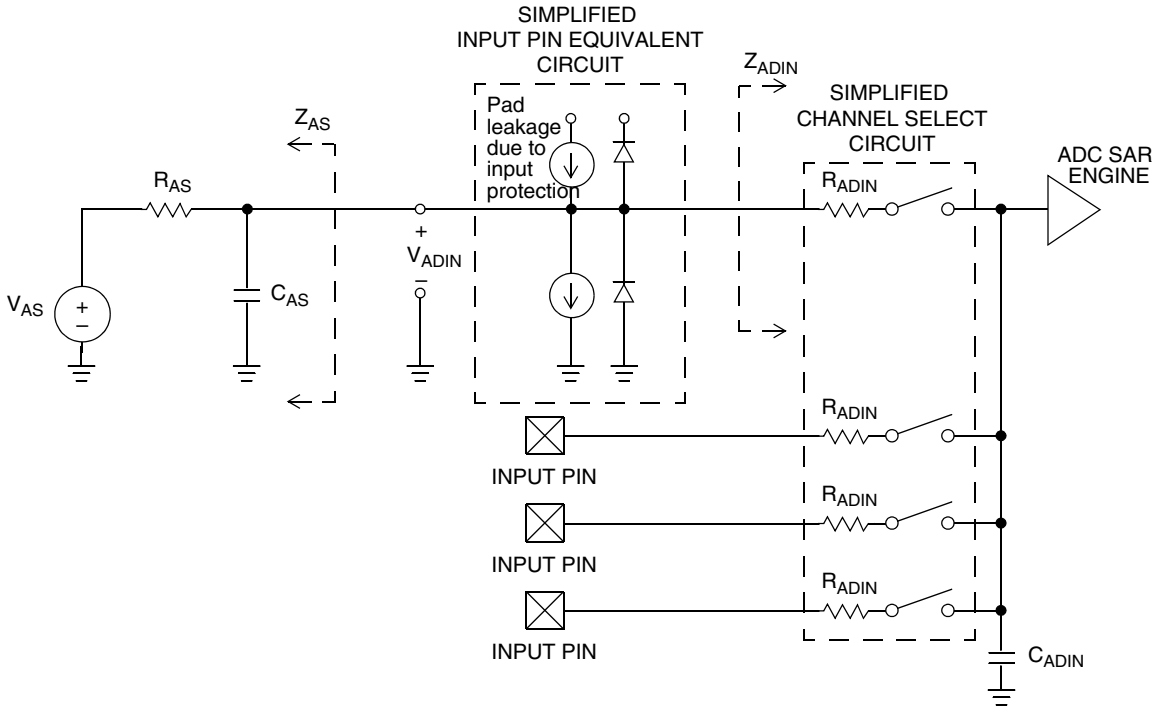


Figure 18. ADC Input Impedance Equivalency Diagram

Table 13. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

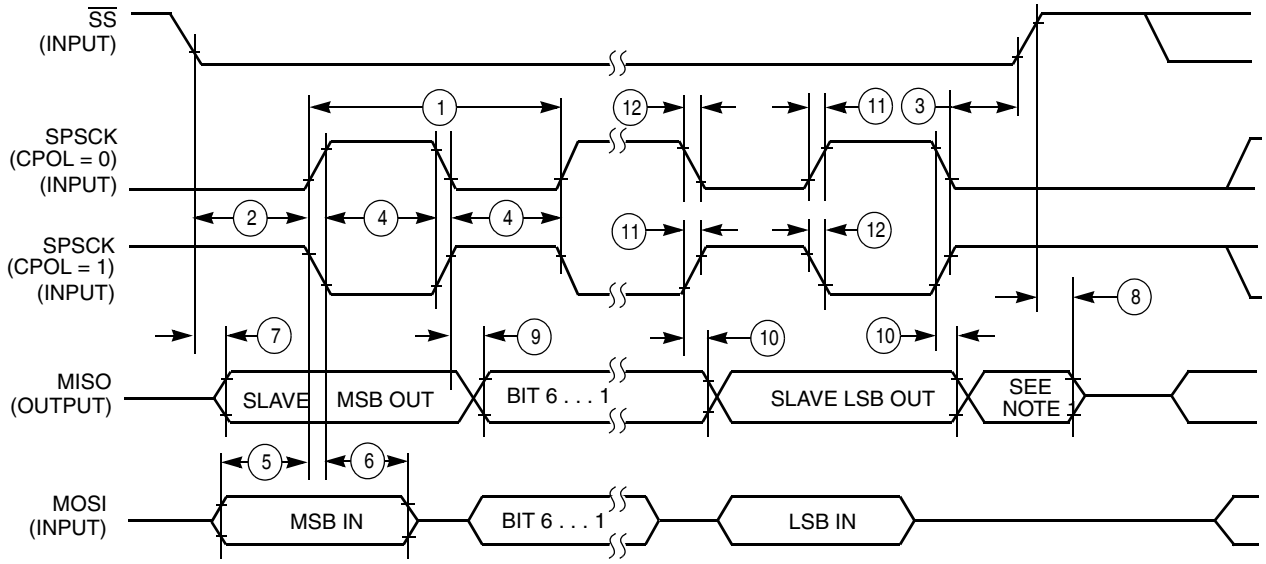
Num	C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
13	T	Full-Scale Error	12-bit mode	E_{FS}	—	±1	—	LSB[2]	V_{ADIN} = V_{DDAD}
	P		10-bit mode		—	±0.5	±1		
	T		8-bit mode		—	±0.5	±0.5		
14	D	Quantization Error	12-bit mode	E_Q	—	–1 to 0	—	LSB[2]	—
			10-bit mode		—	—	±0.5		
			8-bit mode		—	—	±0.5		
15	D	Input Leakage Error	12-bit mode	E_{IL}	—	±1	—	LSB[2]	Pad leakage[4] * R_{AS}
			10-bit mode		—	±0.2	±2.5		
			8-bit mode		—	±0.1	±1		
16	C	Temp Sensor Slope	–40 °C to 25 °C	m	—	1.646	—	mV/°C	—
			25 °C to 125°C		—	1.769	—		
17	C	Temp Sensor Voltage	25 °C	V_{TEMP25}	—	701.2	—	mV	—

1 Typical values assume V_{DDAD} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

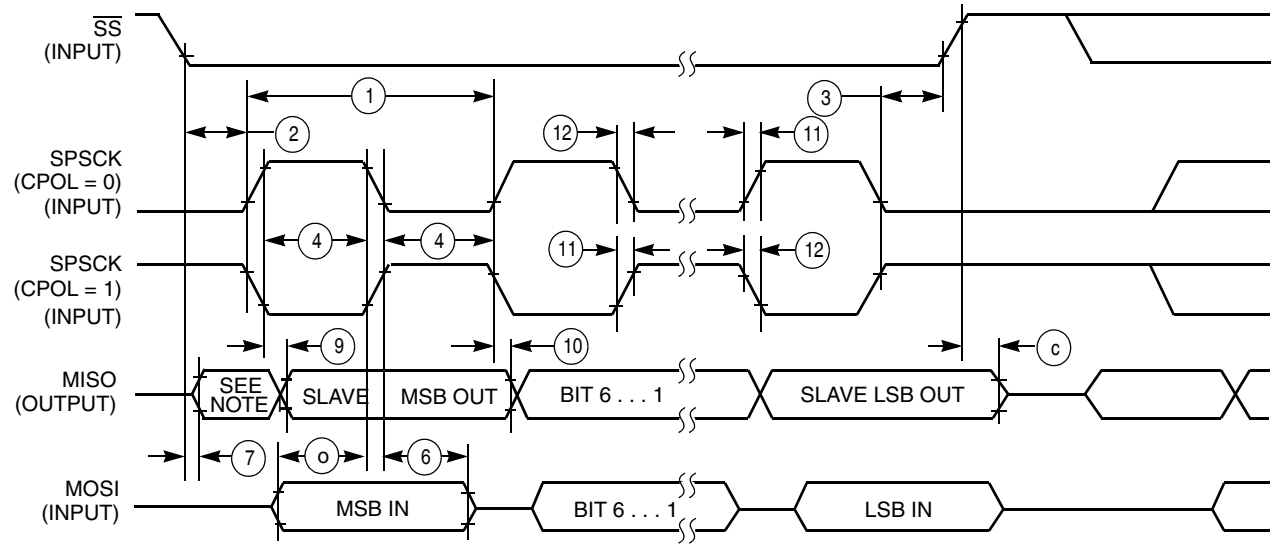
3 Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes

4 Based on input pad leakage current. Refer to pad electricals.



NOTE:
1. Not defined but normally MSB of character just received.

Figure 25. SPI Slave Timing (CPHA = 0)



NOTE:
1. Not defined but normally LSB of character just received

Figure 26. SPI Slave Timing (CPHA = 1)

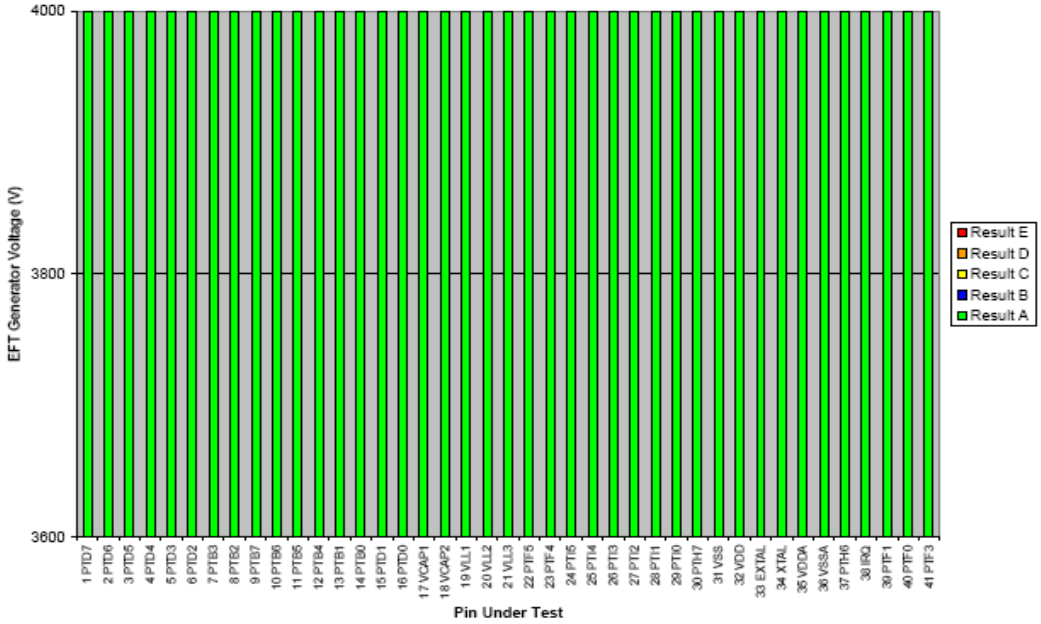
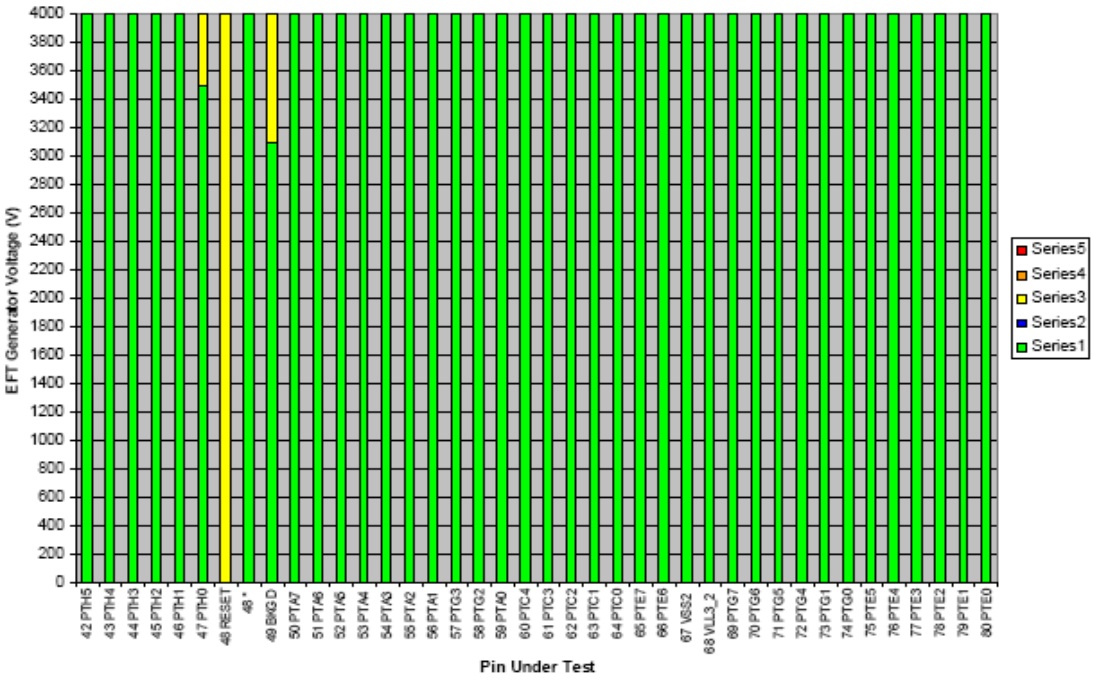


Figure 29. 4 MHz, Negative Polarity Pins 1 – 41



Note:
RESET retested with 0.1 μF capacitor from pin to ground is Class A compliant as shown by 48*.

Figure 30. 4 MHz, Negative Polarity Pins 42 – 80

3.1 Device Numbering System

Example of the device numbering system:

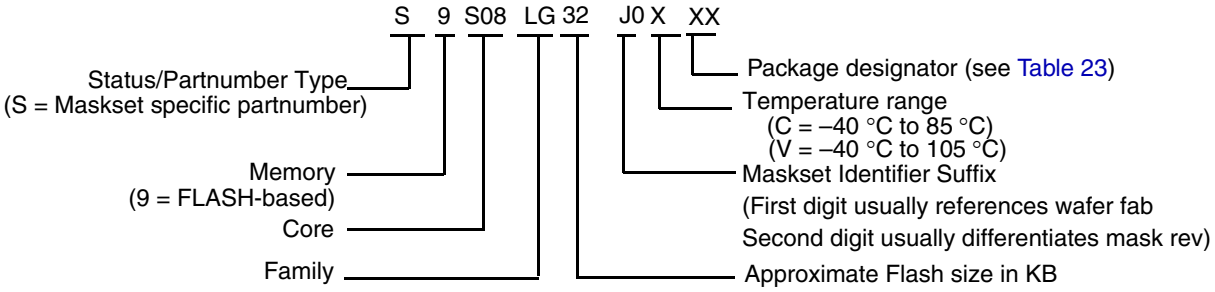


Figure 31. Device Number Example for Auto Parts

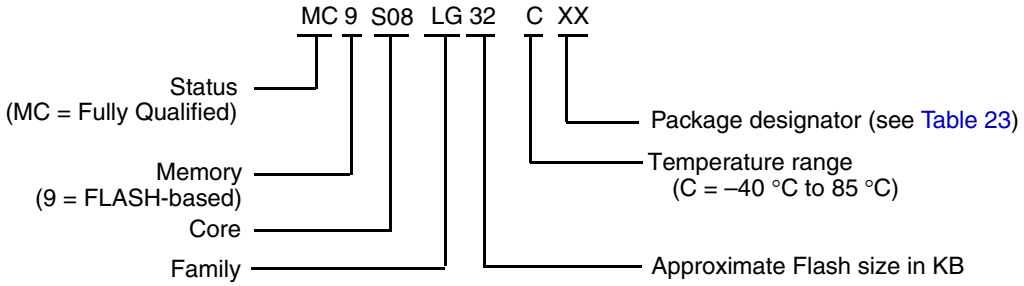


Figure 32. Device Number Example for IMM Parts

4 Package Information

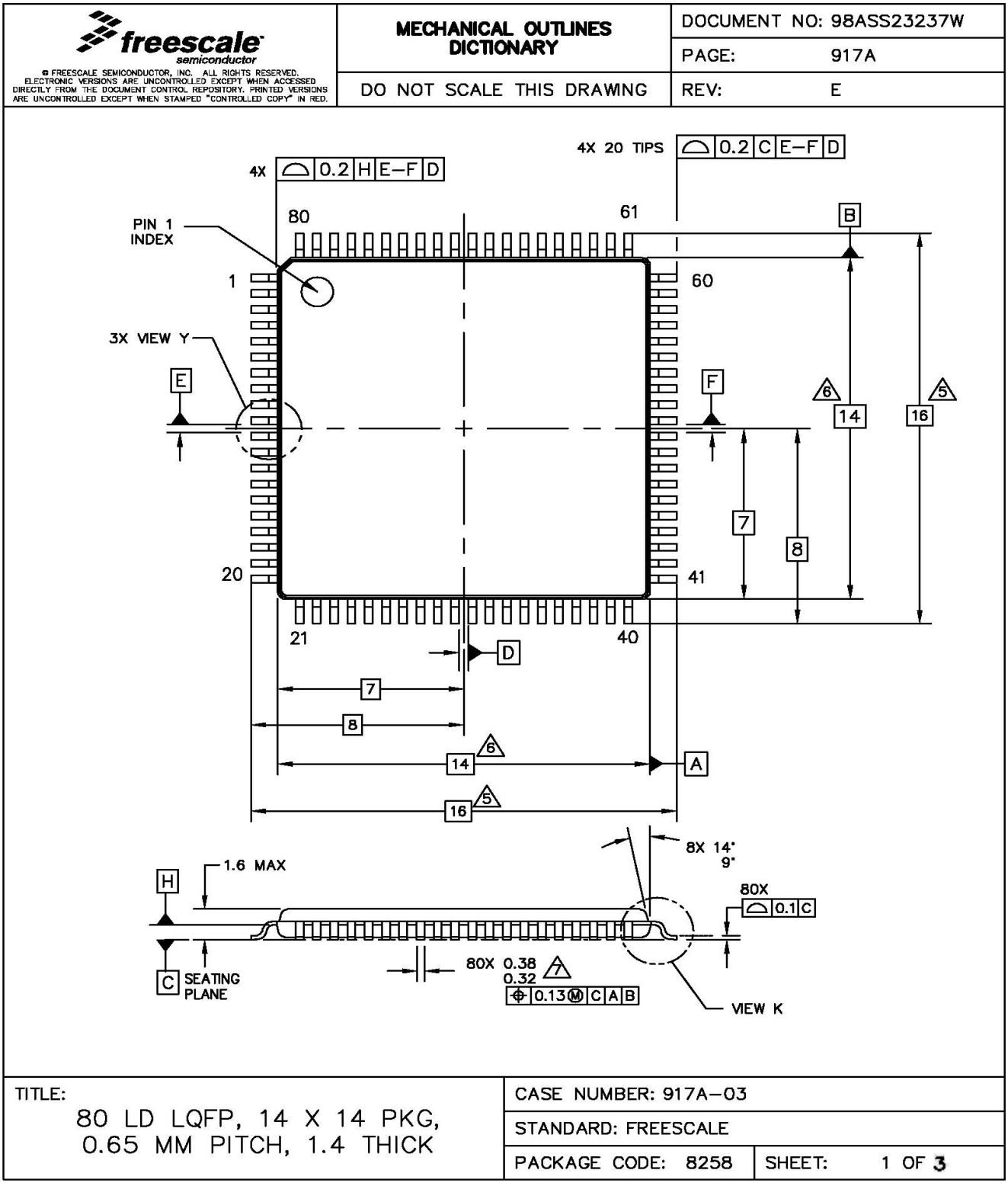
Table 23. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
80	Low Quad Flat Package	LQFP	LK	917A	98ASS23237W
64	Low Quad Flat Package	LQFP	LH	840F	98ASS23234W
48	Low Quad Flat Package	LQFP	LF	932	98ASH00962A

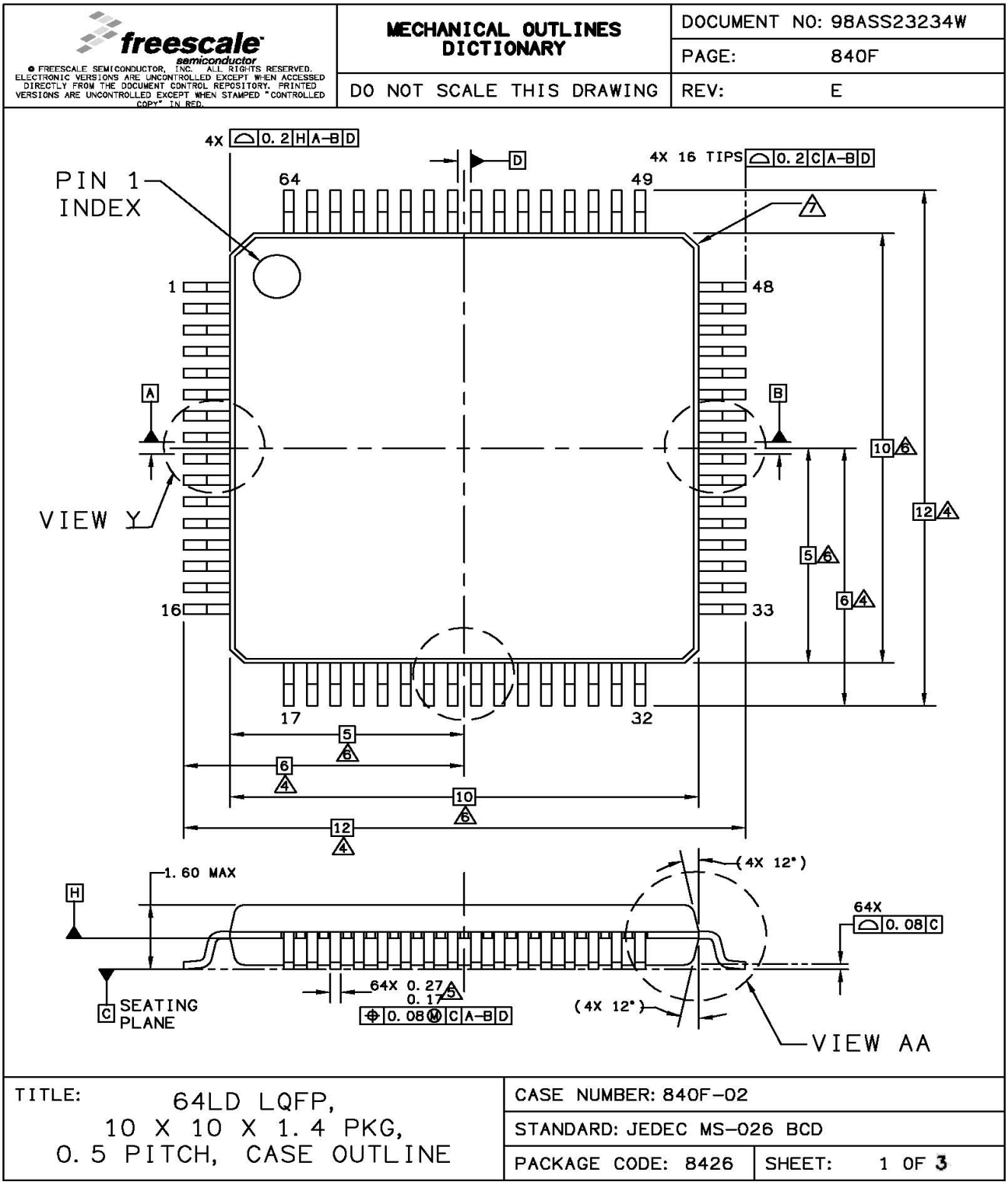
4.1 Mechanical Drawings

The following pages are mechanical drawings for the packages described in Table 23. For the latest available drawings please visit our web site (http://www.freescale.com) and enter the package's document number into the keyword search box.

4.1.1 80-pin LQFP



4.1.2 64-pin LQFP



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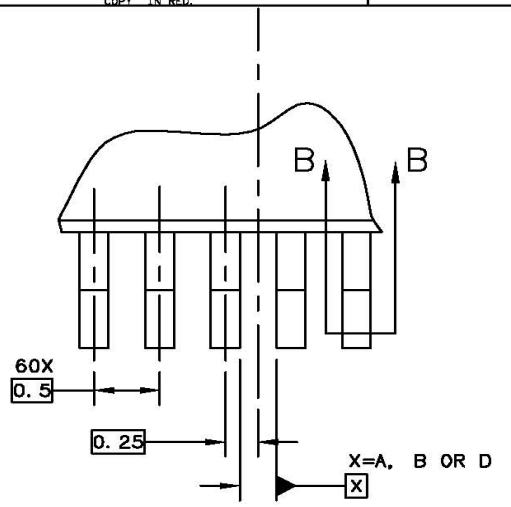
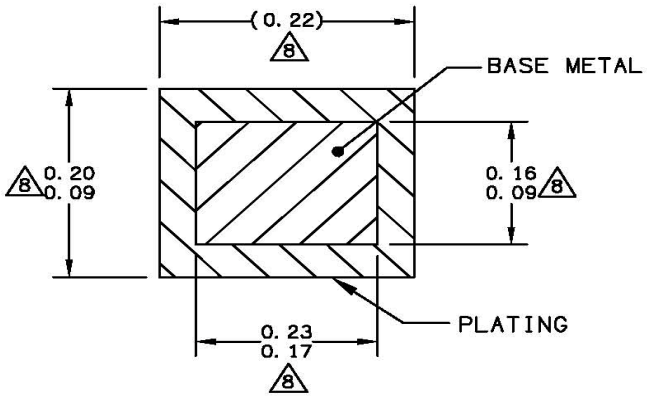
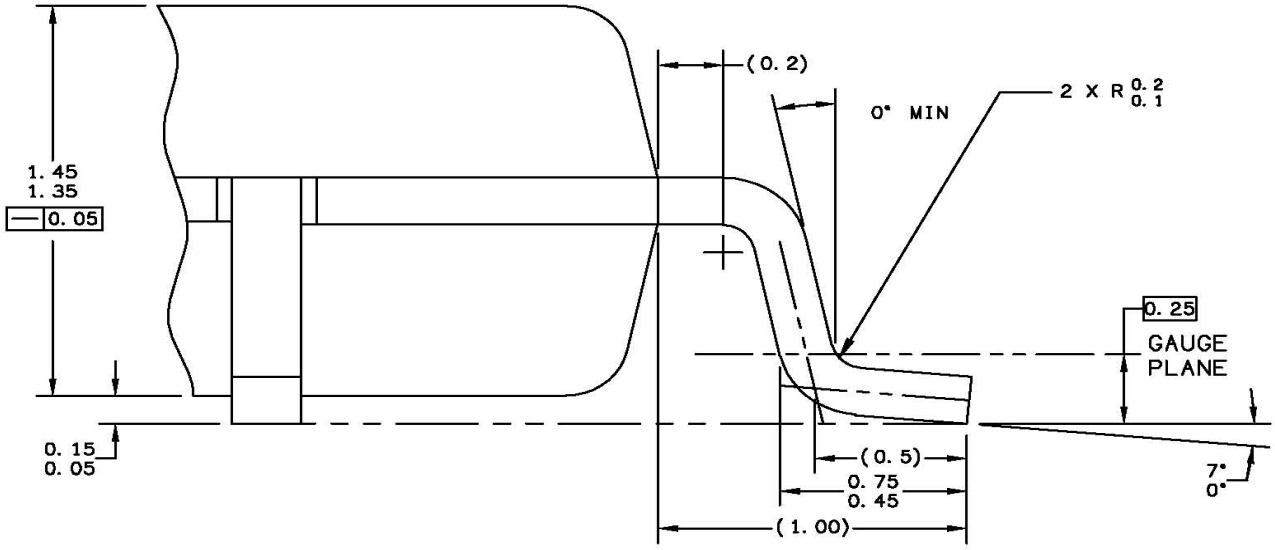
	PAGE: 840F
DO NOT SCALE THIS DRAWING	REV: E



VIEW Y



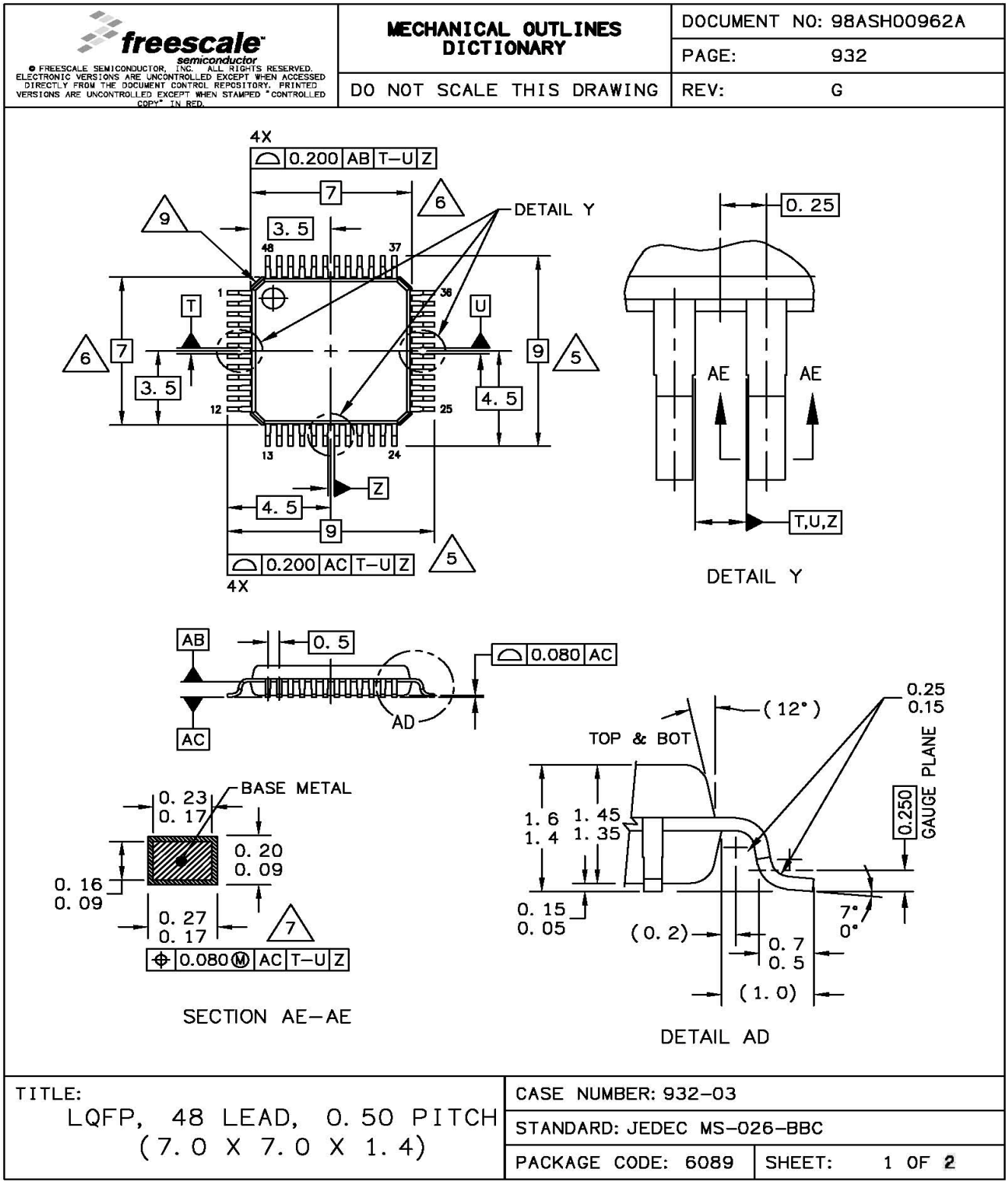
SECTION B–B



VIEW AA

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F–02	
	STANDARD: JEDEC MS–026 BCD	
	PACKAGE CODE: 8426	SHEET: 2 OF 3

4.1.3 48-pin LQFP



5 Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web are the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://www.freescale.com

The following revision history table summarizes changes contained in this document.

Table 24. Revision History

Revision	Date	Description of Changes
1	8/2008	First Initial release.
2	9/2008	Second Initial Release.
3	11/2008	Alpha Customer Release.
4	2/2009	Launch Release.
5	4/2009	Added EMC Radiated Emission and Transient Susceptibility data in Table 19 and Table 20.
6	4/2009	Updated EMC performance data.
7	8/2009	Updated auto part numbers, changed TCLK, T0CH0, T0CH1, T1CH0, T1CH1, T1CH2, T1CH3, T1CH3, T1CH4, and T1CH5 to TPMCLK, TPM0CH0, TPM0CH1,TPM1CH0, TPM1CH1, TPM1CH2, TPM1CH3, TPM1CH4, and TPM1CH5, and changed the maximum LCD frame frequency to 64 Hz.
8	8/2011	Updated Table “ICS Frequency Specifications (Temperature Range = –40 ×C to 105 ×C Ambient)”. Changed the value of row 8 column C from C to P.
9	9/2011	Updated Table “ICS Frequency Specifications (Temperature Range = –40 ×C to 105 ×C Ambient)”. Removed Footnote from Row 8. Updated the Revision History