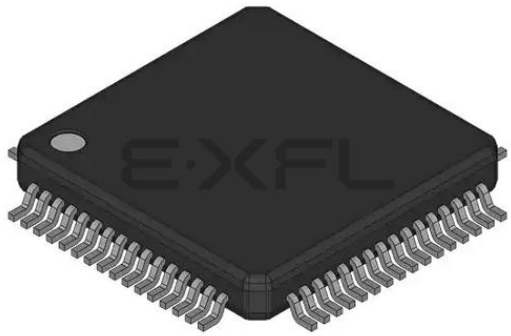

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | S08 |
| Core Size | 8-Bit |
| Speed | 40MHz |
| Connectivity | I²C, SCI, SPI |
| Peripherals | LCD, LVD, PWM |
| Number of I/O | 53 |
| Program Memory Size | 18KB (18K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1.9K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 12x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08lg16clh |

**Table 1. MC9S08LG32 Series Features by MCU and Package**

| Feature | MC9S08LG32 | | | MC9S08LG16 | |
|---|---|---|---|---|---|
| Flash size (bytes) | 32,768 | | | 18,432 | |
| RAM size (bytes) | 1984 | | | | |
| Pin quantity | 80 | 64 | 48 | 64 | 48 |
| ADC | 16 ch | 12 ch | 9 ch | 12 ch | 9 ch |
| LCD | 8 x 37<br>4 x 41 | 8 x 29<br>4 x 33 | 8 x 21<br>4 x 25 | 8 x 29<br>4 x 33 | 8 x 21<br>4 x 25 |
| ICE + DBG | yes | | | | |
| ICS | yes | | | | |
| IIC | yes | | | | |
| IRQ | yes | | | | |
| KBI | 8 pin | | | | |
| GPIOs | 69 | 53 | 39 | 53 | 39 |
| RTC | yes | | | | |
| MTIM | yes | | | | |
| SCI1 | yes | | | | |
| SCI2 | yes | | | | |
| SPI | yes | | | | |
| TPM1 channels | 2 | | | | |
| TPM2 channels | 6 | | | | |
| XOSC | yes | | | | |

# 1 Pin Assignments

This section shows the pin assignments for the MC9S08LG32 series devices. The priority of functions on a pin is in ascending order from left to right and bottom to top. Another view of pinouts and function priority is given in Table 2.

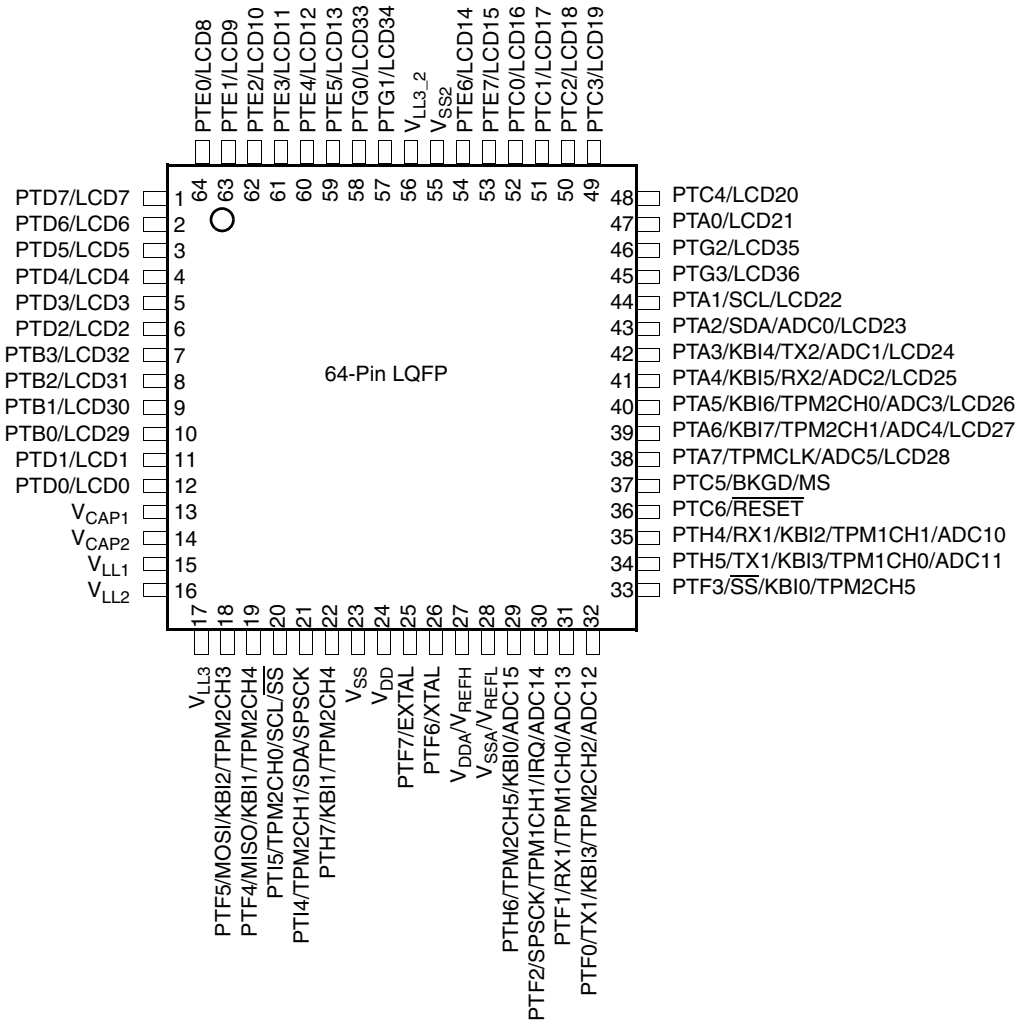



**Figure 3. 64-Pin LQFP**

## NOTE

$V_{REFH}/V_{REFL}$ are internally connected to $V_{DDA}/V_{SSA}$.

**Table 7. ESD and Latch-Up Protection Characteristics**

| No. | Rating[1] | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | Human body model (HBM) | $V_{HBM}$ | 2500 | — | V |
| 2 | Charge device model (CDM) | $V_{CDM}$ | 750 | — | V |
| 3 | Latch-up current at $T_A$ = 85 °C | $I_{LAT}$ | ±100 | — | mA |

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

## 2.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

**Table 8. DC Characteristics**

| Num | C | Characteristic | Symbol | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | — | Operating Voltage | — | 2.7 | — | 5.5 | V |
| 2 | P | Output high voltage — Low Drive (PTxDSn = 0)<br>5 V, $I_{Load}$ = –2 mA<br>3 V, $I_{Load}$ = –0.6 mA | $V_{OH}$ | <br>$V_{DD}$ – 0.8<br>$V_{DD}$ – 0.8 | <br>—<br>— | <br>—<br>— | V |
| | | Output high voltage — High Drive (PTxDSn = 1) V<br>5 V, $I_{Load}$ = –10 mA<br>3 V, $I_{Load}$ = –3 mA | | <br>$V_{DD}$ – 0.8<br>$V_{DD}$ – 0.8 | <br>—<br>— | <br>—<br>— | |
| 3 | P | Output low voltage — Low Drive (PTxDSn = 0)<br>5 V, $I_{Load}$ = 2 mA<br>3 V, $I_{Load}$ = 0.6 mA | $V_{OL}$ | — | <br>—<br>— | <br>0.8<br>0.8 | V |
| | | Output low voltage — High Drive (PTxDSn = 1)<br>5 V, $I_{Load}$ = 10 mA<br>3 V, $I_{Load}$ = 3 mA | | | <br>—<br>— | <br>0.8<br>0.8 | |
| 4 | P | Output high current — Max total $I_{OH}$ for all ports<br>5 V<br>3 V | $I_{OHT}$ | — | — | <br>100<br>60 | mA |
| 5 | C | Output high current — Max total $I_{OL}$ for all ports<br>5 V<br>3 V | $I_{OLT}$ | — | — | <br>100<br>60 | mA |
| 6 | P | Bandgap voltage reference | $V_{BG}$ | — | 1.225 | — | V |
| 7 | P | Input high voltage; all digital inputs | $V_{IH}$ | 0.65 x $V_{DD}$ | — | — | V |
| 8 | P | Input low voltage; all digital inputs | $V_{IL}$ | — | — | 0.35 x $V_{DD}$ | V |
| 9 | P | Input hysteresis; all digital inputs | $V_{hys}$ | 0.06 x $V_{DD}$ | — | — | mV |
| 10 | P | Input leakage current; input only pins[2]<br>$V_{In}$ = $V_{DD}$ or $V_{SS}$ | $\lvert I_{In} \rvert$ | — | 0.1 | 1 | μA |
| 11 | P | High impedence (off-state) leakage current<br>$V_{In}$ = $V_{DD}$ or $V_{SS}$ | $\lvert I_{OZ} \rvert$ | — | 0.1 | 1 | μA |
| 12 | P | Internal pullup resistors[3] | $R_{PU}$ | 20 | 45 | 65 | kΩ |
| 13 | P | Internal pulldown resistors[4] | $R_{PD}$ | 20 | 45 | 65 | kΩ |

**Table 8. DC Characteristics (continued)**

| Num | C | Characteristic | | Symbol | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| 14 | D | DC injection current [5, 6, 7] $V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$ | Single pin limit | $I_{IC}$ | — | — | 2 | mA |
| | | | Total MCU limit, includes sum of all stressed pins | | — | — | 25 | mA |
| 15 | C | Input Capacitance, all non-supply pins | | $C_{In}$ | — | — | 8 | pF |
| 16 | C | RAM retention voltage | | $V_{RAM}$ | 2 | — | — | V |
| 17 | P | POR rearm voltage | | $V_{POR}$ | 0.9 | 1.4 | 2.0 | V |
| 18 | D | POR rearm time | | $t_{POR}$ | 10 | — | — | µs |
| 19 | P | Low-voltage detection threshold — high range<br>$V_{DD}$ falling<br>$V_{DD}$ rising | | $V_{LVD1}$ | <br>3.9<br>4.0 | <br>4.0<br>4.1 | <br>4.1<br>4.2 | V |
| 20 | P | Low-voltage detection threshold — low range<br>$V_{DD}$ falling<br>$V_{DD}$ rising | | $V_{LVD0}$ | <br>2.48<br>2.54 | <br>2.56<br>2.62 | <br>2.64<br>2.70 | V |
| 21 | P | Low-voltage warning threshold — high range 1<br>$V_{DD}$ falling<br>$V_{DD}$ rising | | $V_{LVW3}$ | <br>4.5<br>4.6 | <br>4.6<br>4.7 | <br>4.7<br>4.8 | V |
| 22 | P | Low-voltage warning threshold — high range 0<br>$V_{DD}$ falling<br>$V_{DD}$ rising | | $V_{LVW2}$ | <br>4.2<br>4.3 | <br>4.3<br>4.4 | <br>4.4<br>4.5 | V |
| 23 | P | Low-voltage warning threshold — low range 1<br>$V_{DD}$ falling<br>$V_{DD}$ rising | | $V_{LVW1}$ | <br>2.84<br>2.90 | <br>2.92<br>2.98 | <br>3.00<br>3.06 | V |
| 24 | P | Low-voltage warning threshold — low range 0<br>$V_{DD}$ falling<br>$V_{DD}$ rising | | $V_{LVW0}$ | <br>2.66<br>2.72 | <br>2.74<br>2.80 | <br>2.82<br>2.88 | V |
| 25 | P | Low-voltage inhibit reset/recover hysteresis<br>5 V<br>3 V | | $V_{hys}$ | — | <br>100<br>60 | — | mV |

1 Typical values are measured at 25 °C. Characterized, not tested

2 Measured with $V_{In} = V_{DD}$ or $V_{SS}$.

3 Measured with $V_{In} = V_{SS}$.

4 Measured with $V_{In} = V_{DD}$.

5 All functional non-supply pins, except for PTC6 are internally clamped to $V_{SS}$ and $V_{DD}$.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 Power supply must maintain regulation within operating $V_{DD}$ range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is greater than $I_{DD}$, the injection current may flow out of $V_{DD}$ and could result in external power supply going out of regulation. Ensure that external $V_{DD}$ load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. For instance, if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

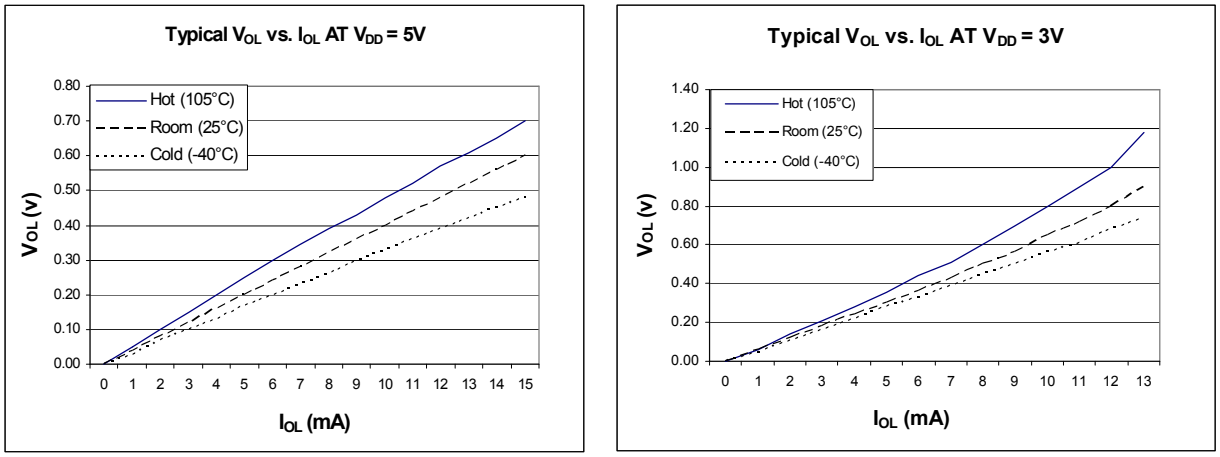



**Figure 5. Typical Low-side Drive (sink) characteristics – High Drive (PTxDSn = 1)**

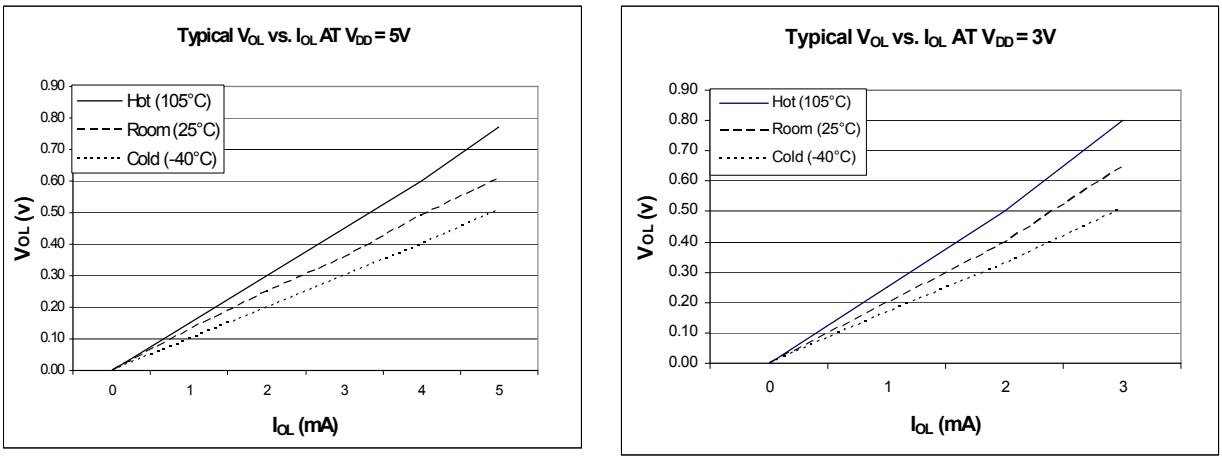



**Figure 6. Typical Low-side Drive (sink) characteristics – Low Drive (PTxDSn = 0)**

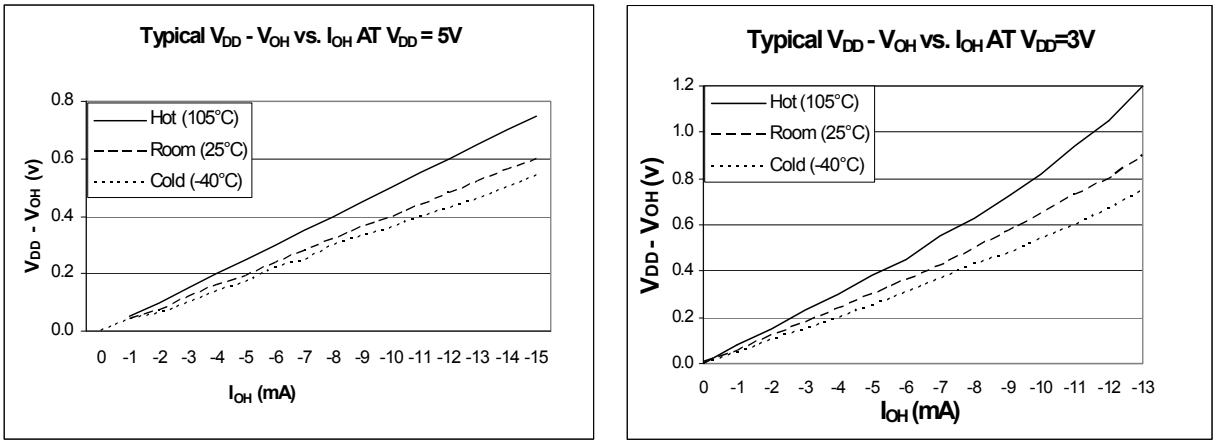



**Figure 7. Typical High-side Drive (source) characteristics – High Drive (PTxDSn = 1)**

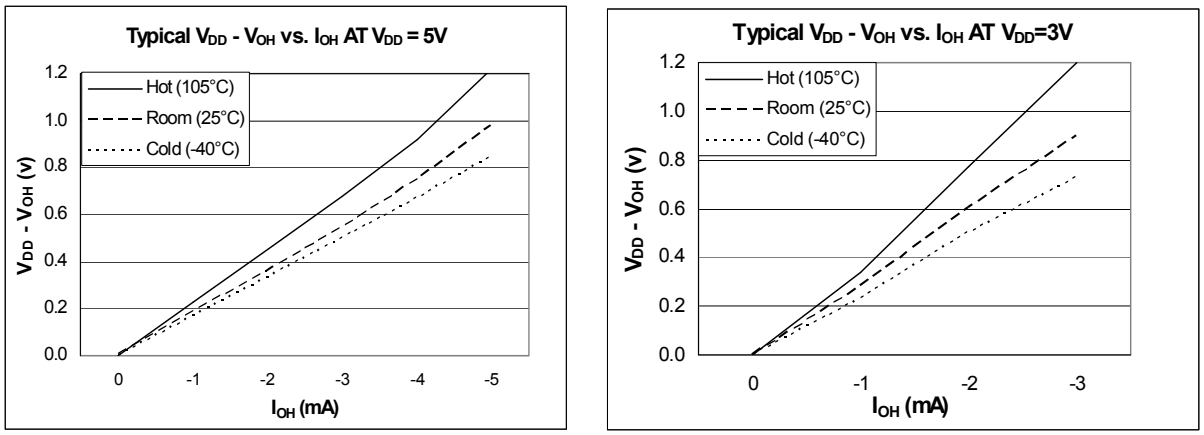



**Figure 8. Typical High-side Drive (source) characteristics – Low Drive (PTxDSn = 0)**

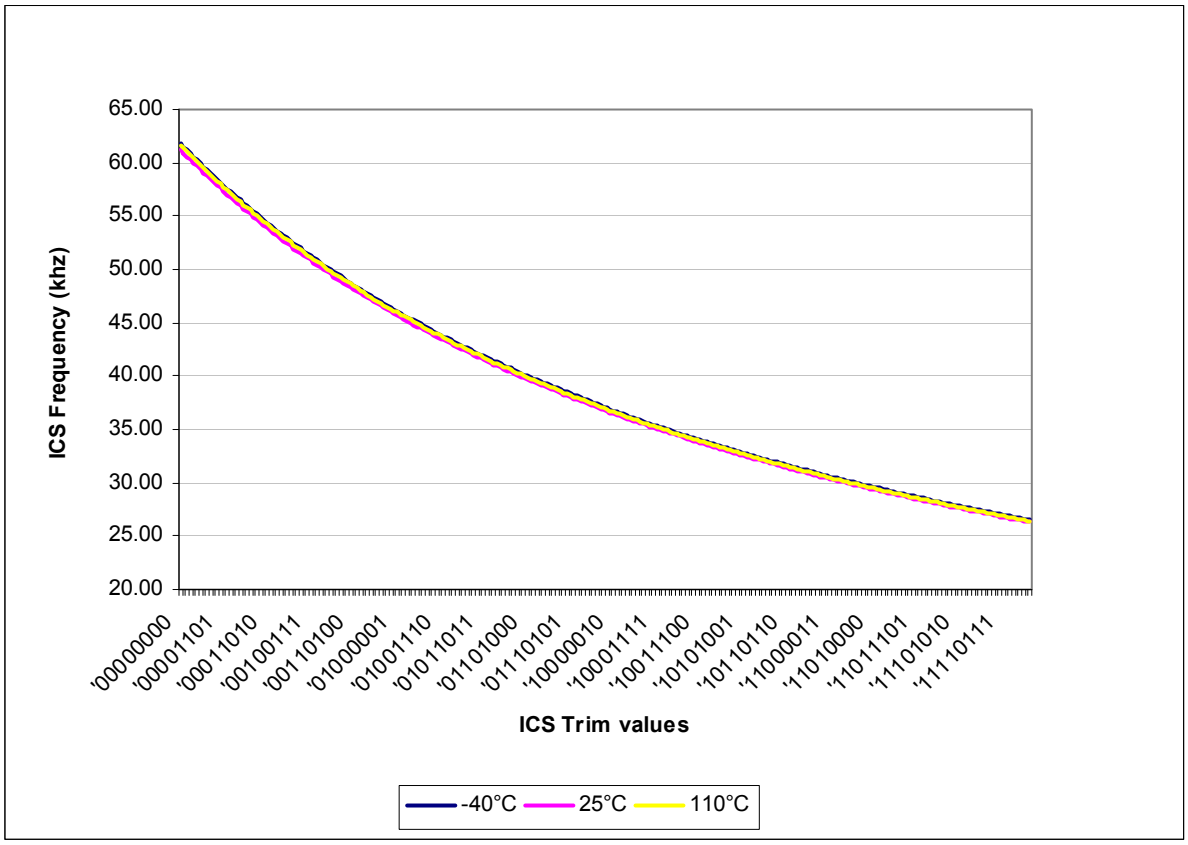



**Figure 17. Internal Oscillator Deviation from Trimmed Frequency**

## 2.10 ADC Characteristics

**Table 12. 12-bit ADC Operating Conditions**

| Characteristic | Conditions | Symb | Min | Typ[1] | Max | Unit | Comment |
|---|---|---|---|---|---|---|---|
| Supply voltage | Absolute | $V_{DDAD}$ | 2.7 | — | 5.5 | V | — |
| | Delta to $V_{DD}$ ($V_{DD} - V_{DDAD}$)[2] | $\Delta V_{DDAD}$ | –100 | 0 | +100 | mV | — |
| Ground voltage | Delta to $V_{SS}$ ($V_{SS} - V_{SSAD}$)[2] | $\Delta V_{SSAD}$ | –100 | 0 | +100 | mV | — |
| Ref Voltage High | — | $V_{REFH}$ | — | — | — | V | $V_{REFH}$ shorted to $V_{DDAD}$ |
| Ref Voltage Low | — | $V_{REFL}$ | — | — | — | V | $V_{REFL}$ shorted to $V_{SSAD}$ |
| Input Voltage | — | $V_{ADIN}$ | $V_{REFL}$ | — | $V_{REFH}$ | V | — |
| Input Capacitance | — | $C_{ADIN}$ | — | 4.5 | 5.5 | pF | — |

**Table 12. 12-bit ADC Operating Conditions (continued)**

| Characteristic | Conditions | Symb | Min | Typ[1] | Max | Unit | Comment |
|---|---|---|---|---|---|---|---|
| Input Resistance | — | $R_{ADIN}$ | — | 5 | 7 | kΩ | — |
| Analog Source Resistance | 12-bit mode<br>$f_{ADCK}$ > 4MHz<br>$f_{ADCK}$ < 4MHz | $R_{AS}$ | <br>—<br>— | <br>—<br>— | <br>2<br>5 | kΩ | External to MCU |
| | 10-bit mode<br>$f_{ADCK}$ > 4MHz<br>$f_{ADCK}$ < 4MHz | | <br>—<br>— | <br>—<br>— | <br>5<br>10 | | |
| | 8-bit mode (all valid $f_{ADCK}$) | | — | — | 10 | | |
| ADC Conversion Clock Freq. | High Speed (ADLPC = 0) | $f_{ADCK}$ | 0.4 | — | 8.0 | MHz | — |
| | Low Power (ADLPC = 1) | | 0.4 | — | 4.0 | | |

1 Typical values assume $V_{DDAD}$ = 5.0 V, Temp = 25 °C, $f_{ADCK}$ = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

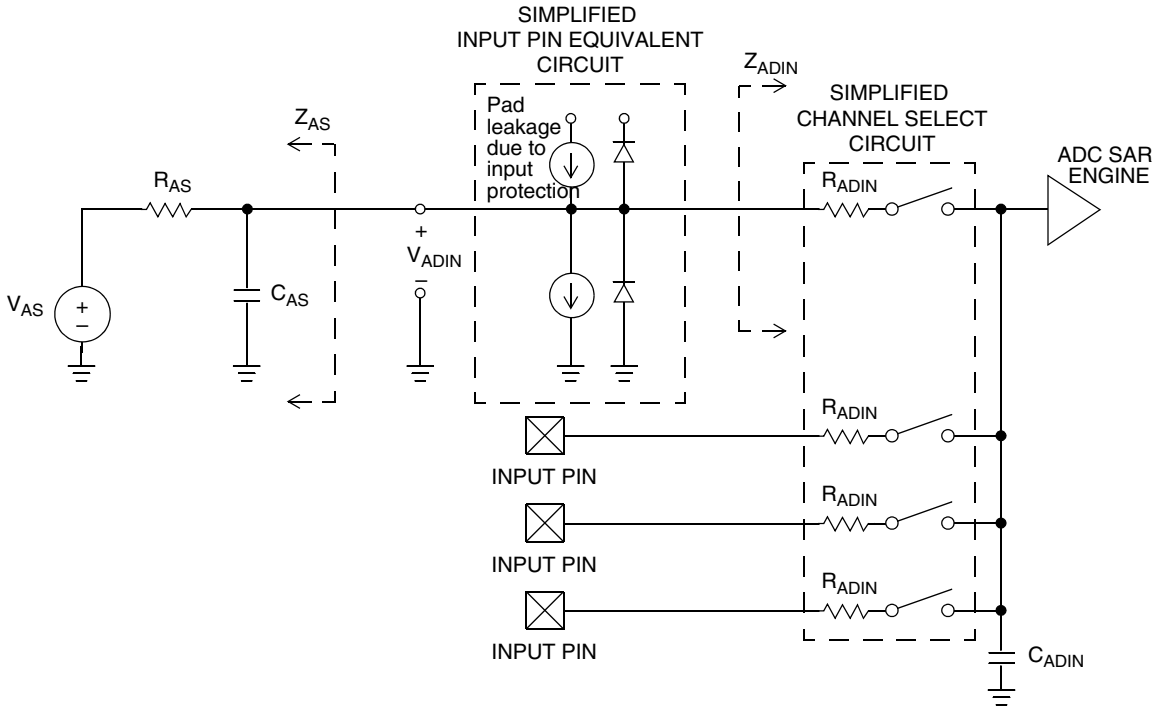



**Figure 18. ADC Input Impedance Equivalency Diagram**

## 2.11 AC Characteristics

This section describes timing characteristics for each peripheral system.

### 2.11.1 Control Timing

**Table 14. Control Timing**

| Num | C | Rating | Symbol | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | D | Bus frequency ($t_{cyc}$ = 1/$f_{Bus}$) | $f_{Bus}$ | dc | — | 20 | MHz |
| 2 | D | Internal low power oscillator period | $t_{LPO}$ | 700 | — | 1300 | µs |
| 3 | D | External reset pulse width[2] | $t_{extrst}$ | 100 | — | — | ns |
| 4 | D | Reset low drive | $t_{rstdrv}$ | 66 x $t_{cyc}$ | — | — | ns |
| 5 | D | BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes | $t_{MSSU}$ | 500 | — | — | ns |
| 6 | D | BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3] | $t_{MSH}$ | 100 | — | — | µs |
| 7 | D | IRQ pulse width<br>Asynchronous path[2]<br>Synchronous path[4] | <br>$t_{ILIH}$<br>$t_{IHIL}$ | <br>100<br>1.5 x $t_{cyc}$ | <br>—<br>— | <br>—<br>— | ns |
| 8 | D | Keyboard interrupt pulse width<br>Asynchronous path[2]<br>Synchronous path[4] | <br>$t_{ILIH}$<br>$t_{IHIL}$ | <br>100<br>1.5 x $t_{cyc}$ | <br>—<br>— | <br>—<br>— | ns |
| 9 | C | Port rise and fall time — (load = 50 pF)[5, 6]<br>Slew rate control disabled (PTxSE = 0)<br>Slew rate control enabled (PTxSE = 1) | <br>$t_{Rise}$<br>$t_{Fall}$ | <br>—<br>— | <br>3<br>30 | <br>—<br>— | ns |

1 Typical values are based on characterization data at $V_{DD}$ = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of $t_{MSH}$ after $V_{DD}$ rises above $V_{LVD}$.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

5 Timing is shown with respect to 20% $V_{DD}$ and 80% $V_{DD}$ levels. Temperature range –40 °C to 105 °C.

6 Except for LCD pins in Open Drain mode.

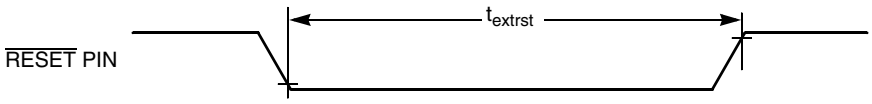



**Figure 19. Reset Timing**

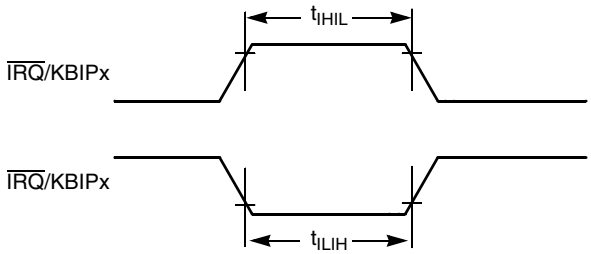



**Figure 20. IRQ/KBIPx Timing**

## 2.11.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

**Table 15. TPM Input Timing**

| No. | C | Function | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | D | External clock frequency | $f_{TCLK}$ | 0 | $f_{Bus}/4$ | Hz |
| 2 | D | External clock period | $t_{TCLK}$ | 4 | — | $t_{cyc}$ |
| 3 | D | External clock high time | $t_{clkh}$ | 1.5 | — | $t_{cyc}$ |
| 4 | D | External clock low time | $t_{clkl}$ | 1.5 | — | $t_{cyc}$ |
| 5 | D | Input capture pulse width | $t_{ICPW}$ | 1.5 | — | $t_{cyc}$ |

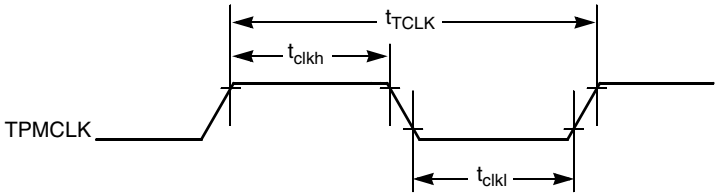



**Figure 21. Timer External Clock**

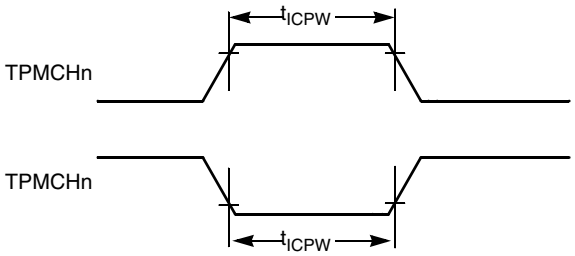
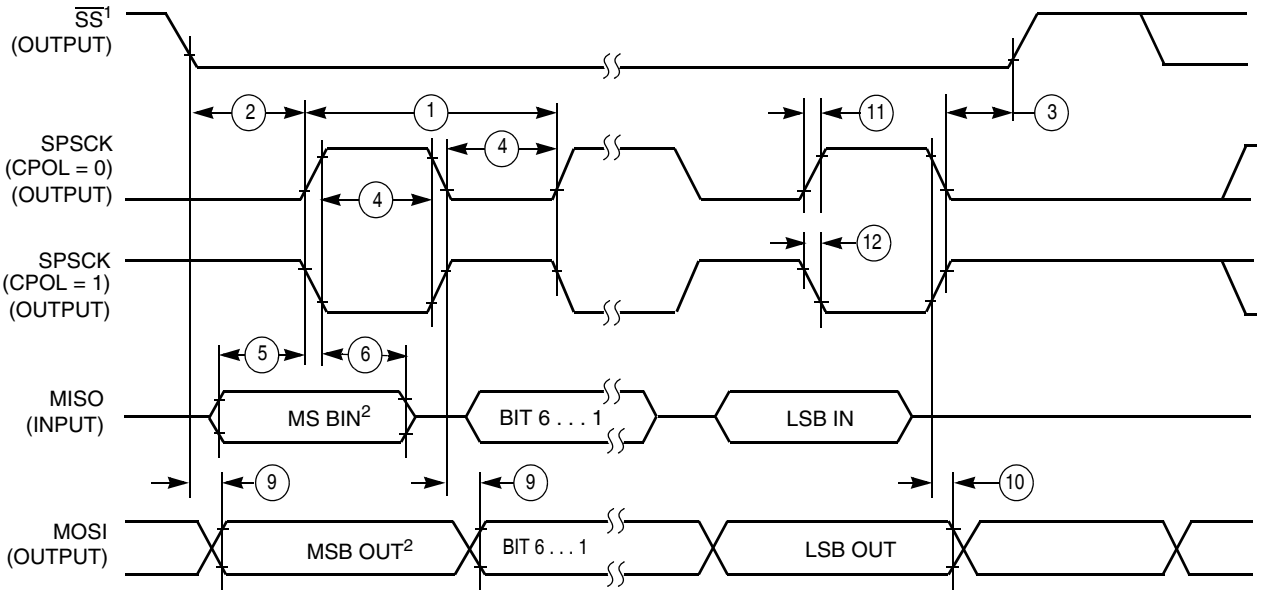
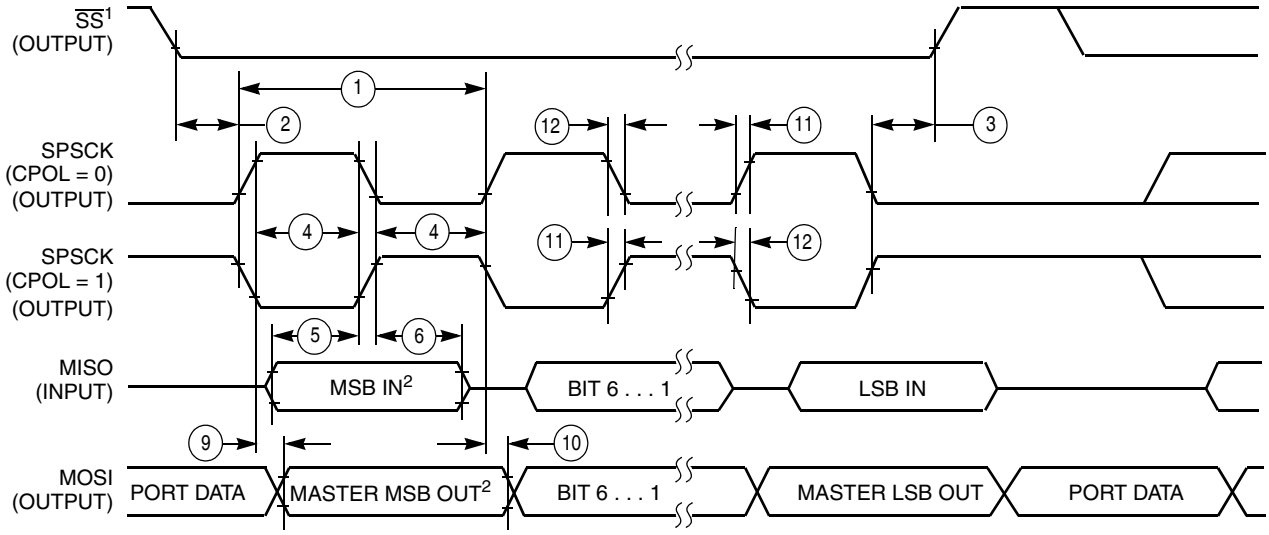



**Figure 22. Timer Input Capture Pulse**




NOTES:
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 23. SPI Master Timing (CPHA = 0)**




NOTES:
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 24. SPI Master Timing (CPHA =1)**

## 2.12 LCD Specifications

**Table 17. LCD Electricals, 3 V Glass**

| C | Characteristic | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| D | VLL3 Supply Voltage | VLL3 | 2.7 | — | 5.5 | V |
| D | LCD Frame Frequency | $f_{Frame}$ | 28 | 30 | 64 | Hz |
| D | LCD Charge Pump Capacitance | $C_{LCD}$ | — | 100 | 100 | pF |
| D | LCD Bypass Capacitance | $C_{BYLCD}$ | — | 100 | 100 | |
| D | LCD Glass Capacitance | $C_{glass}$ | — | 2000 | 8000 | |

## 2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal $V_{DD}$ supply. For more detailed information about program/erase operations, see the Memory section.

**Table 18. Flash Characteristics**

| C | Characteristic | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| D | Supply voltage for program/erase<br>–40 °C to 85 °C | $V_{prog/erase}$ | 2.7 | | 5.5 | V |
| D | Supply voltage for read operation | $V_{Read}$ | 2.7 | | 5.5 | V |
| D | Internal FCLK frequency[1] | $f_{FCLK}$ | 150 | | 200 | kHz |
| D | Internal FCLK period (1/FCLK) | $t_{Fcyc}$ | 5 | | 6.67 | µs |
| C | Byte program time (random location)[2] | $t_{prog}$ | 9 | | | $t_{Fcyc}$ |
| C | Byte program time (burst mode)[2] | $t_{Burst}$ | 4 | | | $t_{Fcyc}$ |
| C | Page erase time[2] | $t_{Page}$ | 4000 | | | $t_{Fcyc}$ |
| C | Mass erase time[2] | $t_{Mass}$ | 20,000 | | | $t_{Fcyc}$ |
| D | Byte program current[3] | $R_{IDDBP}$ | — | 4 | — | mA |
| D | Page erase current[3] | $R_{IDDPE}$ | — | 6 | — | mA |
| C | Program/erase endurance[4]<br>$T_L$ to $T_H$ = –40 °C to + 85 °C<br>T = 25 °C | | 10,000 | —<br>100,000 | —<br>— | cycles |
| C | Data retention[5] | $t_{D\_ret}$ | 15 | 100 | — | years |

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 The program and erase currents are additional to the standard run $I_{DD}$. These values are measured at room temperatures with $V_{DD}$ = 5.0 V, bus frequency = 4.0 MHz.

4 **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to *Engineering Bulletin EB619, Typical Endurance for Nonvolatile Memory.*

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25 °C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to *Engineering Bulletin EB618, Typical Data Retention for Nonvolatile Memory.*

## 2.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

### 2.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

**Table 19. Radiated Emissions, Electric Field**

| Parameter | Symbol | Conditions | Frequency | $f_{OSC}/f_{BUS}$ | Level[1] (Max) | Unit |
|---|---|---|---|---|---|---|
| Radiated emissions, electric field | $V_{RE\_TEM}$ | $V_{DD}$ = 5.5<br>$T_A$ = +25 °C<br>Package type = 80 LQFP | 0.15 – 50 MHz | 4 MHz crystal<br>16 MHz bus | 10 | dBμV |
| | | | 50 – 150 MHz | | 14 | |
| | | | 150 – 500 MHz | | 8 | |
| | | | 500 – 1000 MHz | | 5 | |
| | | | IEC Level | | L | — |
| | | | SAE Level | | 2 | — |

1 Data based on qualification test results.

### 2.14.2 Conducted Transient Susceptibility

Microcontroller transient conducted susceptibility is measured in accordance with an internal Freescale test method. The measurement is performed with the microcontroller installed on a custom EMC evaluation board and running specialized EMC test software designed in compliance with the test method. The conducted susceptibility is determined by injecting the transient susceptibility signal on each pin of the microcontroller. The transient waveform and injection methodology is based on IEC 61000-4-4 (EFT/B). The transient voltage required to cause performance degradation on any pin in the tested configuration is greater than or equal to the reported levels unless otherwise indicated by footnotes below Table 20.

**Table 20. Conducted Susceptibility, EFT/B**

| Parameter | Symbol | Conditions | $f_{OSC}/f_{BUS}$ | Result | Amplitude[1] (Min) | Unit |
|---|---|---|---|---|---|---|
| Conducted susceptibility, electrical fast transient/burst (EFT/B) | $V_{CS\_EFT}$ | $V_{DD}$ = 5.5<br>$T_A$ = +25 °C<br>Package type = 80-pin LQFP | 4 kHz crystal<br>4 MHz bus | A<br>B<br>C<br>D | >4.0[2]<br>>4.0[3]<br>>4.0[4]<br>>4.0 | kV |

1 Data based on qualification test results. Not tested in production.

2 Exceptions as covered in footnotes 3 and 4.

3 Except pins PHT1, PTH2, PTH3, PTH4, PTH5. See figures below for values.
4 Except pins PTF3, PTH5, PTH4, PHT0, Reset, and BKGD. See figures below for values.

Individual performance of each pin is shown in Figure 27, Figure 28, Figure 29, and Figure 30.

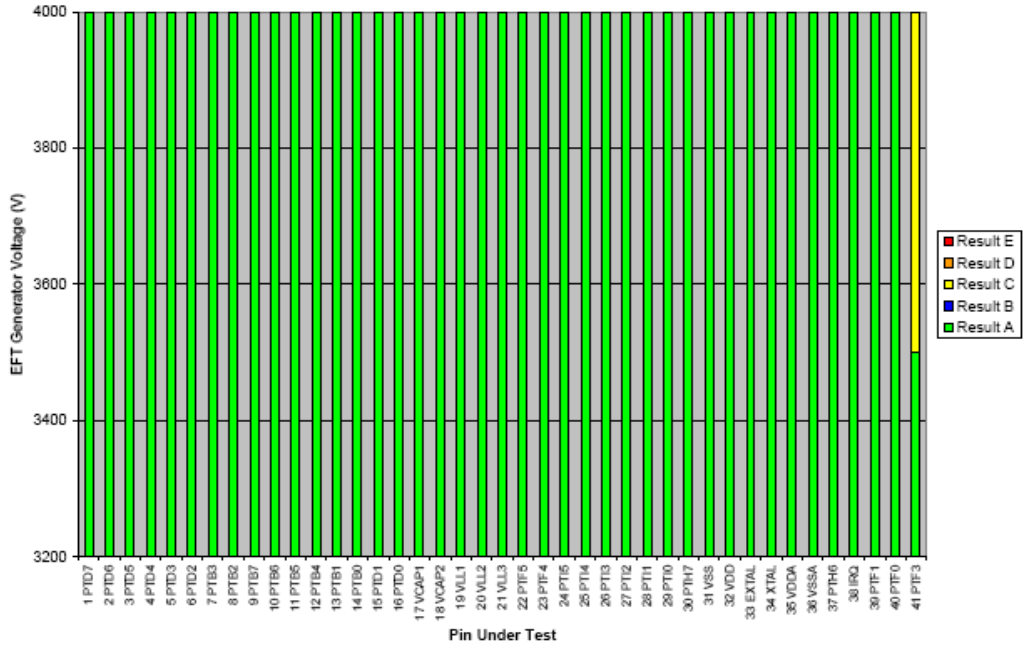
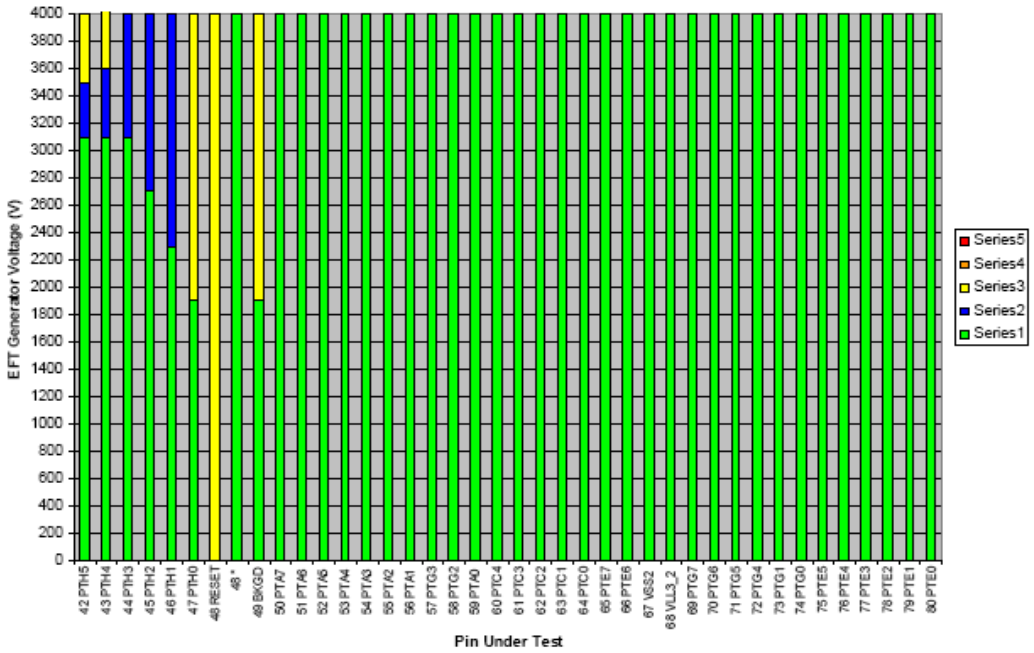



**Figure 27. 4 MHz, Positive Polarity Pins 1 – 41**




**Note:**
RESET retested with 0.1 μF capacitor from pin to ground is Class A compliant as shown by 48*.

**Figure 28. 4 MHz, Positive Polarity Pins 42 – 80**

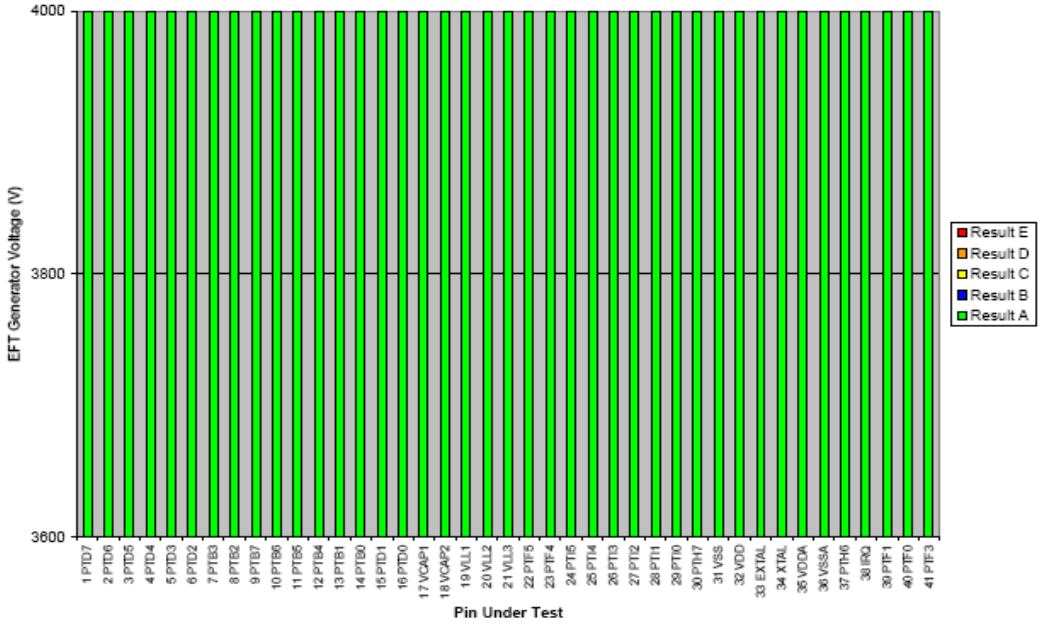
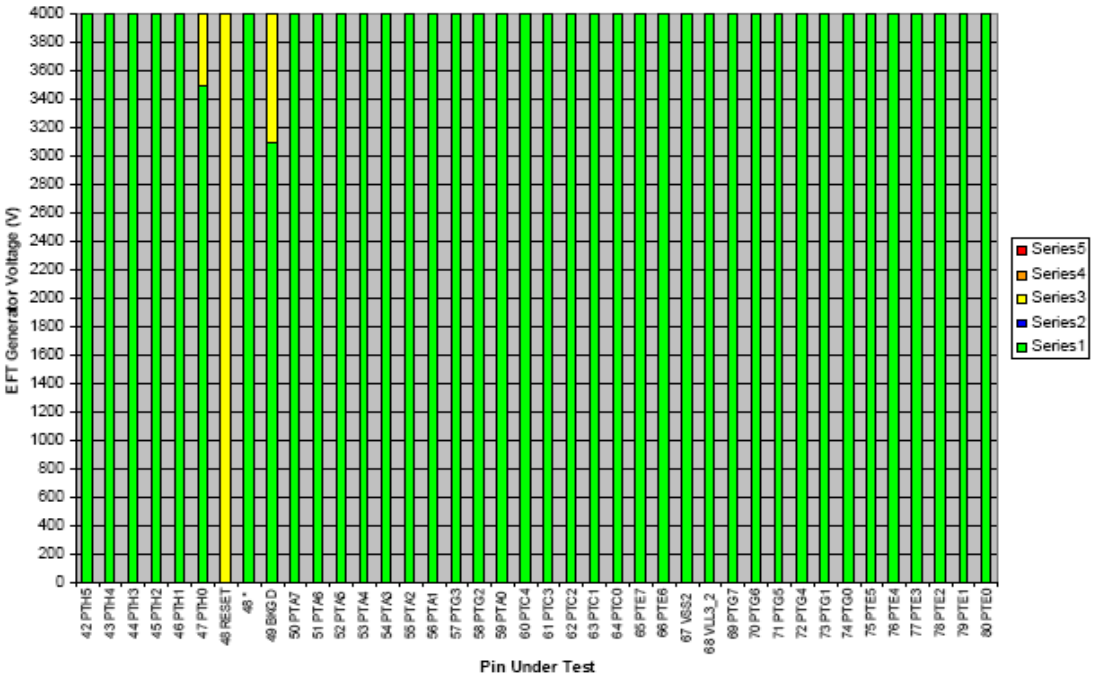



**Figure 29. 4 MHz, Negative Polarity Pins 1 – 41**




**Note:**
RESET retested with 0.1 μF capacitor from pin to ground is Class A compliant as shown by 48*.

**Figure 30. 4 MHz, Negative Polarity Pins 42 – 80**

## 3.1 Device Numbering System

Example of the device numbering system:

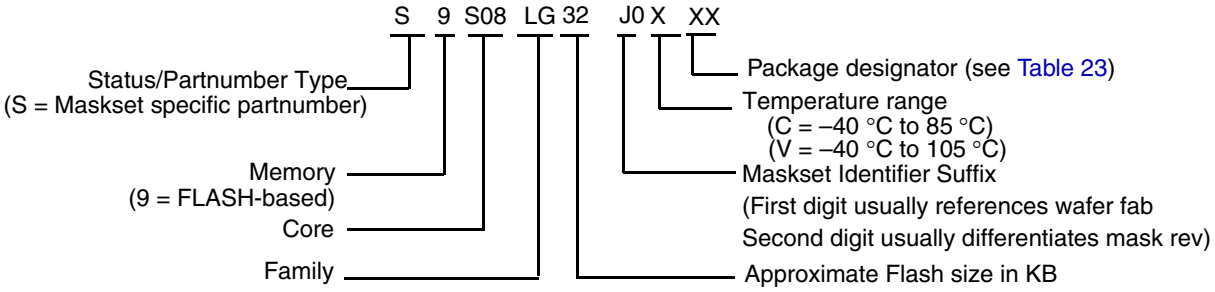



**Figure 31. Device Number Example for Auto Parts**

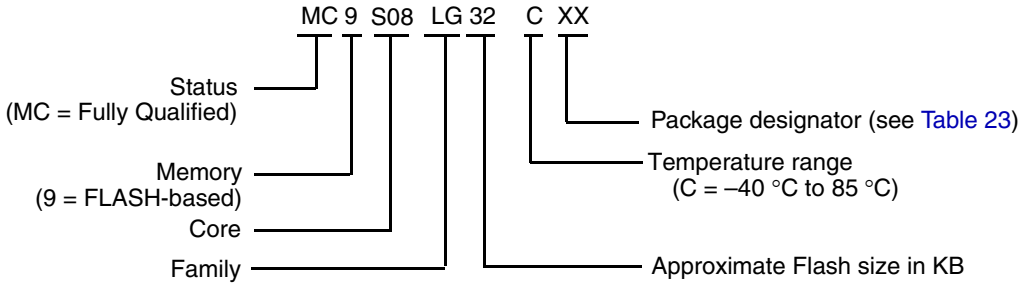



**Figure 32. Device Number Example for IMM Parts**

# 4 Package Information

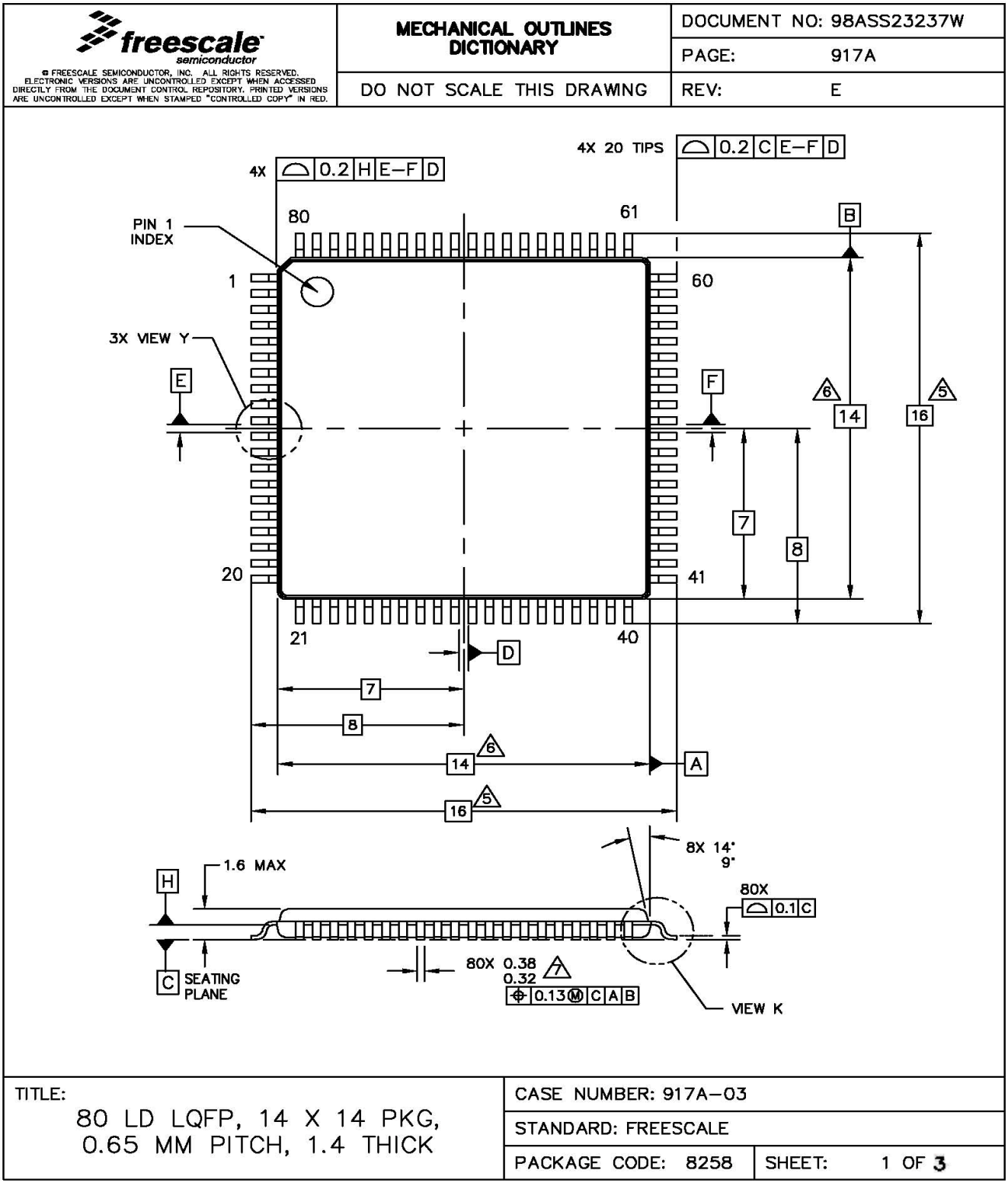
**Table 23. Package Descriptions**

| Pin Count | Package Type | Abbreviation | Designator | Case No. | Document No. |
|---|---|---|---|---|---|
| 80 | Low Quad Flat Package | LQFP | LK | 917A | 98ASS23237W |
| 64 | Low Quad Flat Package | LQFP | LH | 840F | 98ASS23234W |
| 48 | Low Quad Flat Package | LQFP | LF | 932 | 98ASH00962A |

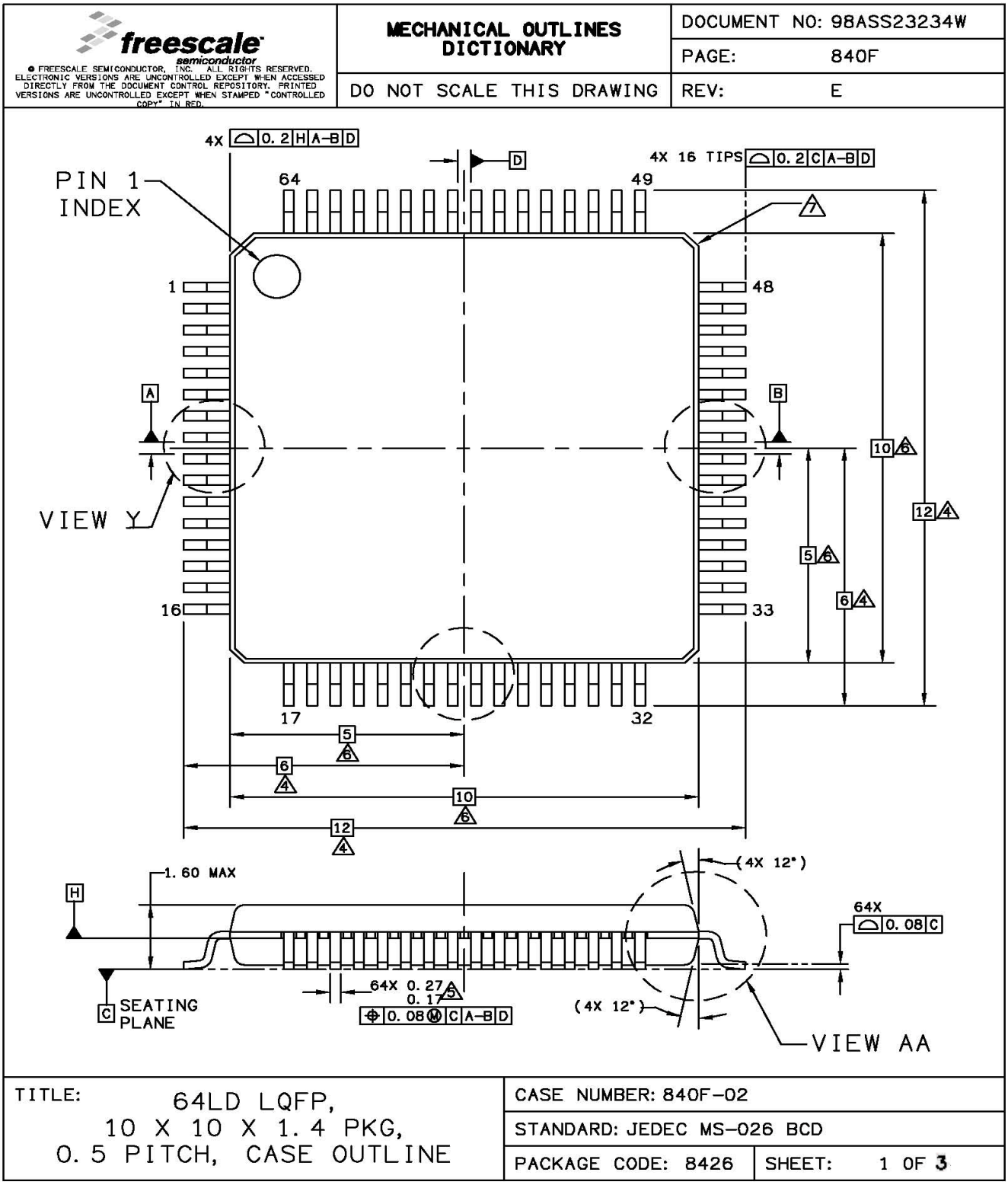
## 4.1 Mechanical Drawings

The following pages are mechanical drawings for the packages described in Table 23. For the latest available drawings please visit our web site (http://www.freescale.com) and enter the package's document number into the keyword search box.

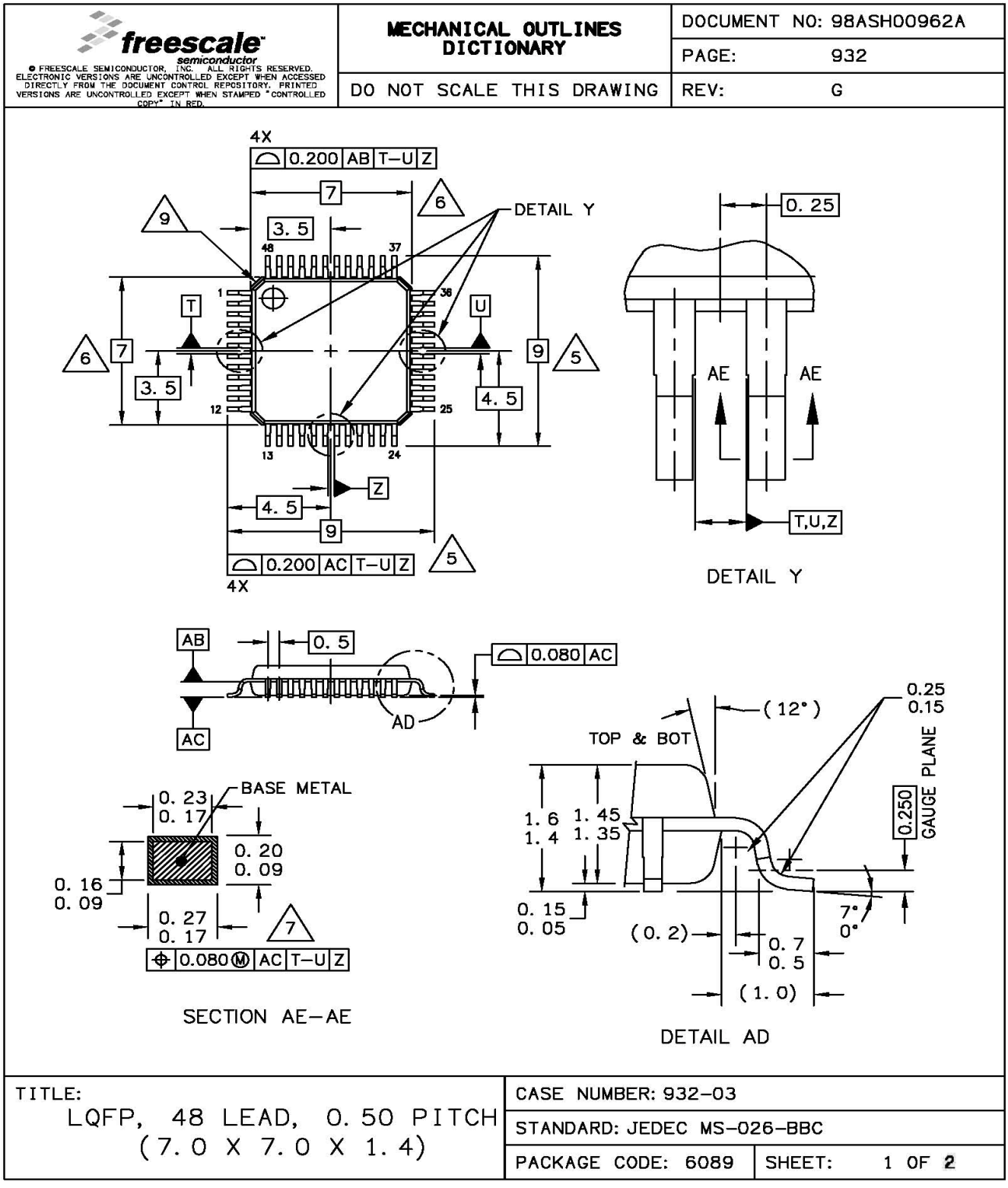
## 4.1.1 80-pin LQFP



## 4.1.2 64-pin LQFP



## 4.1.3 48-pin LQFP



# 5 Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web are the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://www.freescale.com

The following revision history table summarizes changes contained in this document.

**Table 24. Revision History**

| Revision | Date | Description of Changes |
|---|---|---|
| 1 | 8/2008 | First Initial release. |
| 2 | 9/2008 | Second Initial Release. |
| 3 | 11/2008 | Alpha Customer Release. |
| 4 | 2/2009 | Launch Release. |
| 5 | 4/2009 | Added EMC Radiated Emission and Transient Susceptibility data in Table 19 and Table 20. |
| 6 | 4/2009 | Updated EMC performance data. |
| 7 | 8/2009 | Updated auto part numbers, changed TCLK, T0CH0, T0CH1, T1CH0, T1CH1, T1CH2, T1CH3, T1CH3, T1CH4, and T1CH5 to TPMCLK, TPM0CH0, TPM0CH1,TPM1CH0, TPM1CH1, TPM1CH2, TPM1CH3, TPM1CH4, and TPM1CH5, and changed the maximum LCD frame frequency to 64 Hz. |
| 8 | 8/2011 | Updated Table “ICS Frequency Specifications (Temperature Range = –40 ×C to 105 ×C Ambient)”. Changed the value of row 8 column C from C to P. |
| 9 | 9/2011 | Updated Table “ICS Frequency Specifications (Temperature Range = –40 ×C to 105 ×C Ambient)”. Removed Footnote from Row 8.<br>Updated the Revision History |