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#### Applications of "[Embedded - Microcontrollers](#)"

##### Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I <sup>2</sup> C, SCI, SPI
Peripherals	LCD, LVD, PWM
Number of I/O	39
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.9K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mc9s08lg32clf">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mc9s08lg32clf</a>

## MC9S08LG32 Series

### Covers: MC9S08LG32 and MC9S08LG16

#### Features

- 8-bit HCS08 Central Processor Unit (CPU)
  - Up to 40 MHz CPU at 5.5 V to 2.7 V across temperature range of –40 °C to 85 °C and –40 °C to 105 °C
  - HCS08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - 32 KB or 18 KB dual array flash; read/program/erase over full operating voltage and temperature
  - 1984 byte random access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
  - Two low-power stop modes (stop2 and stop3)
  - Reduced-power wait mode
  - Peripheral clock gating register can disable clocks to unused modules, thereby reducing currents
  - Low power On-Chip crystal oscillator (XOSC) that can be used in low-power modes to provide accurate clock source to real time counter and LCD controller
  - 100 µs typical wakeup time from stop3 mode
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports bus frequencies from 1 MHz to 20 MHz.
- System Protection
  - COP reset with option to run from dedicated 1 kHz internal clock or bus clock
  - Low-voltage warning with interrupt
  - Low-voltage detection with reset
  - Illegal opcode detection with reset
  - Illegal address detection with reset
  - Flash and RAM protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging and plus two more breakpoints in On-Chip debug module

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## MC9S08LG32

- On-Chip in-circuit emulator (ICE) debug module containing three comparators and nine trigger modes; eight deep FIFO for storing change-of-flow addresses and event-only data; debug module supports both tag and force breakpoints
- Peripherals
  - **LCD** — Up to 4 × 41 or 8 × 37 LCD driver with internal charge pump.
  - **ADC** — Up to 16-channel, 12-bit resolution, 2.5 µs conversion time, automatic compare function, temperature sensor, internal bandgap reference channel, runs in stop3 and can wake up the system, fully functional from 5.5 V to 2.7 V
  - **SCI** — Full duplex non-return to zero (NRZ), LIN master extended break generation, LIN slave extended break detection, wakeup on active edge
  - **SPI** — Full-duplex or single-wire bidirectional, double-buffered transmit and receive, master or slave mode, MSB-first or LSB-first shifting
  - **IIC** — With up to 100 kbps with maximum bus loading, multi-master operation, programmable slave address, interrupt driven byte-by-byte data transfer, supports broadcast mode and 10-bit addressing
  - **TPMx** — One 6 channel and one 2 channel, selectable input capture, output compare, or buffered edge or center-aligned PWM on each channel
  - **MTIM** — 8-bit counter with match register, four clock sources with prescaler dividers, can be used for periodic wakeup
  - **RTC** — 8-bit modulus counter with binary or decimal based prescaler, three clock sources including one external source, can be used for time base, calendar, or task scheduling functions
  - **KBI** — One keyboard control module capable of supporting 8 × 8 keyboard matrix
  - **IRQ** — External pin for wakeup from low-power modes
- Input/Output
  - 39, 53, or 69 GPIOs
  - 8 KBI and 1 IRQ interrupt with selectable polarity
  - Hysteresis and configurable pullup device on all input pins, configurable slew rate and drive strength on all output pins.
- Package Options
  - 48-pin LQFP, 64-pin LQFP, and 80-pin LQFP

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**Table 1. MC9S08LG32 Series Features by MCU and Package**

Feature	MC9S08LG32			MC9S08LG16
Flash size (bytes)	32,768			18,432
RAM size (bytes)	1984			
Pin quantity	80	64	48	64
ADC	16 ch	12 ch	9 ch	12 ch
LCD	8 x 37 4 x 41	8 x 29 4 x 33	8 x 21 4 x 25	8 x 29 4 x 33
ICE + DBG	yes			
ICS	yes			
IIC	yes			
IRQ	yes			
KBI	8 pin			
GPIOs	69	53	39	53
RTC	yes			
MTIM	yes			
SCI1	yes			
SCI2	yes			
SPI	yes			
TPM1 channels	2			
TPM2 channels	6			
XOSC	yes			

## 1 Pin Assignments

This section shows the pin assignments for the MC9S08LG32 series devices. The priority of functions on a pin is in ascending order from left to right and bottom to top. Another view of pinouts and function priority is given in [Table 2](#).

## Pin Assignments

Table 2. Pin Availability by Package Pin-Count

Packages				<-- Lowest Priority --> Highest			
80	64	48	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	1	1	PTD7	LCD7	—	—	—
2	2	2	PTD6	LCD6	—	—	—
3	3	3	PTD5	LCD5	—	—	—
4	4	4	PTD4	LCD4	—	—	—
5	5	5	PTD3	LCD3	—	—	—
6	6	6	PTD2	LCD2	—	—	—
7	7	—	PTB3	LCD32	—	—	—
8	8	—	PTB2	LCD31	—	—	—
9	—	—	PTB7	LCD40	—	—	—
10	—	—	PTB6	LCD39	—	—	—
11	—	—	PTB5	LCD38	—	—	—
12	—	—	PTB4	LCD37	—	—	—
13	9	—	PTB1	LCD30	—	—	—
14	10	—	PTB0	LCD29	—	—	—
15	11	7	PTD1	LCD1	—	—	—
16	12	8	PTD0	LCD0	—	—	—
17	13	9	V <sub>CAP1</sub>	—	—	—	—
18	14	10	V <sub>CAP2</sub>	—	—	—	—
19	15	11	V <sub>LL1</sub>	—	—	—	—
20	16	12	V <sub>LL2</sub>	—	—	—	—
21	17	13	V <sub>LL3</sub>	—	—	—	—
22	18	14	PTF5	MOSI	KBI2	TPM2CH3	—
23	19	15	PTF4	MISO	KBI1	TPM2CH4	—
24	20	—	PTI5	TPM2CH0	SCL	SS	—
25	21	—	PTI4	TPM2CH1	SDA	SPSCK	—
26	—	—	PTI3	TPM2CH2	MOSI	—	—
27	—	—	PTI2	TPM2CH3	MISO	—	—
28	—	—	PTI1	TMRCLK	TX2	—	—
29	—	—	PTI0	RX2	—	—	—
30	22	—	PTH7	KBI1	TPM2CH4	—	—
31	23	16	V <sub>SS</sub>	—	—	—	—
32	24	17	V <sub>DD</sub>	—	—	—	—
33	25	18	PTF7	EXTAL	—	—	—
34	26	19	PTF6	XTAL	—	—	—
35	27	20	V <sub>DDA</sub>	V <sub>REFH</sub>	—	—	—
36	28	21	V <sub>SSA</sub>	V <sub>REFL</sub>	—	—	—
37	29	—	PTH6	TPM2CH5	KBI0	ADC15	—
38	30	22	PTF2	SPSCK	TPM1CH1	IRQ	ADC14

**Table 4. Absolute Maximum Ratings**

Rating	Symbol	Value	Unit
Supply voltage	V <sub>DD</sub>	-0.3 to +5.8	V
Maximum current into V <sub>DD</sub>	I <sub>DD</sub>	120	mA
Digital input voltage	V <sub>In</sub>	-0.3 to V <sub>DD</sub> + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins) <sup>1, 2, 3</sup>	I <sub>D</sub>	±25 ±2	mA
Storage temperature range	T <sub>stg</sub>	-55 to 150	°C

<sup>1</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V<sub>DD</sub>) and negative (V<sub>SS</sub>) clamp voltages and use the largest of the two resistance values.

<sup>2</sup> All functional non-supply pins are internally clamped to V<sub>SS</sub> and V<sub>DD</sub>.

<sup>3</sup> Power supply must maintain regulation within operating V<sub>DD</sub> range during instantaneous and operating maximum current conditions. If positive injection current (V<sub>In</sub> > V<sub>DD</sub>) is greater than I<sub>DD</sub>, the injection current may flow out of V<sub>DD</sub> and could result in an external power supply going out of regulation. Ensure that the external V<sub>DD</sub> load will shunt current greater than maximum injection current, this will be of greater risk when the MCU is not consuming power. For instance, if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

## 2.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in On-Chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take P<sub>I/O</sub> into account in power calculations, determine the difference between actual pin voltage and V<sub>SS</sub> or V<sub>DD</sub> and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V<sub>SS</sub> or V<sub>DD</sub> will be very small.

**Table 5. Thermal Characteristics**

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T <sub>A</sub>	T <sub>L</sub> to T <sub>H</sub> -40 to +105	°C
Maximum junction temperature	T <sub>J</sub>	125	°C
Thermal resistance Single-layer board 80-pin LQFP 64-pin LQFP 48-pin LQFP	θ <sub>JA</sub>	61 71 80	°C/W
Thermal resistance Four-layer board 80-pin LQFP 64-pin LQFP 48-pin LQFP	θ <sub>JA</sub>	48 52 56	°C/W

The average chip-junction temperature (T<sub>J</sub>) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA})$$

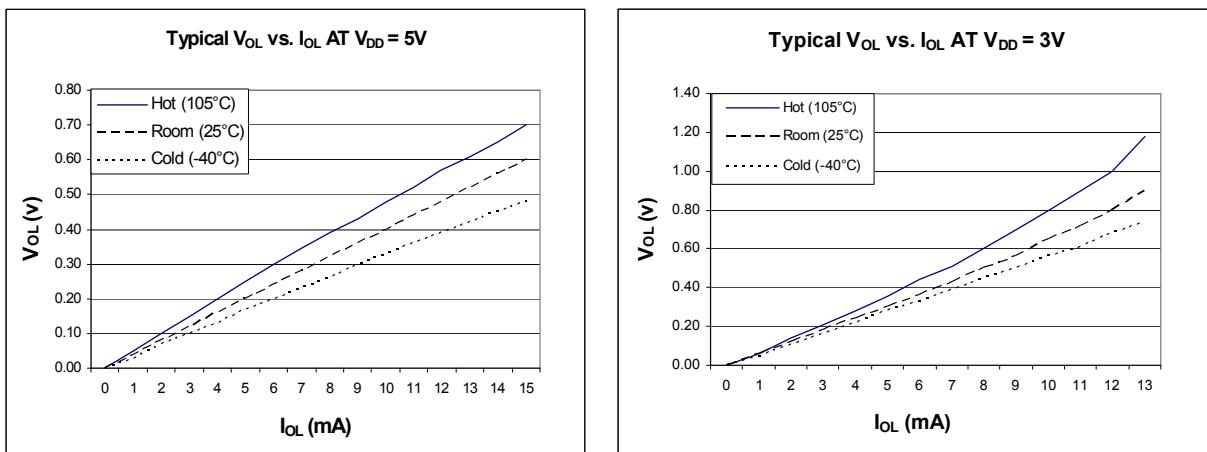
*Eqn. 1*

## Electrical Characteristics

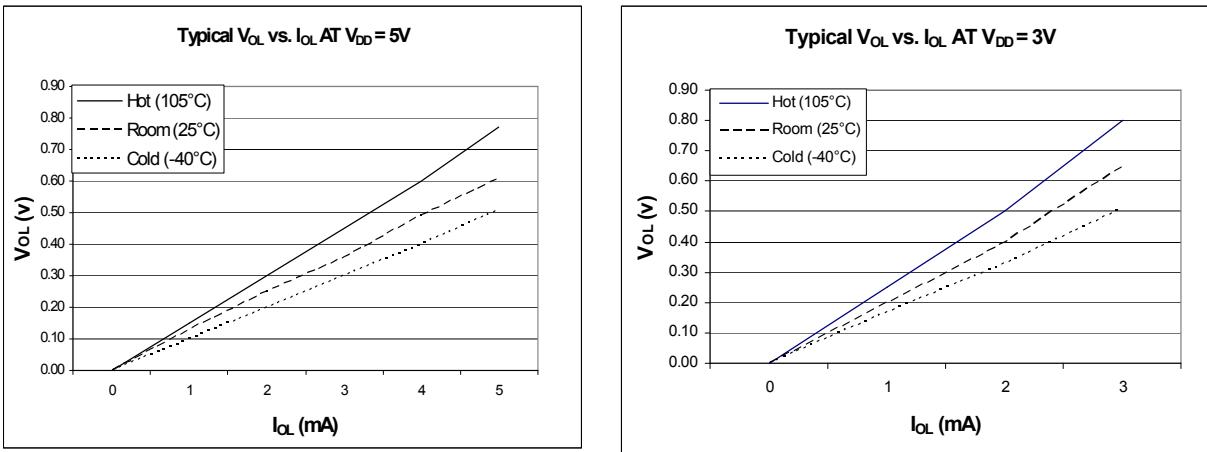
Table 8. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Min	Typ <sup>1</sup>	Max	Unit
14	D	DC injection current <sup>5, 6, 7</sup> $V_{IN} < V_{SS}$ , $V_{IN} > V_{DD}$	$I_{IC}$	—	—	2	mA
				—	—	25	mA
15	C	Input Capacitance, all non-supply pins	$C_{IN}$	—	—	8	pF
16	C	RAM retention voltage	$V_{RAM}$	2	—	—	V
17	P	POR rearm voltage	$V_{POR}$	0.9	1.4	2.0	V
18	D	POR rearm time	$t_{POR}$	10	—	—	$\mu s$
19	P	Low-voltage detection threshold — high range	$V_{LVD1}$	$V_{DD}$ falling $V_{DD}$ rising	3.9	4.0	4.1
					4.0	4.1	4.2
20	P	Low-voltage detection threshold — low range	$V_{LVD0}$	$V_{DD}$ falling $V_{DD}$ rising	2.48	2.56	2.64
					2.54	2.62	2.70
21	P	Low-voltage warning threshold — high range 1	$V_{LVW3}$	$V_{DD}$ falling $V_{DD}$ rising	4.5	4.6	4.7
					4.6	4.7	4.8
22	P	Low-voltage warning threshold — high range 0	$V_{LVW2}$	$V_{DD}$ falling $V_{DD}$ rising	4.2	4.3	4.4
					4.3	4.4	4.5
23	P	Low-voltage warning threshold — low range 1	$V_{LVW1}$	$V_{DD}$ falling $V_{DD}$ rising	2.84	2.92	3.00
					2.90	2.98	3.06
24	P	Low-voltage warning threshold — low range 0	$V_{LVW0}$	$V_{DD}$ falling $V_{DD}$ rising	2.66	2.74	2.82
					2.72	2.80	2.88
25	P	Low-voltage inhibit reset/recover hysteresis	$V_{hys}$	—	100 60	—	mV

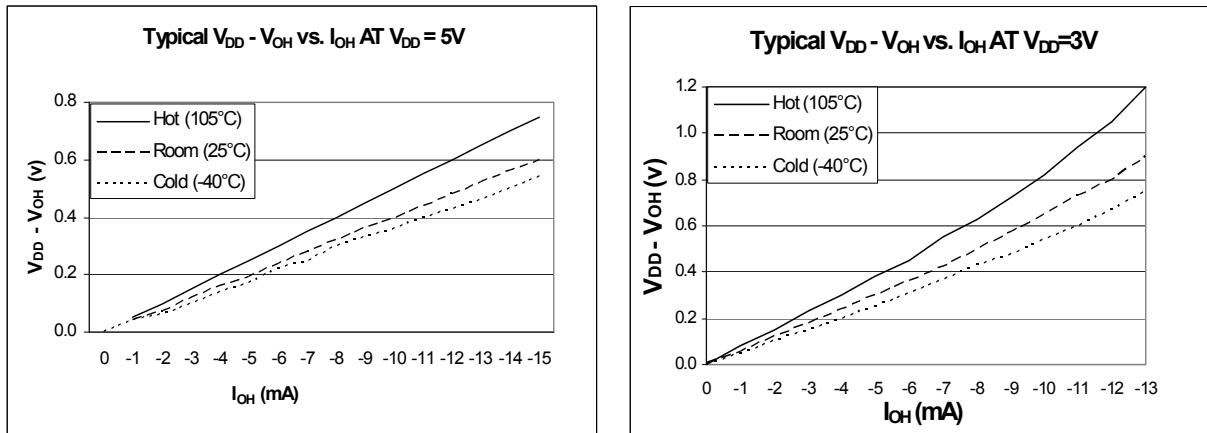
<sup>1</sup> Typical values are measured at 25 °C. Characterized, not tested.<sup>2</sup> Measured with  $V_{IN} = V_{DD}$  or  $V_{SS}$ .<sup>3</sup> Measured with  $V_{IN} = V_{SS}$ .<sup>4</sup> Measured with  $V_{IN} = V_{DD}$ .<sup>5</sup> All functional non-supply pins, except for PTC6 are internally clamped to  $V_{SS}$  and  $V_{DD}$ .<sup>6</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.<sup>7</sup> Power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions. If the positive injection current ( $V_{IN} > V_{DD}$ ) is greater than  $I_{DD}$ , the injection current may flow out of  $V_{DD}$  and could result in external power supply going out of regulation. Ensure that external  $V_{DD}$  load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. For instance, if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).



**Figure 5. Typical Low-side Drive (sink) characteristics – High Drive (PTxDSn = 1)**



**Figure 6. Typical Low-side Drive (sink) characteristics – Low Drive (PTxDSn = 0)**



**Figure 7. Typical High-side Drive (source) characteristics – High Drive (PTxDSn = 1)**

## Electrical Characteristics

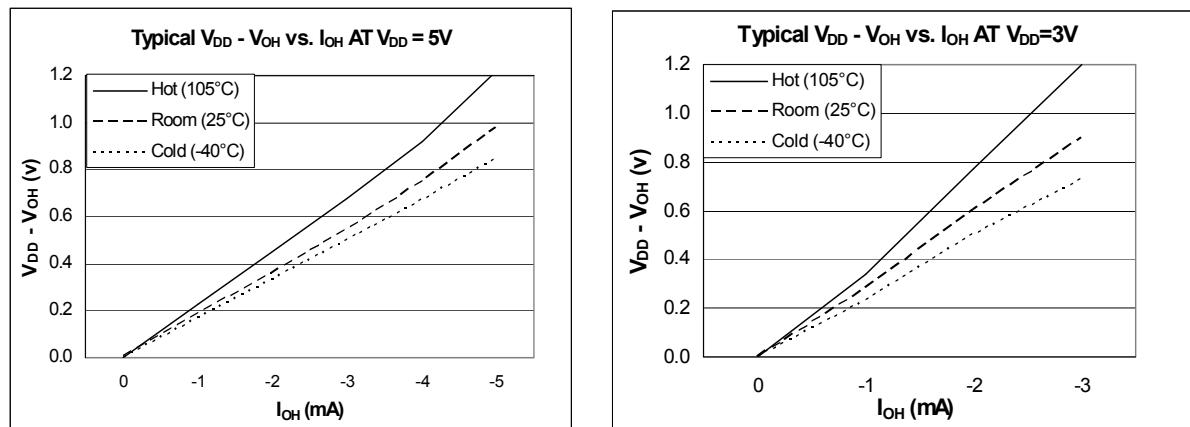


Figure 8. Typical High-side Drive (source) characteristics – Low Drive ( $PTxDSn = 0$ )

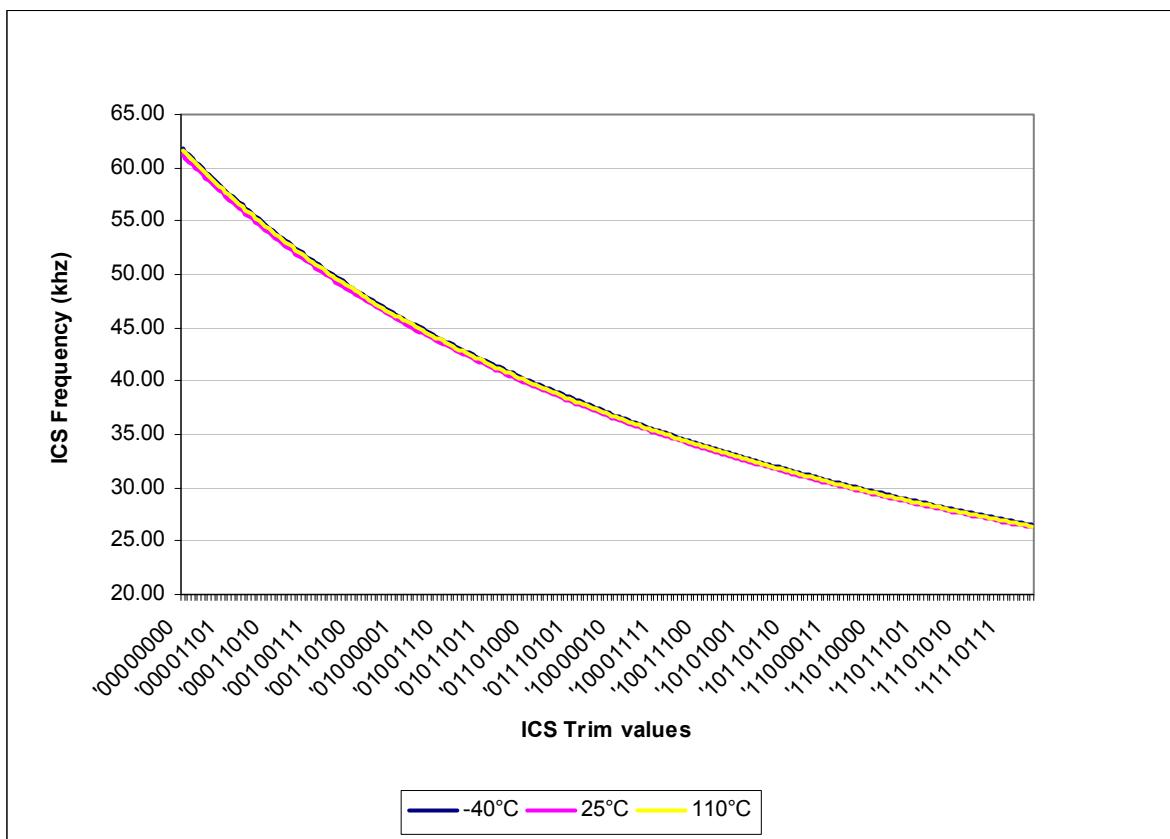
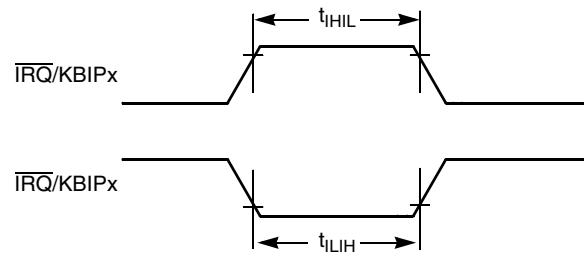


Figure 17. Internal Oscillator Deviation from Trimmed Frequency

## 2.10 ADC Characteristics

Table 12. 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ <sup>1</sup>	Max	Unit	Comment
Supply voltage	Absolute	$V_{DDAD}$	2.7	—	5.5	V	—
	Delta to $V_{DD}$ $(V_{DD} - V_{DDAD})^2$	$\Delta V_{DDAD}$	-100	0	+100	mV	—
Ground voltage	Delta to $V_{SS}$ $(V_{SS} - V_{SSAD})^2$	$\Delta V_{SSAD}$	-100	0	+100	mV	—
Ref Voltage High	—	$V_{REFH}$	—	—	—	V	$V_{REFH}$ shorted to $V_{DDAD}$
Ref Voltage Low	—	$V_{REFL}$	—	—	—	V	$V_{REFL}$ shorted to $V_{SSAD}$
Input Voltage	—	$V_{ADIN}$	$V_{REFL}$	—	$V_{REFH}$	V	—
Input Capacitance	—	$C_{ADIN}$	—	4.5	5.5	pF	—

Figure 20.  $\overline{\text{IRQ}}/\text{KBIPx}$  Timing

## 2.11.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 15. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	$f_{\text{TCLK}}$	0	$f_{\text{Bus}}/4$	Hz
2	D	External clock period	$t_{\text{TCLK}}$	4	—	$t_{\text{cyc}}$
3	D	External clock high time	$t_{\text{clkh}}$	1.5	—	$t_{\text{cyc}}$
4	D	External clock low time	$t_{\text{clkI}}$	1.5	—	$t_{\text{cyc}}$
5	D	Input capture pulse width	$t_{\text{ICPW}}$	1.5	—	$t_{\text{cyc}}$

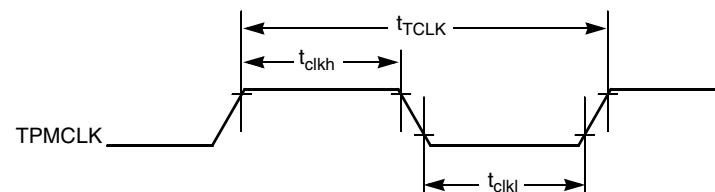


Figure 21. Timer External Clock

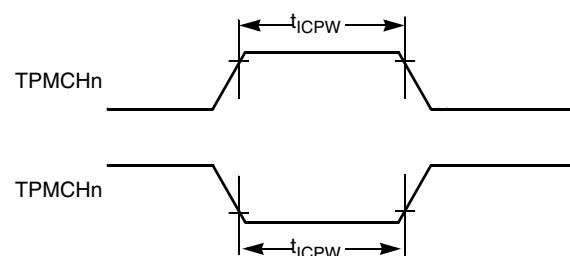
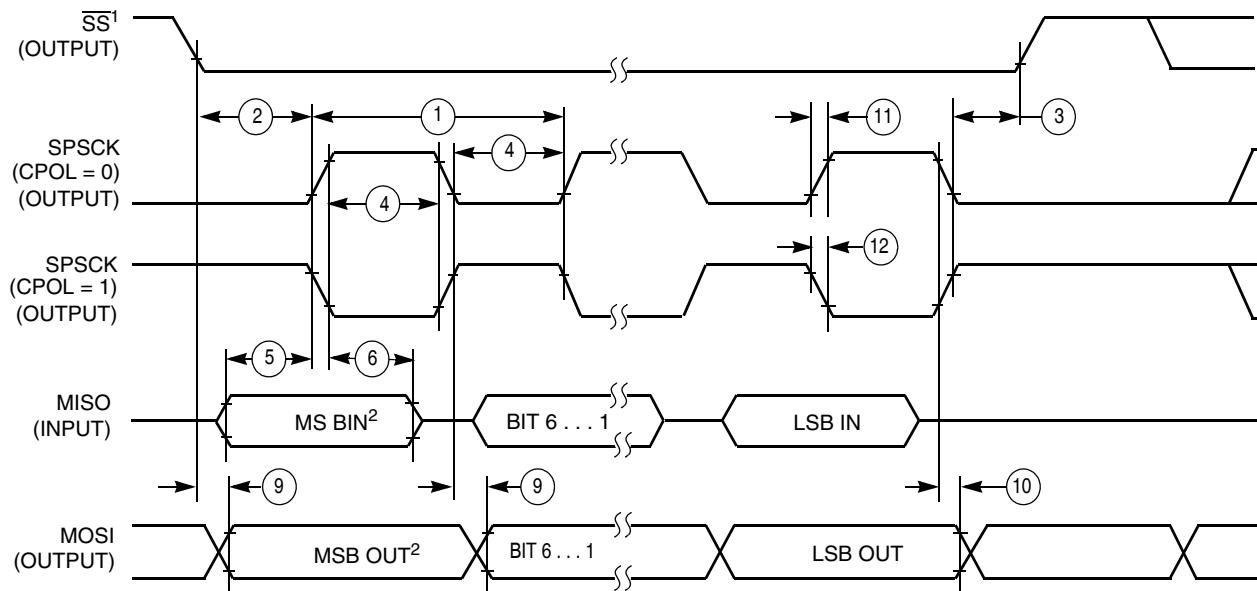


Figure 22. Timer Input Capture Pulse

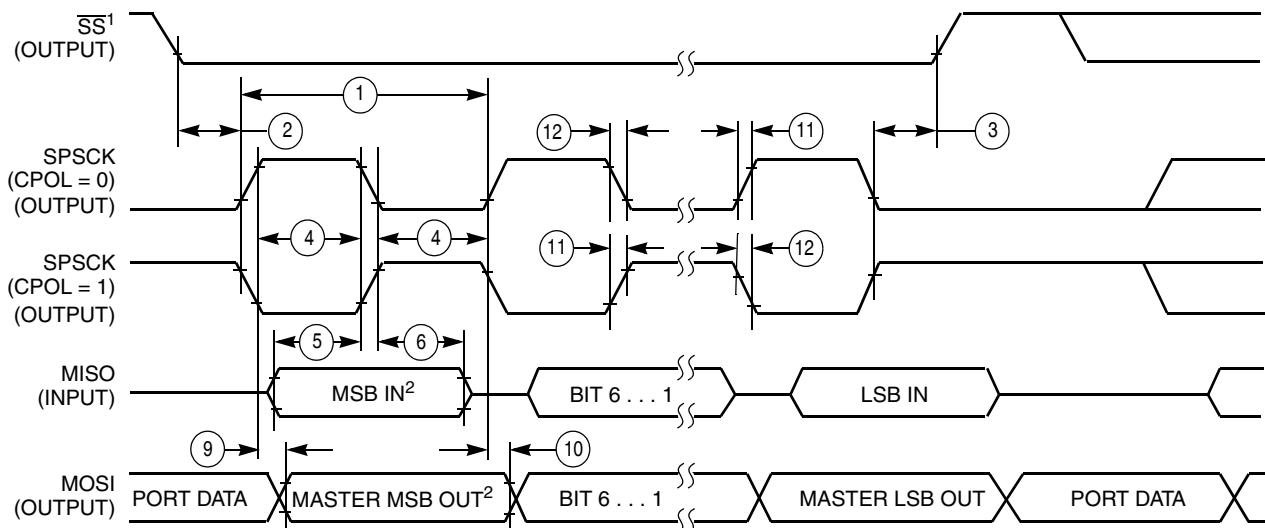
## Electrical Characteristics



## NOTES:

1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 23. SPI Master Timing (CPHA = 0)



## NOTES:

1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 24. SPI Master Timing (CPHA = 1)

## 2.12 LCD Specifications

**Table 17. LCD Electricals, 3 V Glass**

C	Characteristic	Symbol	Min	Typ	Max	Units
D	VLL3 Supply Voltage	VLL3	2.7	—	5.5	V
D	LCD Frame Frequency	f <sub>Frame</sub>	28	30	64	Hz
D	LCD Charge Pump Capacitance	C <sub>LCD</sub>	—	100	100	pF
D	LCD Bypass Capacitance	C <sub>BYLCD</sub>	—	100	100	
D	LCD Glass Capacitance	C <sub>glass</sub>	—	2000	8000	

## 2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V<sub>DD</sub> supply. For more detailed information about program/erase operations, see the Memory section.

**Table 18. Flash Characteristics**

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase –40 °C to 85 °C	V <sub>prog/erase</sub>	2.7		5.5	V
D	Supply voltage for read operation	V <sub>Read</sub>	2.7		5.5	V
D	Internal FCLK frequency <sup>1</sup>	f <sub>FCLK</sub>	150		200	kHz
D	Internal FCLK period (1/FCLK)	t <sub>Fcyc</sub>	5		6.67	μs
C	Byte program time (random location) <sup>2</sup>	t <sub>prog</sub>		9		t <sub>Fcyc</sub>
C	Byte program time (burst mode) <sup>2</sup>	t <sub>Burst</sub>		4		t <sub>Fcyc</sub>
C	Page erase time <sup>2</sup>	t <sub>Page</sub>		4000		t <sub>Fcyc</sub>
C	Mass erase time <sup>2</sup>	t <sub>Mass</sub>		20,000		t <sub>Fcyc</sub>
D	Byte program current <sup>3</sup>	I <sub>IDDBP</sub>	—	4	—	mA
D	Page erase current <sup>3</sup>	I <sub>IDDPE</sub>	—	6	—	mA
C	Program/erase endurance <sup>4</sup> T <sub>L</sub> to T <sub>H</sub> = –40 °C to + 85 °C T = 25 °C		10,000	— 100,000	— —	cycles
C	Data retention <sup>5</sup>	t <sub>D_ret</sub>	15	100	—	years

<sup>1</sup> The frequency of this clock is controlled by a software setting.

<sup>2</sup> These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

<sup>3</sup> The program and erase currents are additional to the standard run I<sub>DD</sub>. These values are measured at room temperatures with V<sub>DD</sub> = 5.0 V, bus frequency = 4.0 MHz.

<sup>4</sup> **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to *Engineering Bulletin EB619, Typical Endurance for Nonvolatile Memory*.

<sup>5</sup> **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25 °C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to *Engineering Bulletin EB618, Typical Data Retention for Nonvolatile Memory*.

**Ordering Information**

The susceptibility performance classification is described in [Table 21](#).

**Table 21. Susceptibility Performance Classification**

<b>Result</b>	<b>Performance Criteria</b>		
A	No failure	The MCU performs as designed during and after exposure.	
B	Self-recovering failure	The MCU does not perform as designed during exposure. The MCU returns automatically to normal operation after exposure is removed.	
C	Soft failure	The MCU does not perform as designed during exposure. The MCU does not return to normal operation until exposure is removed and the RESET pin is asserted.	
D	Hard failure	The MCU does not perform as designed during exposure. The MCU does not return to normal operation until exposure is removed and the power to the MCU is cycled.	
E	Damage	The MCU does not perform as designed during and after exposure. The MCU cannot be returned to proper operation due to physical damage or other permanent performance degradation.	

### 3 Ordering Information

This section contains ordering information for MC9S08LG32 and MC9S08LG16 devices.

**Table 22. Device Numbering System**

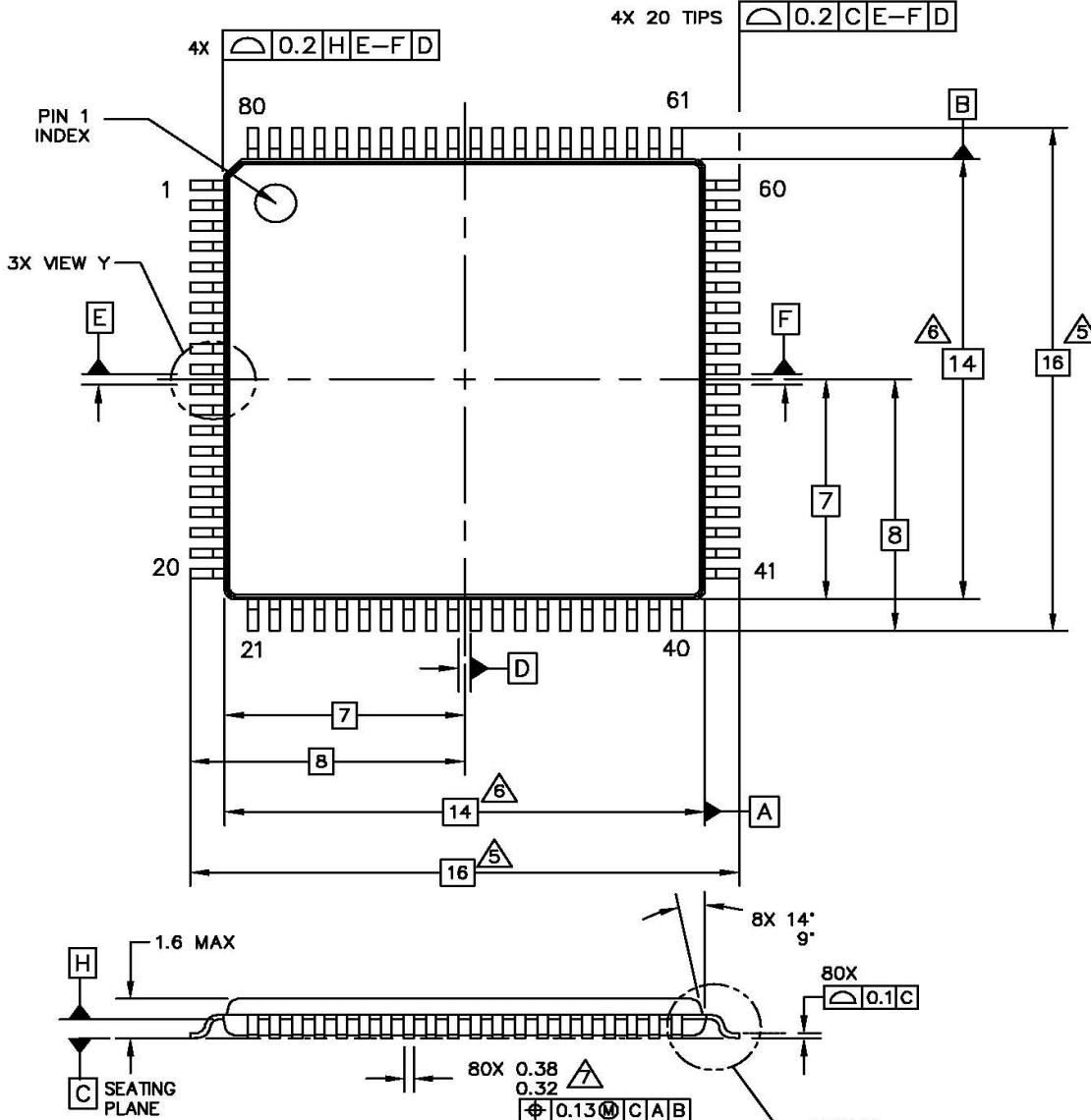
<b>Device Number<sup>1</sup></b>	<b>Memory</b>		<b>Temperature Range (°C)</b>	<b>LCD Mode Operation</b>	<b>Available Packages<sup>2</sup></b>
	<b>FLASH</b>	<b>RAM</b>			
<b>Auto</b>					
S9S08LG32J0CLK	32 KB	1984	-40 °C to +85 °C	Charge Pump	80-pin LQFP
S9S08LG32J0CLH					64-pin LQFP
S9S08LG32J0CLF					48-pin LQFP
S9S08LG32J0VLK	32 KB	1984	-40 °C to +105 °C	Register Bias	80-pin LQFP
S9S08LG32J0VLH					64-pin LQFP
S9S08LG32J0VLF					48-pin LQFP
S9S08LG16J0VLH	18 KB	1984			64-pin LQFP
S9S08LG16J0VLF					48-pin LQFP
<b>IMM</b>					
MC9S08LG32CLK	32 KB	1984	-40 °C to +85 °C	Charge Pump	80-pin LQFP
MC9S08LG32CLH					64-pin LQFP
MC9S08LG32CLF					48-pin LQFP
MC9S08LG16CLH	18 KB	1984			64-pin LQFP
MC9S08LG16CLF					48-pin LQFP

<sup>1</sup> See the *MC9S08LG32 Reference Manual* (document MC9S08LG32RM), for a complete description of modules included on each device.

<sup>2</sup> See [Table 23](#) for package information.

## Package Information

## 4.1.1 80-pin LQFP

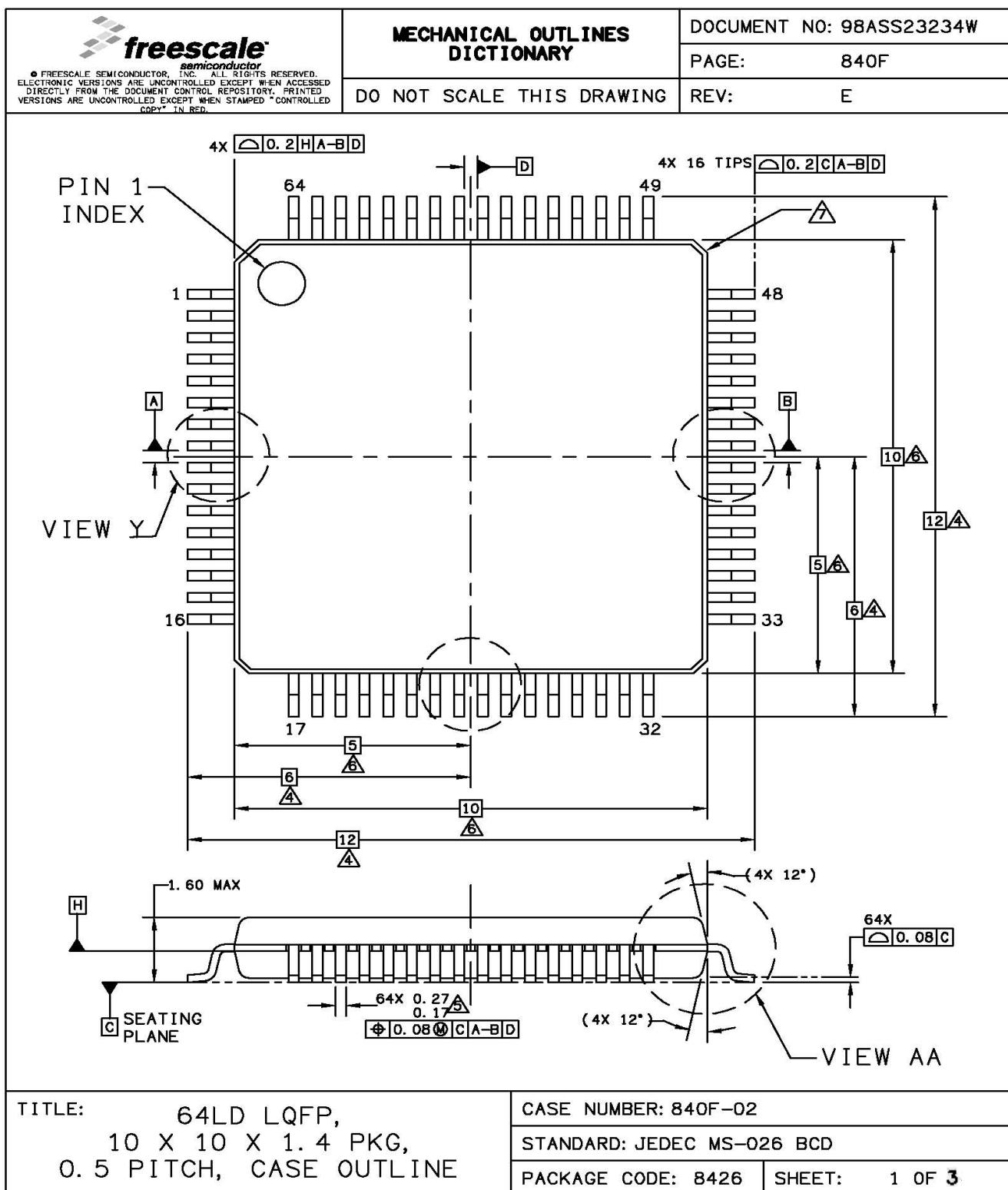
 <p>FREESCALE SEMICONDUCTOR. ALL RIGHTS RESERVED. ELECTRONIC VERSIONS ARE UNCONTROLLED EXCEPT WHEN ACCESSED DIRECTLY FROM THE DOCUMENT CONTROL REPOSITORY. PRINTED VERSIONS ARE UNCONTROLLED EXCEPT WHEN STAMPED "CONTROLLED COPY" IN RED.</p>	<b>MECHANICAL OUTLINES DICTIONARY</b>  DO NOT SCALE THIS DRAWING	DOCUMENT NO: 98ASS23237W	
		PAGE: 917A	
REV: E			
 <p>The diagram shows a top-down view of an 80-pin LQFP package. It features two rows of pins: a top row of 40 pins and a bottom row of 40 pins. Pin 1 is located at the bottom-left corner of the package. The package is 61 units wide and 60 units high. Pin numbers are indicated along the outer edges. Internal connection lines are shown for pins 7, 8, 14, 21, 40, 41, 6, 16, and 5. A seating plane is indicated at the bottom left. View K shows a cross-section of the lead frame with a thickness of 1.4 mm. Lead spacing is 0.38 mm, and lead width is 0.32 mm. Lead height is 0.13 mm. A note specifies a maximum height of 1.6 mm for the top surface. View Y shows the package from the side.</p>			
TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK		CASE NUMBER: 917A-03	
		STANDARD: FREESCALE	
		PACKAGE CODE: 8258 SHEET: 1 OF 3	

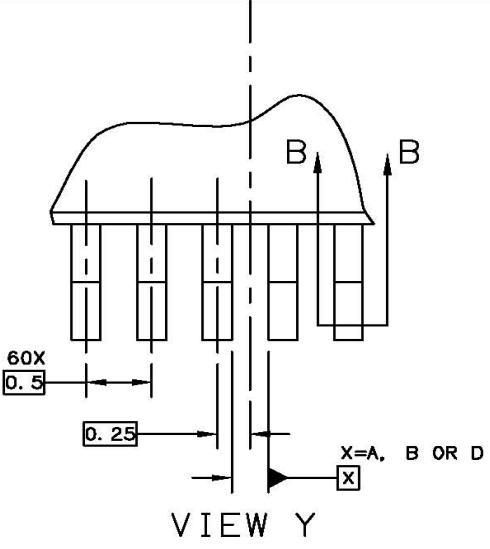
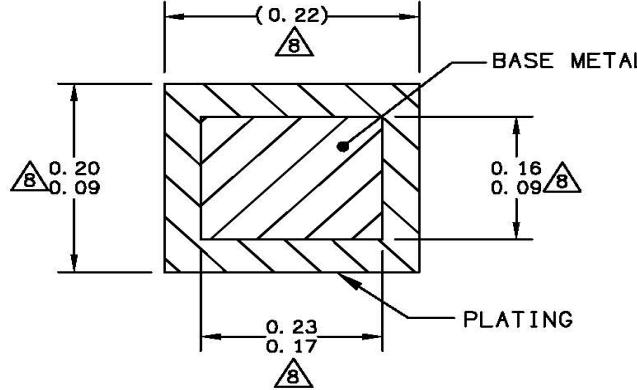
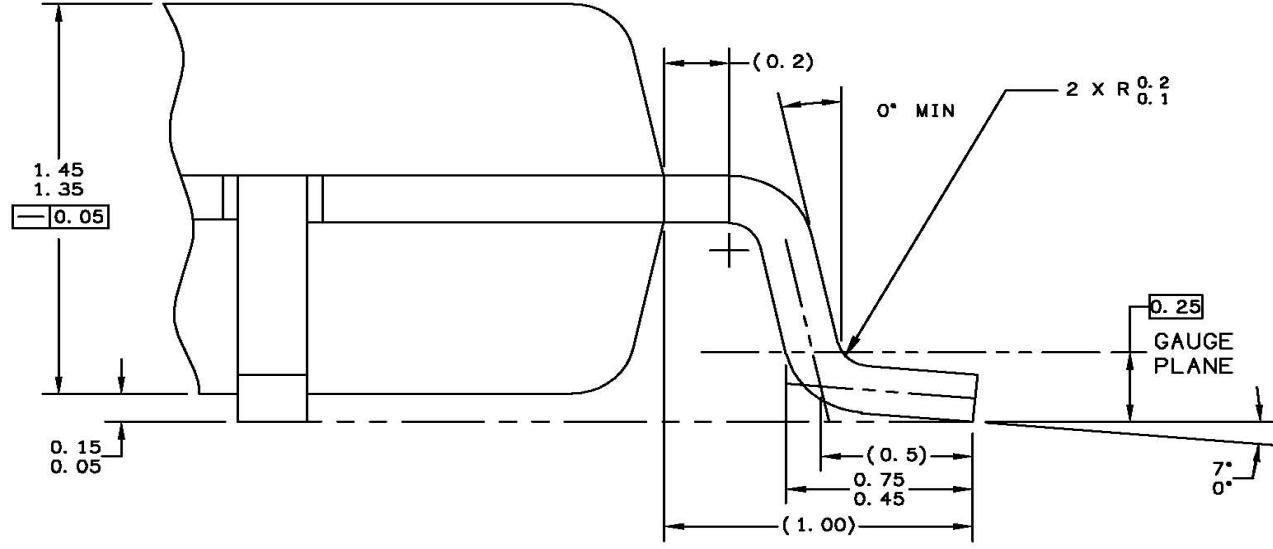
## Package Information

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	PAGE:	917A
DO NOT SCALE THIS DRAWING		REV: E
<b>NOTES:</b>		
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994. 2. CONTROLLING DIMENSION : MILLIMETER. 3. DATUM PLANE H IS LOCATED AT THE BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE. 4. DATUM E, F AND D TO BE DETERMINED AT DATUM PLANE H. <b>△</b> DIMENSIONS TO BE DETERMINED AT SEATING PLANE C. <b>△</b> DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H. <b>△</b> DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.		
<b>TITLE:</b> 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK		
CASE NUMBER: 917A-03 STANDARD: FREESCALE PACKAGE CODE: 8258    SHEET: 3 OF 3		

Figure 33. 80-pin LQFP Package Drawing (Case 917A, Doc #98ASS23237W)

## 4.1.2 64-pin LQFP



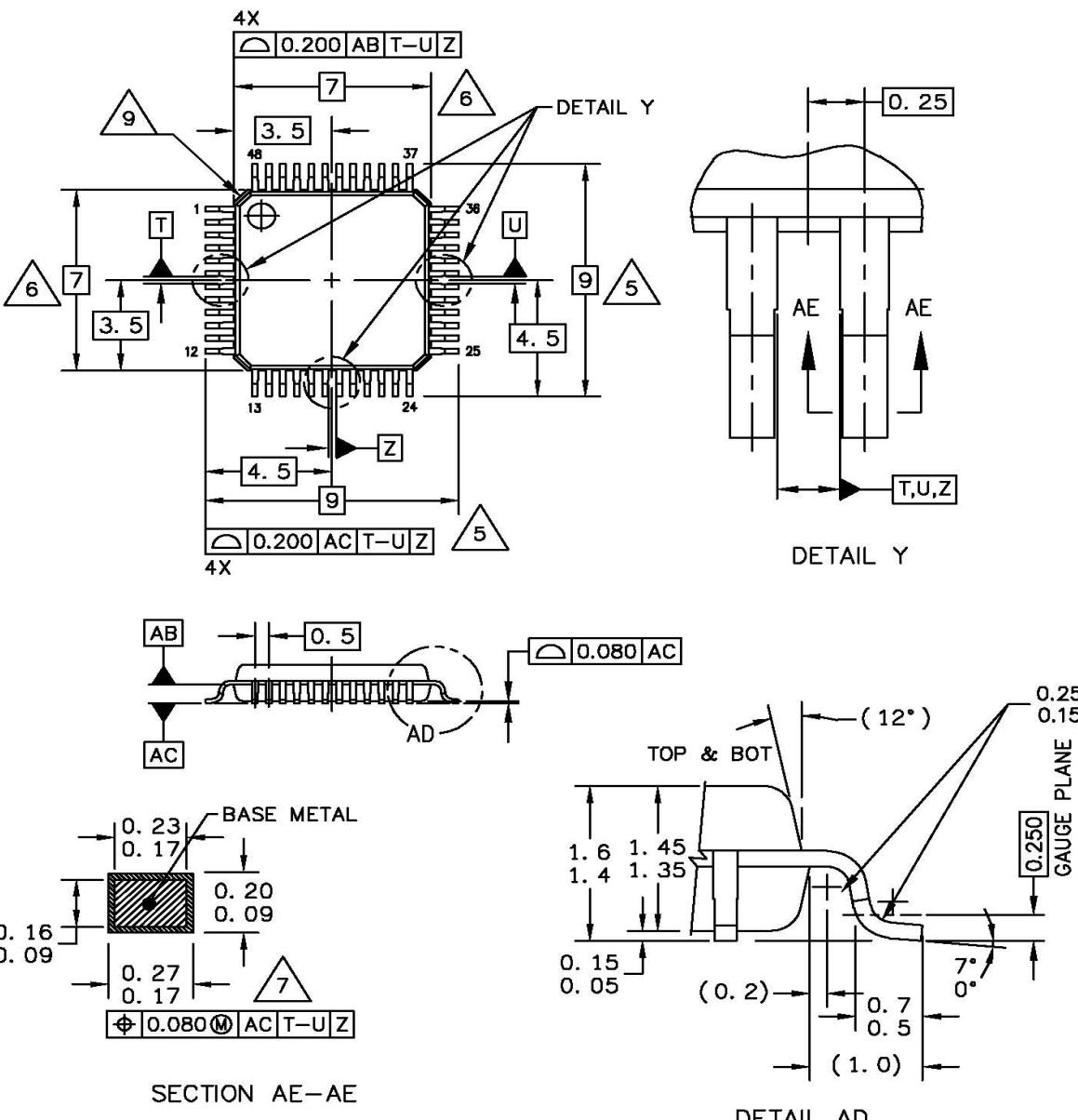
 <p>© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. ELECTRONIC VERSIONS ARE UNCONTROLLED EXCEPT WHEN ACCESSED DIRECTLY FROM THE DOCUMENTATION REPOSITORY. PRINTED VERSIONS ARE UNCONTROLLED EXCEPT WHEN STAMPED "CONTROLLED COPY" IN RED.</p>	<b>MECHANICAL OUTLINES DICTIONARY</b>  DO NOT SCALE THIS DRAWING	DOCUMENT NO: 98ASS23234W
		PAGE: 840F
		REV: E
	 <p>VIEW Y</p>	 <p>SECTION B-B</p>
	 <p>VIEW AA</p>	
TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F-02  STANDARD: JEDEC MS-026 BCD	PACKAGE CODE: 8426    SHEET: 2 OF 3

 <p><small>© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. ELECTRONIC VERSIONS ARE UNCONTROLLED EXCEPT WHEN ACCESSED DIRECTLY FROM THE DOCUMENT CONTROL REPOSITORY. PRINTED VERSIONS ARE UNCONTROLLED EXCEPT WHEN STAMPED "CONTROLLED COPY" IN RED.</small></p>	<b>MECHANICAL OUTLINES DICTIONARY</b>	DOCUMENT NO: 98ASS23234W
	PAGE: 840F	
DO NOT SCALE THIS DRAWING		REV: E
<b>NOTES:</b>		
<p>1. DIMENSIONS ARE IN MILLIMETERS.</p> <p>2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.</p> <p>3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.</p> <p><b>4.</b> DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.</p> <p><b>5.</b> THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.</p> <p><b>6.</b> THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.</p> <p><b>7.</b> EXACT SHAPE OF EACH CORNER IS OPTIONAL.</p> <p><b>8.</b> THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.</p>		
<b>TITLE:</b> 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE		<b>CASE NUMBER:</b> 840F-02 <b>STANDARD:</b> JEDEC MS-026 BCD <b>PACKAGE CODE:</b> 8426 <b>SHEET:</b> 3 OF 3

Figure 34. 64-pin LQFP Package Drawing (Case 840F, Doc #98ASS23234W)

## Package Information

## 4.1.3 48-pin LQFP

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		PAGE: 932
		REV: G
	 <p>The drawing shows a top view of the package with pin numbers 1 through 48. Pin 1 is at the bottom left. Pin numbers are grouped in sets of four along the perimeter. Pin 12 is on the left, 24 is on the right, 13 is at the bottom, and 25 is at the top. Pin 48 is at the top center. Pin 38 is at the top right. Pin 37 is at the top left. Pin 36 is at the bottom right. Pin 35 is at the bottom left. Pin 34 is at the top right. Pin 33 is at the top left. Pin 32 is at the bottom right. Pin 31 is at the bottom left. Pin 30 is at the top right. Pin 29 is at the top left. Pin 28 is at the bottom right. Pin 27 is at the bottom left. Pin 26 is at the top right. Pin 25 is at the top left. Pin 24 is at the bottom right. Pin 23 is at the bottom left. Pin 22 is at the top right. Pin 21 is at the top left. Pin 20 is at the bottom right. Pin 19 is at the bottom left. Pin 18 is at the top right. Pin 17 is at the top left. Pin 16 is at the bottom right. Pin 15 is at the bottom left. Pin 14 is at the top right. Pin 13 is at the top left. Pin 12 is at the bottom right. Pin 11 is at the bottom left. Pin 10 is at the top right. Pin 9 is at the top left. Pin 8 is at the bottom right. Pin 7 is at the bottom left. Pin 6 is at the top right. Pin 5 is at the top left. Pin 4 is at the bottom right. Pin 3 is at the bottom left. Pin 2 is at the top right. Pin 1 is at the top left.</p> <p>Detail Y shows a cross-section of the lead frame with dimensions: 0.200 AB T-U Z, 3.5, 7, 37, 6, 9, 4.5, 25, 4.5, 9, 5, 0.200 AC T-U Z, 4X, 0.25, AE, AE, T,U,Z.</p> <p>Section AE-AE shows a cross-section of the lead frame with dimensions: AB, 0.5, 0.080 AC, AD, AC, BASE METAL, 0.23, 0.17, 0.20, 0.09, 0.16, 0.09, 0.27, 0.17, 0.080 M AC T-U Z.</p> <p>Detail AD shows a cross-section of the lead frame with dimensions: TOP &amp; BOT, 1.6, 1.45, 1.35, 0.15, 0.05, (0.2), 0.7, 0.5, (1.0), 0.25, 0.15, 0.250 GAUGE PLANE, 7°, 0°.</p>	
TITLE: LQFP, 48 LEAD, 0.50 PITCH (7.0 X 7.0 X 1.4)	CASE NUMBER: 932-03 STANDARD: JEDEC MS-026-BBC PACKAGE CODE: 6089	SHEET: 1 OF 2

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		PAGE: 932	
DO NOT SCALE THIS DRAWING		REV: G	
<b>NOTES:</b>			
<ol style="list-style-type: none"> <li>1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M-1994.</li> <li>2. CONTROLLING DIMENSION: MILLIMETER.</li> <li>3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.</li> <li>4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.</li> </ol> <p> 5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE AC.</p> <p> 6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.</p> <p> 7. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.350.</p> <ol style="list-style-type: none"> <li>8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.</li> </ol> <p> 9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.</p>			
<b>TITLE:</b> LQFP, 48 LEAD, 0.50 PITCH (7.0 X 7.0 X 1.4)		CASE NUMBER: 932-03 STANDARD: JEDEC MS-026-BBC PACKAGE CODE: 6089    SHEET: 2 OF 2	

Figure 35. 48-pin LQFP Package Drawing (Case 932, Doc #98ASH00962A)