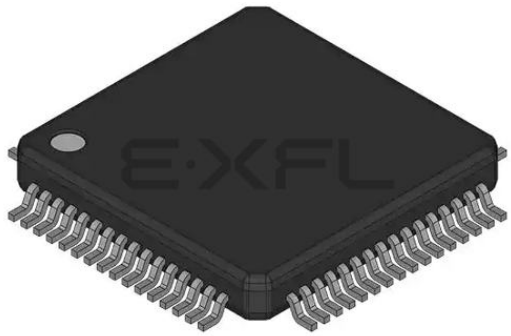

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.9K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s9s08lg32j0clh

Freescale Semiconductor, Inc.
Data Sheet Addendum

Document Number: MC9S08LG32AD
Rev. 0, 04/2015

Addendum to Rev. 9 of the MC9S08LG32 Series Covers: MC9S08LG32 and MC9S08LG16

This addendum identifies changes to Rev. 9 of the MC9S08LG32 Series data sheet (covering MC9S08LG32 and MC9S08LG16). The changes described in this addendum have not been implemented in the specified pages.

1 Add min values for I_{IC} (DC injection current)

Location:	Table 8. DC Characteristics, Page 14

In Table 8, “DC Characteristics,” add min values for I_{IC} (row number 14) as follows:

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
14	D	DC injection current [5, 6, 7] $V_{IN} < V_{SS}$ (min) $V_{IN} > V_{DD}$ (max)	Single pin limit	I_{IC}	**-0.2**	—	2	mA
			Total MCU limit, includes sum of all stressed pins		**-5**	—	25	mA

2 Change the max value of t_{LPO} (low power oscillator period)

Location:	Table 14. Control Timing, Page 29

In Table 14, “Control Timing,” change the max value of t_{LPO} (row number 2) from 1300 to 1500 µs.

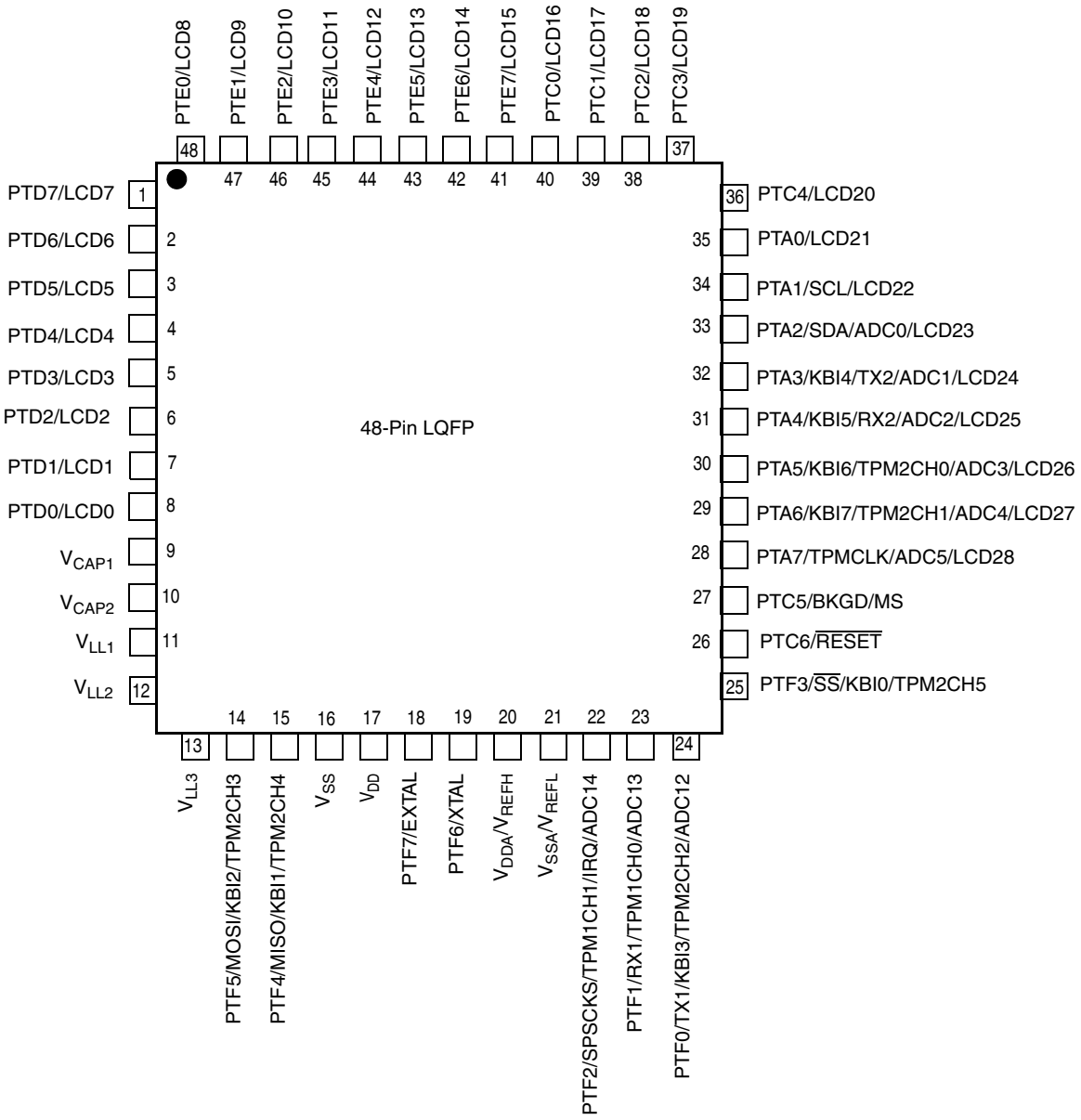


Figure 4. 48-Pin LQFP

NOTE

V_{REFH}/V_{REFL} are internally connected to V_{DDA}/V_{SSA}.

Table 2. Pin Availability by Package Pin-Count

Packages			<-- Lowest **Priority** --> Highest				
80	**64**	**48**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	1	1	PTD7	LCD7	—	—	—
2	2	2	PTD6	LCD6	—	—	—
3	3	3	PTD5	LCD5	—	—	—
4	4	4	PTD4	LCD4	—	—	—
5	5	5	PTD3	LCD3	—	—	—
6	6	6	PTD2	LCD2	—	—	—
7	7	—	PTB3	LCD32	—	—	—
8	8	—	PTB2	LCD31	—	—	—
9	—	—	PTB7	LCD40	—	—	—
10	—	—	PTB6	LCD39	—	—	—
11	—	—	PTB5	LCD38	—	—	—
12	—	—	PTB4	LCD37	—	—	—
13	9	—	PTB1	LCD30	—	—	—
14	10	—	PTB0	LCD29	—	—	—
15	11	7	PTD1	LCD1	—	—	—
16	12	8	PTD0	LCD0	—	—	—
17	13	9	V_{CAP1}	—	—	—	—
18	14	10	V_{CAP2}	—	—	—	—
19	15	11	V_{LL1}	—	—	—	—
20	16	12	V_{LL2}	—	—	—	—
21	17	13	V_{LL3}	—	—	—	—
22	18	14	PTF5	MOSI	KBI2	TPM2CH3	—
23	19	15	PTF4	MISO	KBI1	TPM2CH4	—
24	20	—	PTI5	TPM2CH0	SCL	$\overline{SS}$	—
25	21	—	PTI4	TPM2CH1	SDA	SPSCK	—
26	—	—	PTI3	TPM2CH2	MOSI	—	—
27	—	—	PTI2	TPM2CH3	MISO	—	—
28	—	—	PTI1	TMRCLK	TX2	—	—
29	—	—	PTI0	RX2	—	—	—
30	22	—	PTH7	KBI1	TPM2CH4	—	—
31	23	16	V_{SS}	—	—	—	—
32	24	17	V_{DD}	—	—	—	—
33	25	18	PTF7	EXTAL	—	—	—
34	26	19	PTF6	XTAL	—	—	—
35	27	20	V_{DDA}	V_{REFH}	—	—	—
36	28	21	V_{SSA}	V_{REFL}	—	—	—
37	29	—	PTH6	TPM2CH5	KBI0	ADC15	—
38	30	22	PTF2	SPSCK	TPM1CH1	IRQ	ADC14

Table 4. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25 ±2	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages and use the largest of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in an external power supply going out of regulation. Ensure that the external V_{DD} load will shunt current greater than maximum injection current, this will be of greater risk when the MCU is not consuming power. For instance, if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

2.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in On-Chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to +105	°C
Maximum junction temperature	T_J	125	°C
Thermal resistance Single-layer board 80-pin LQFP 64-pin LQFP 48-pin LQFP	θ_{JA}	 61 71 80	°C/W
Thermal resistance Four-layer board 80-pin LQFP 64-pin LQFP 48-pin LQFP	θ_{JA}	 48 52 56	°C/W

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

Table 9. Supply Current Characteristics (continued)

Num	C	Parameter		Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
6	T	Stop2 adders:	RTC using LPO	—	n/a	3	210	—	nA	–40 °C to 105 °C
			RTC using low power crystal oscillator				4.25	—	µA	
			LCD[2] with rbias (Low Gain)				1.2[3]	—		
			LCD[2] with rbias (High Gain)				18[4]	—		
			LCD[2] with Cpump				4.05[3]	—		–40 °C to 85 °C
			RTC using LPO			5	210	—	nA	–40 °C to 105 °C
			RTC using low power crystal oscillator				4.22	—	µA	
			LCD[2] with rbias (Low Gain)				1.5[3]	—		
			LCD[2] with rbias (High Gain)				32[4]	—		
			LCD[2] with Cpump				7.12[3]	—		–40 °C to 85 °C
7	T	Stop3 adders:	RTC using LPO	—	n/a	3	210	—	nA	–40 °C to 105 °C
			RTC using low power crystal oscillator				4.75	—	µA	
			LCD[2] with rbias (Low Gain)				1.2[3]	—		
			LCD[2] with rbias (High Gain)				18[4]	—		
			LCD[2] with Cpump				4.35[3]	—		–40 °C to 85 °C
			RTC using LPO			5	230	—	nA	–40 °C to 105 °C
			RTC using low power crystal oscillator				4.74	—	µA	
			LCD[2] with rbias (Low Gain)				1.5[3]	—		
			LCD[2] with rbias (High Gain)				32[4]	—		
			LCD[2] with Cpump				7.49[3]	—		–40 °C to 85 °C

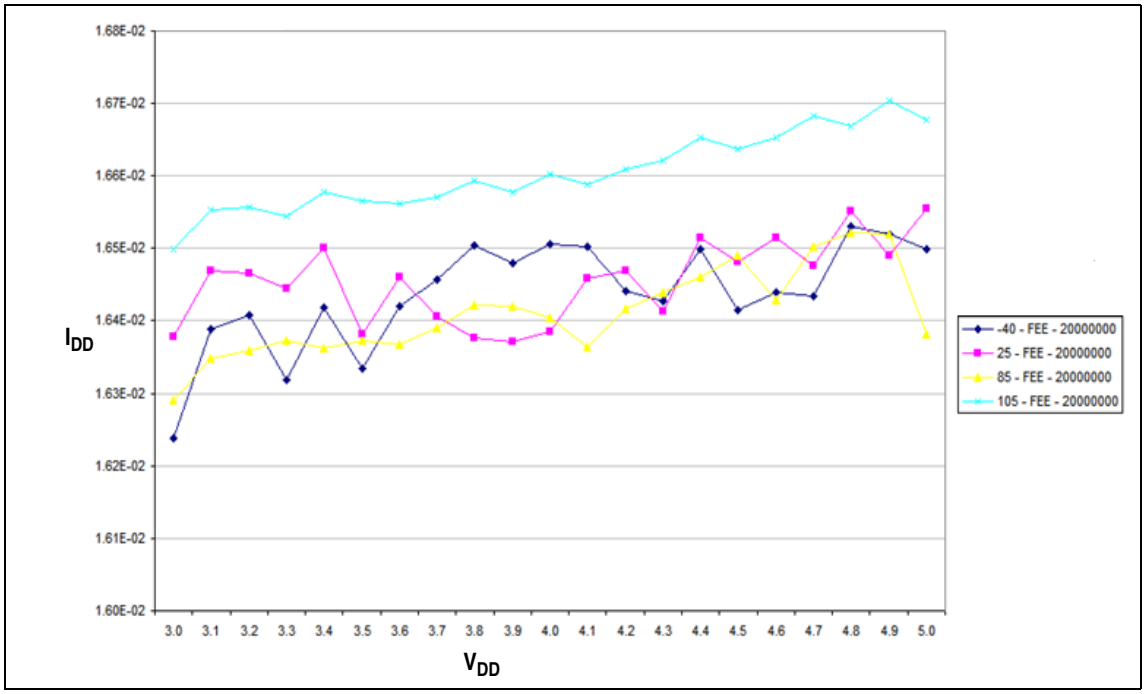


Figure 12. Typical Run I_{DD} for FEE Mode at 20 MHz

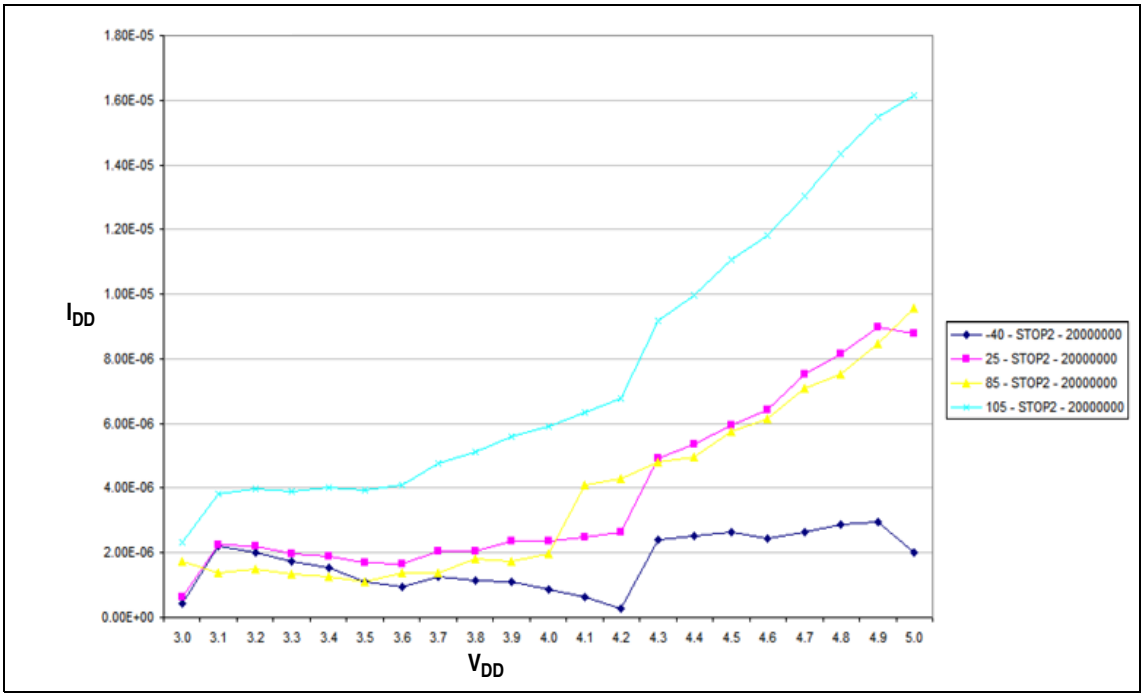


Figure 13. Typical Stop2 I_{DD}

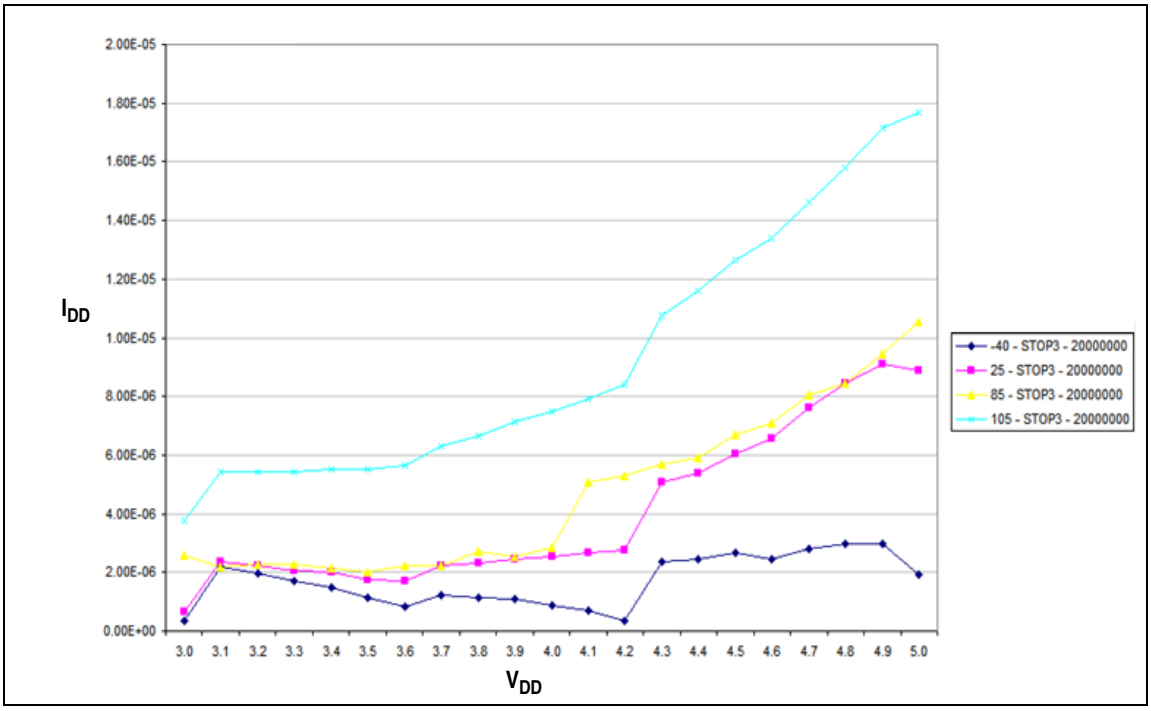


Figure 14. Typical Stop3 I_{DD}

2.8 External Oscillator (XOSC) Characteristics

Table 10. Oscillator Electrical Specifications (Temperature Range = –40 °C to 105 °C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	D	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) • Low range (RANGE = 0) • High range (RANGE = 1) FEE or FBE mode[2] • High range (RANGE = 1, HGO = 1) BLPE mode • High range (RANGE = 1, HGO = 0) BLPE mode	 f_{lo} f_{hi} f_{hi-hgo} f_{hi-lp}	 32 1 1 1	 — — — —	 38.4 5 16 8	 kHz MHz MHz MHz
2	D	Load capacitors	C_1 C_2	See crystal or resonator manufacturer's recommendation.			

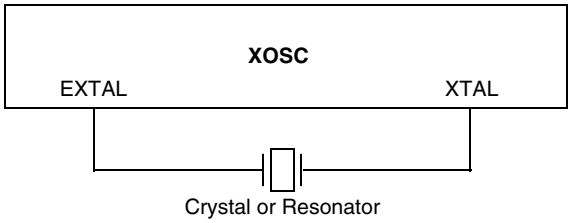


Figure 16. Typical Crystal or Resonator Circuit: Low Range/Low Power

2.9 Internal Clock Source (ICS) Characteristics

Table 11. ICS Frequency Specifications (Temperature Range = –40 °C to 105 °C Ambient)

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
1	P	Average internal reference frequency — factory trimmed at VDD = 5.0 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	C	Average internal reference frequency — user trimmed		f_{int_t}	31.25	—	39.0625	kHz
3	C	Internal reference start-up time		t_{IRST}	—	60	100	µs
4	P	DCO output frequency range — trimmed[2]	Low range (DRS = 00)	f_{dco_t}	16	—	20	MHz
	P		Mid range (DRS = 01)		32	—	40	
5	P	DCO output frequency[2] Reference = 32768 Hz and DMX32 = 1	Low range (DRS = 00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DRS = 01)		—	39.85	—	
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)[3]		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)[3]		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	P	Total deviation of trimmed DCO output frequency over voltage and temperature		Δf_{dco_t}	—	–1.0 to +0.5	±2	$\%f_{dco}$
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 °C to 70 °C[3]		Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	C	FLL acquisition time[3, 4]		$t_{Acquire}$	—	—	1	mS
11	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[5]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This parameter is characterized and not tested on each device.

4 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

5 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in the crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

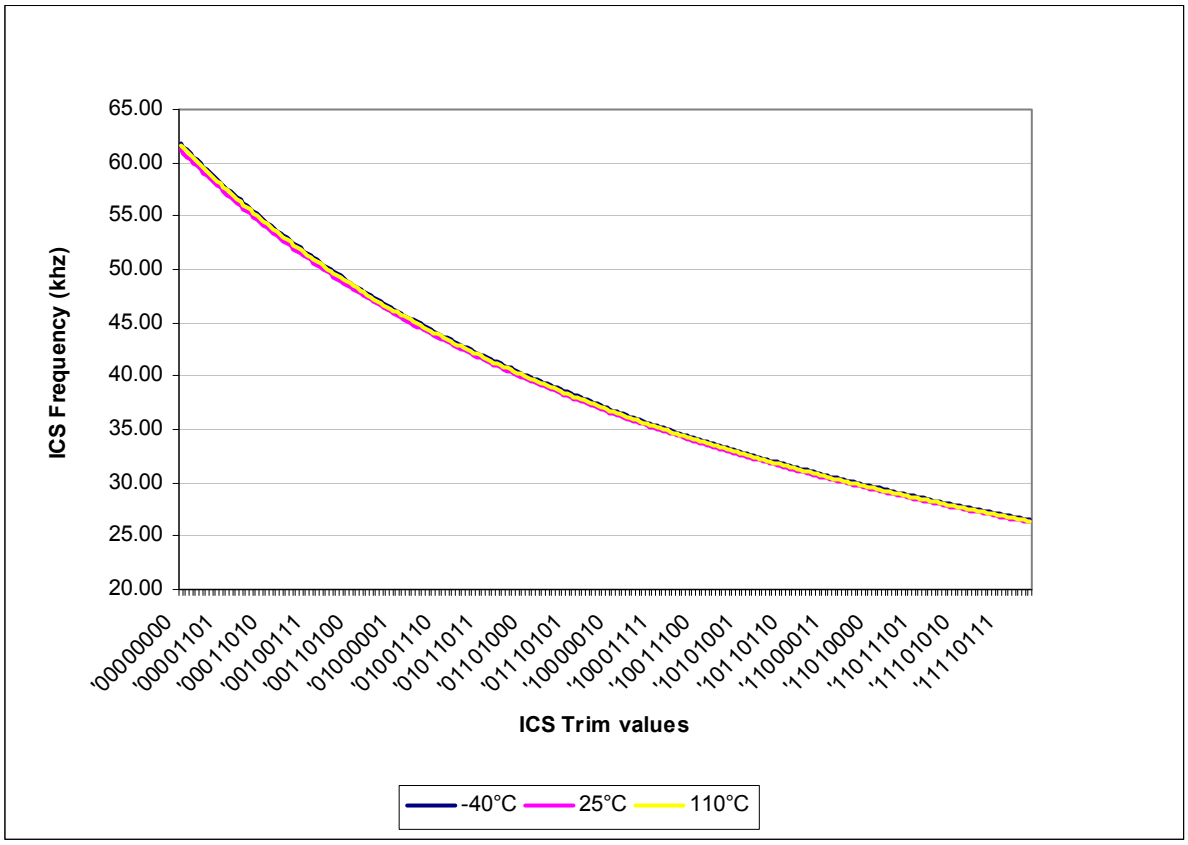


Figure 17. Internal Oscillator Deviation from Trimmed Frequency

2.10 ADC Characteristics

Table 12. 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDAD}	2.7	—	5.5	V	—
	Delta to V_{DD} ($V_{DD} - V_{DDAD}$)[2]	ΔV_{DDAD}	–100	0	+100	mV	—
Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSAD}$)[2]	ΔV_{SSAD}	–100	0	+100	mV	—
Ref Voltage High	—	V_{REFH}	—	—	—	V	V_{REFH} shorted to V_{DDAD}
Ref Voltage Low	—	V_{REFL}	—	—	—	V	V_{REFL} shorted to V_{SSAD}
Input Voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
Input Capacitance	—	C_{ADIN}	—	4.5	5.5	pF	—

Table 12. 12-bit ADC Operating Conditions (continued)

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Input Resistance	—	R_{ADIN}	—	5	7	kΩ	—
Analog Source Resistance	12-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
	10-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz		 — —	 — —	 5 10		
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC Conversion Clock Freq.	High Speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low Power (ADLPC = 1)		0.4	—	4.0		

1 Typical values assume V_{DDAD} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

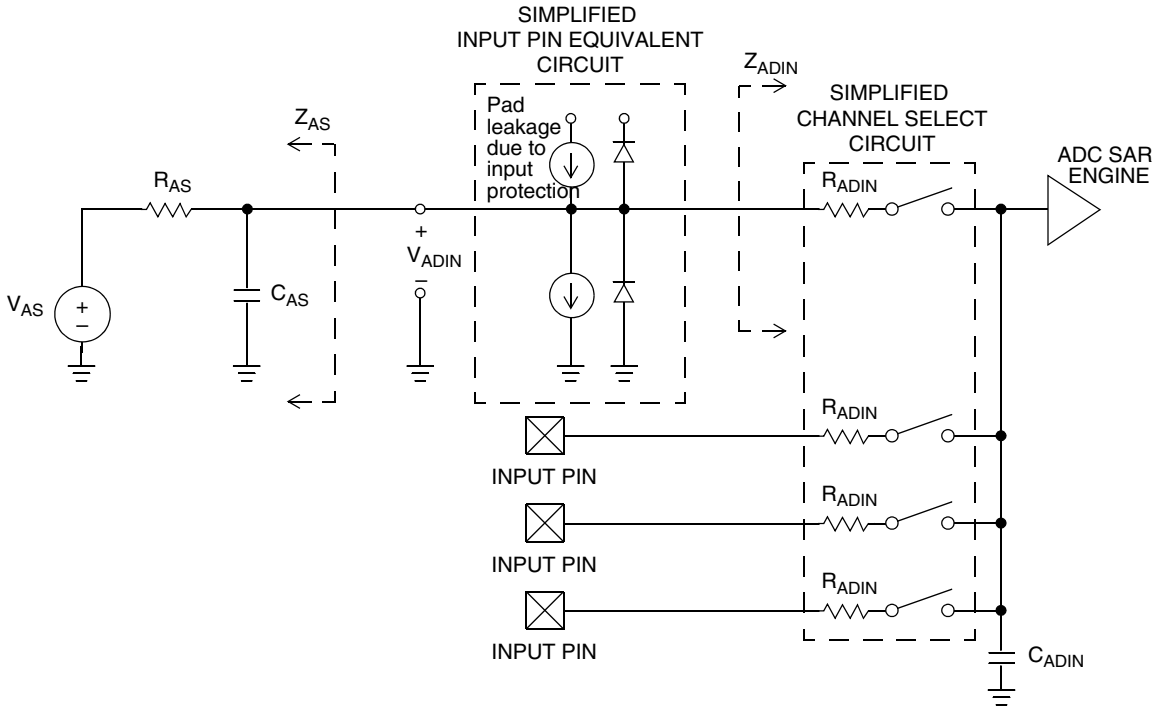


Figure 18. ADC Input Impedance Equivalency Diagram

Table 13. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD})

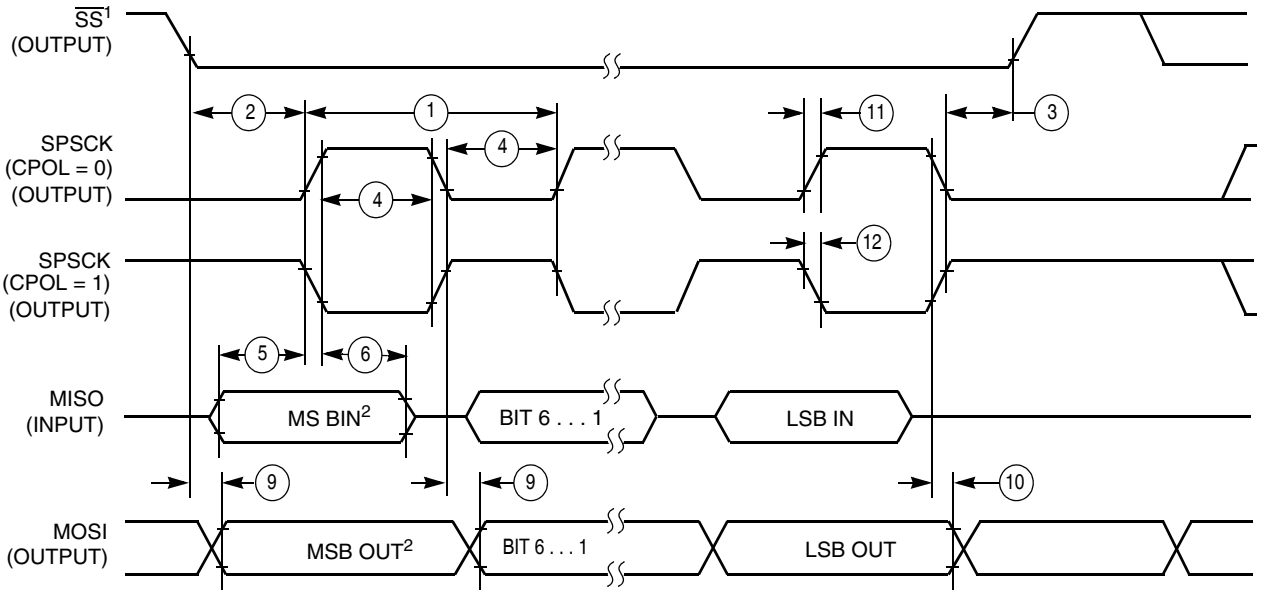
Num	C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
1	T	Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1	—	I_{DDAD}	—	195	—	µA	—
2	T	Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1	—	I_{DDAD}	—	347	—	µA	—
3	T	Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1	—	I_{DDAD}	—	407	—	µA	—
4	P	Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1	—	I_{DDAD}	—	0.755	1	mA	—
5	—	Supply Current	Stop, Reset, Module Off	IDDAD		0.011	1	µA	—
6	P	ADC Asynchronous Clock Source	High Speed (ADLPC=0)	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
			Low Power (ADLPC=1)		1.25	2	3.3		
7	C	Conversion Time (Including sample time)	Short sample (ADLSMP=0)	t_{ADC}	—	20	—	ADCK cycles	See *ADC chapter in the LG32 Reference Manual* for conversion time variances
			Long sample (ADLSMP=1)		—	40	—		
8	C	Sample Time	Short sample (ADLSMP=0)	t_{ADS}	—	3.5	—	ADCK cycles	
			Long sample (ADLSMP=1)		—	23.5	—		
9	T	Total Unadjusted Error	12-bit mode	E_{TUE}	—	±3.0	—	LSB^2	Includes quantization
	P		10-bit mode		—	±1	±2.5		
	T		8-bit mode		—	±0.5	±1		
10	T	Differential Non-Linearity	12-bit mode	DNL	—	±1.75	—	LSB^2	
	P		10-bit mode[3]		—	±0.5	±1.0		
	T		8-bit mode[3]		—	±0.3	±0.5		
11	T	Integral Non-Linearity	12-bit mode	INL	—	±1.5	—	LSB^2	
	P		10-bit mode		—	±0.5	±1		
	T		8-bit mode		—	±0.3	±0.5		
12	T	Zero-Scale Error	12-bit mode	E_{ZS}	—	±1.5	—	LSB^2	V_{ADIN} = V_{SSAD}
	P		10-bit mode		—	±0.5	±1.5		
	T		8-bit mode		—	±0.5	±0.5		

2.11.3 SPI Timing

Table 16 and Figure 23 through Figure 26 describe the timing requirements for the SPI system.

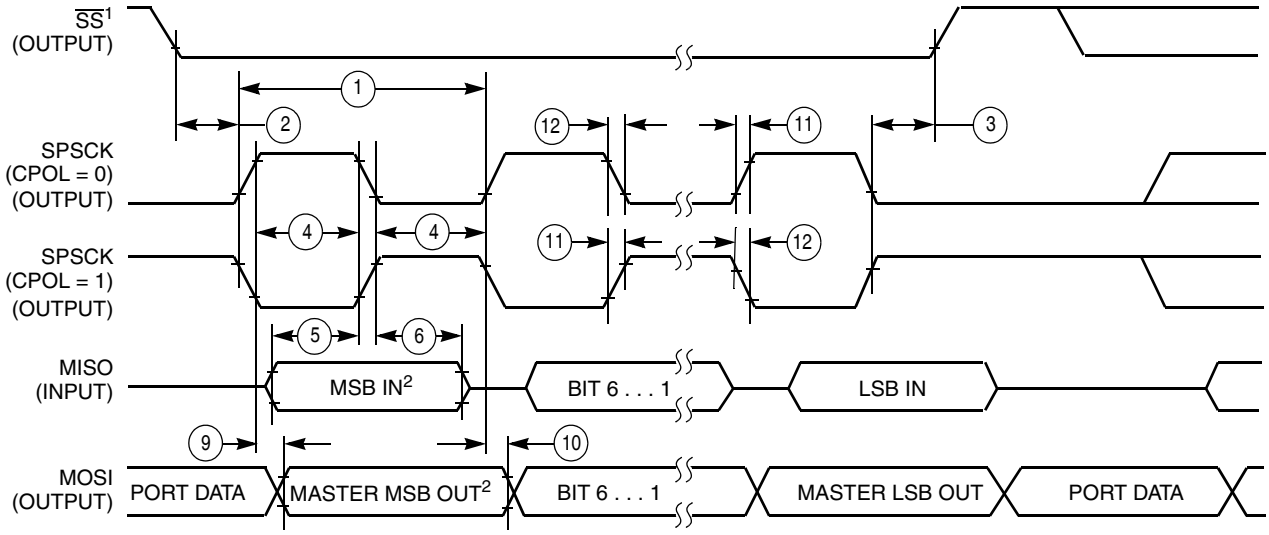
Table 16. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	 $f_{Bus}/2048$ 0	 $f_{Bus}/2$ $f_{Bus}/4$	Hz
①	D	SPSCK period Master Slave	t_{SPSCK}	 2 4	 2048 —	 t_{cyc} t_{cyc}
②	D	Enable lead time Master Slave	t_{Lead}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}
③	D	Enable lag time Master Slave	t_{Lag}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}
④	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	 $t_{cyc} - 30$ $t_{cyc} - 30$	 1024 t_{cyc} —	 ns ns
⑤	D	Data setup time (inputs) Master Slave	t_{SU}	 15 15	 — —	 ns ns
⑥	D	Data hold time (inputs) Master Slave	t_{HI}	 0 25	 — —	 ns ns
⑦	D	Slave access time	t_a	—	1	t_{cyc}
⑧	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
⑨	D	Data valid (after SPSCK edge) Master Slave	t_v	 — —	 25 25	 ns ns
⑩	D	Data hold time (outputs) Master Slave	t_{HO}	 0 0	 — —	 ns ns
⑪	D	Rise time Input Output	 t_{RI} t_{RO}	 — —	 $t_{cyc} - 25$ 25	 ns ns
⑫	D	Fall time Input Output	 t_{FI} t_{FO}	 — —	 $t_{cyc} - 25$ 25	 ns ns



NOTES:
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 23. SPI Master Timing (CPHA = 0)



NOTES:
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 24. SPI Master Timing (CPHA =1)

2.12 LCD Specifications

Table 17. LCD Electricals, 3 V Glass

C	Characteristic	Symbol	Min	Typ	Max	Units
D	VLL3 Supply Voltage	VLL3	2.7	—	5.5	V
D	LCD Frame Frequency	f_{Frame}	28	30	64	Hz
D	LCD Charge Pump Capacitance	C_{LCD}	—	100	100	pF
D	LCD Bypass Capacitance	C_{BYLCD}	—	100	100	
D	LCD Glass Capacitance	C_{glass}	—	2000	8000	

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

Table 18. Flash Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase –40 °C to 85 °C	$V_{prog/erase}$	2.7		5.5	V
D	Supply voltage for read operation	V_{Read}	2.7		5.5	V
D	Internal FCLK frequency[1]	f_{FCLK}	150		200	kHz
D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	µs
C	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}
C	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}
C	Page erase time[2]	t_{Page}	4000			t_{Fcyc}
C	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}
D	Byte program current[3]	R_{IDDBP}	—	4	—	mA
D	Page erase current[3]	R_{IDDPE}	—	6	—	mA
C	Program/erase endurance[4] T_L to T_H = –40 °C to + 85 °C T = 25 °C		10,000	— 100,000	— —	cycles
C	Data retention[5]	t_{D_ret}	15	100	—	years

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 5.0 V, bus frequency = 4.0 MHz.

4 **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to *Engineering Bulletin EB619, Typical Endurance for Nonvolatile Memory.*

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25 °C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to *Engineering Bulletin EB618, Typical Data Retention for Nonvolatile Memory.*

3 Except pins PHT1, PTH2, PTH3, PTH4, PTH5. See figures below for values.
4 Except pins PTF3, PTH5, PTH4, PHT0, Reset, and BKGD. See figures below for values.

Individual performance of each pin is shown in Figure 27, Figure 28, Figure 29, and Figure 30.

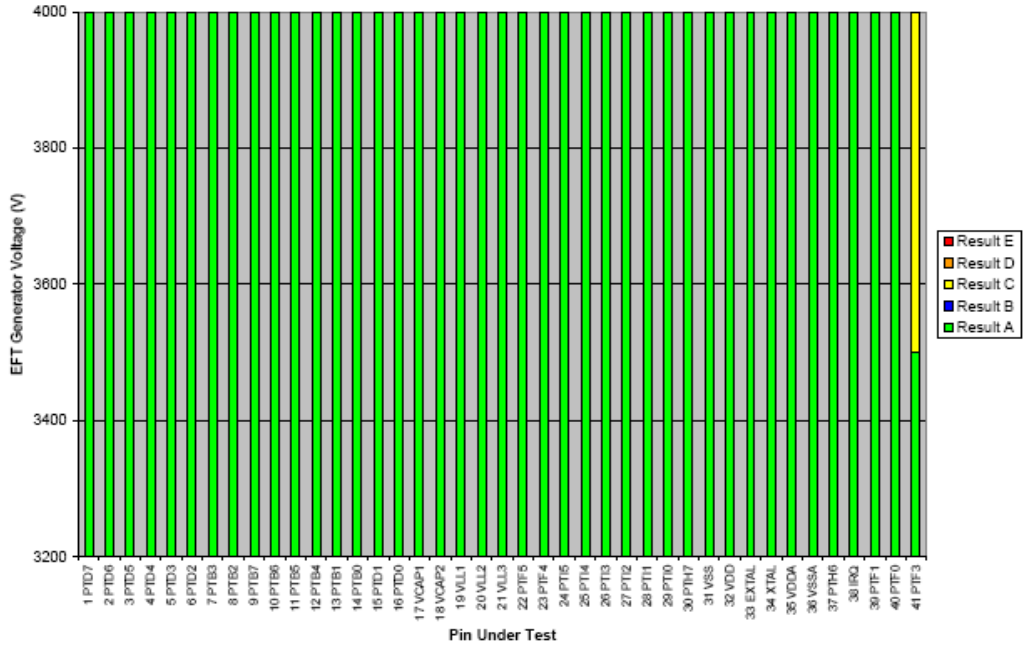
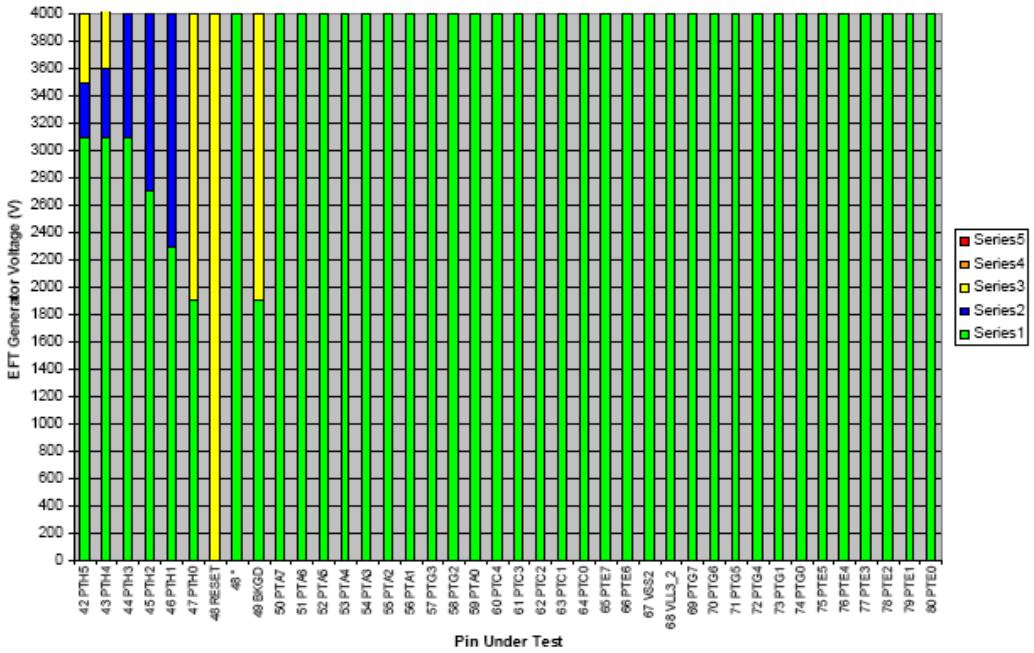


Figure 27. 4 MHz, Positive Polarity Pins 1 – 41



Note:
RESET retested with 0.1 μF capacitor from pin to ground is Class A compliant as shown by 48*.

Figure 28. 4 MHz, Positive Polarity Pins 42 – 80

3.1 Device Numbering System

Example of the device numbering system:

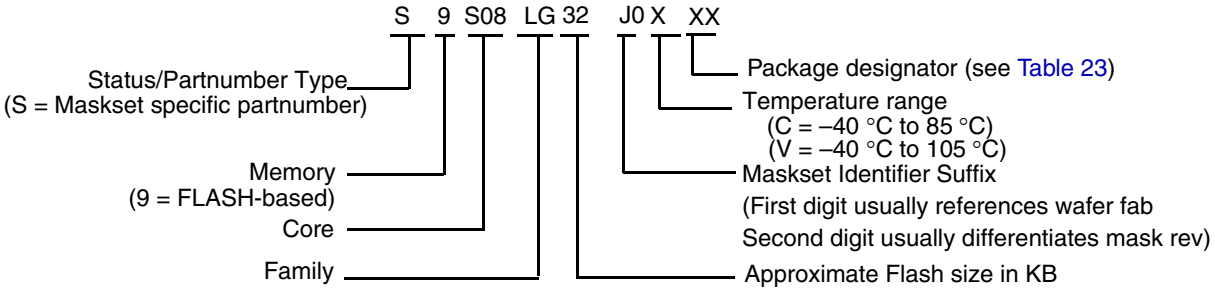


Figure 31. Device Number Example for Auto Parts

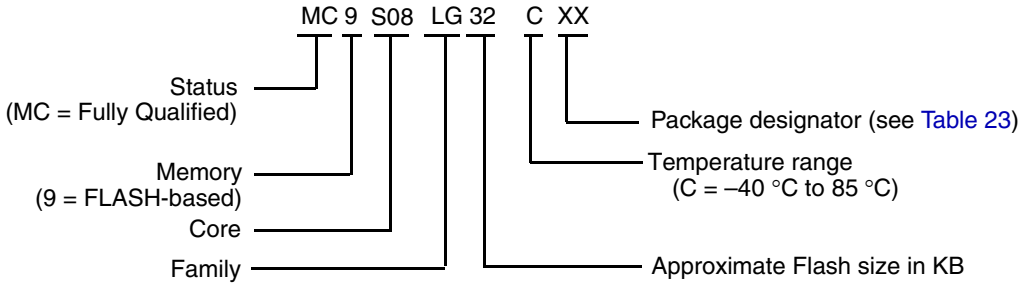


Figure 32. Device Number Example for IMM Parts

4 Package Information

Table 23. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
80	Low Quad Flat Package	LQFP	LK	917A	98ASS23237W
64	Low Quad Flat Package	LQFP	LH	840F	98ASS23234W
48	Low Quad Flat Package	LQFP	LF	932	98ASH00962A

4.1 Mechanical Drawings

The following pages are mechanical drawings for the packages described in Table 23. For the latest available drawings please visit our web site (http://www.freescale.com) and enter the package's document number into the keyword search box.

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23237W
		PAGE: 917A
	DO NOT SCALE THIS DRAWING	REV: E

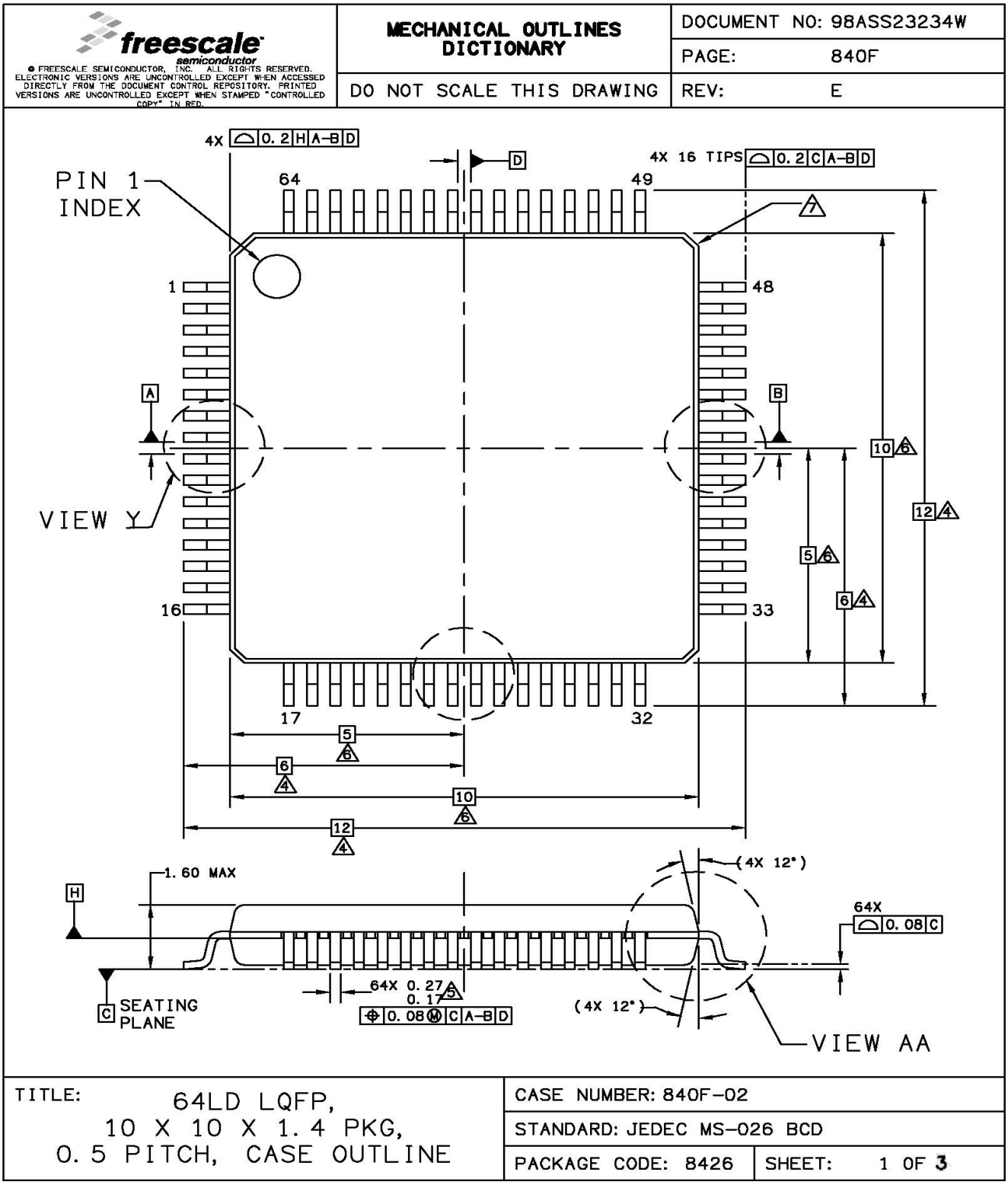
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION : MILIMETER.
3. DATUM PLANE H IS LOCATED AT THE BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUM E, F AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

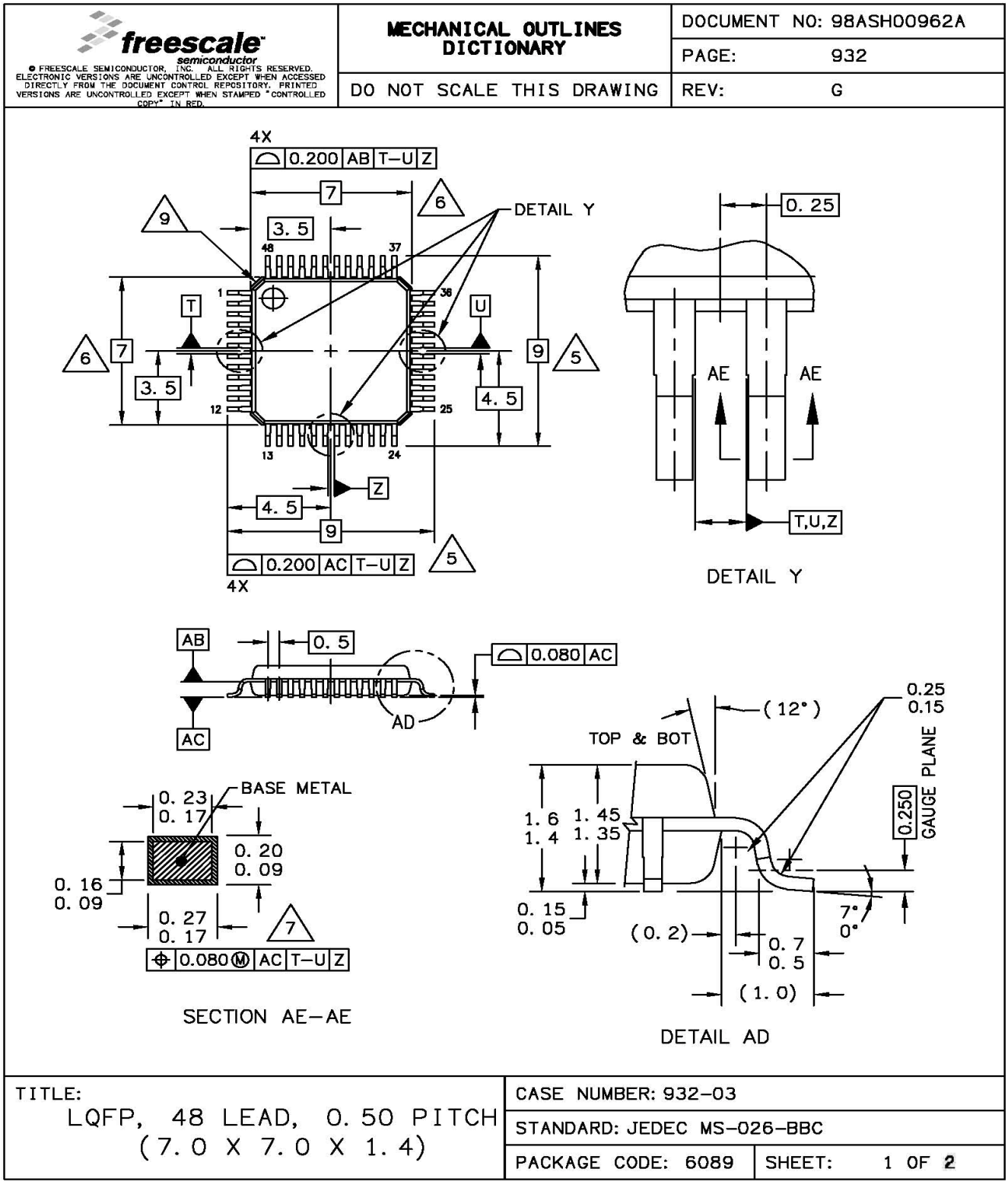
TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	CASE NUMBER: 917A–03	
	STANDARD: FREESCALE	
	PACKAGE CODE: 8258	SHEET: 3 OF 3

Figure 33. 80-pin LQFP Package Drawing (Case 917A, Doc #98ASS23237W)

4.1.2 64-pin LQFP



4.1.3 48-pin LQFP



5 Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web are the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://www.freescale.com

The following revision history table summarizes changes contained in this document.

Table 24. Revision History

Revision	Date	Description of Changes
1	8/2008	First Initial release.
2	9/2008	Second Initial Release.
3	11/2008	Alpha Customer Release.
4	2/2009	Launch Release.
5	4/2009	Added EMC Radiated Emission and Transient Susceptibility data in Table 19 and Table 20.
6	4/2009	Updated EMC performance data.
7	8/2009	Updated auto part numbers, changed TCLK, T0CH0, T0CH1, T1CH0, T1CH1, T1CH2, T1CH3, T1CH3, T1CH4, and T1CH5 to TPMCLK, TPM0CH0, TPM0CH1,TPM1CH0, TPM1CH1, TPM1CH2, TPM1CH3, TPM1CH4, and TPM1CH5, and changed the maximum LCD frame frequency to 64 Hz.
8	8/2011	Updated Table “ICS Frequency Specifications (Temperature Range = –40 ×C to 105 ×C Ambient)”. Changed the value of row 8 column C from C to P.
9	9/2011	Updated Table “ICS Frequency Specifications (Temperature Range = –40 ×C to 105 ×C Ambient)”. Removed Footnote from Row 8. Updated the Revision History