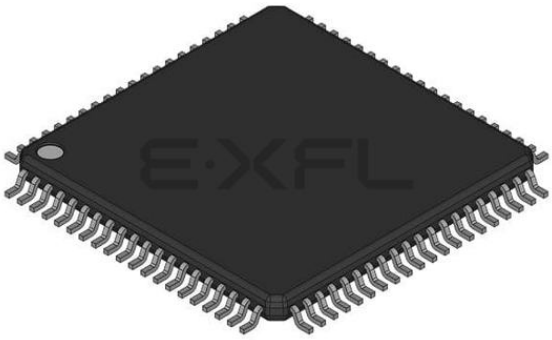

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.9K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s9s08lg32j0clk

Table 1. MC9S08LG32 Series Features by MCU and Package

Feature	MC9S08LG32			MC9S08LG16	
Flash size (bytes)	32,768			18,432	
RAM size (bytes)	1984				
Pin quantity	80	64	48	64	48
ADC	16 ch	12 ch	9 ch	12 ch	9 ch
LCD	8 x 37 4 x 41	8 x 29 4 x 33	8 x 21 4 x 25	8 x 29 4 x 33	8 x 21 4 x 25
ICE + DBG	yes				
ICS	yes				
IIC	yes				
IRQ	yes				
KBI	8 pin				
GPIOs	69	53	39	53	39
RTC	yes				
MTIM	yes				
SCI1	yes				
SCI2	yes				
SPI	yes				
TPM1 channels	2				
TPM2 channels	6				
XOSC	yes				

1 Pin Assignments

This section shows the pin assignments for the MC9S08LG32 series devices. The priority of functions on a pin is in ascending order from left to right and bottom to top. Another view of pinouts and function priority is given in Table 2.

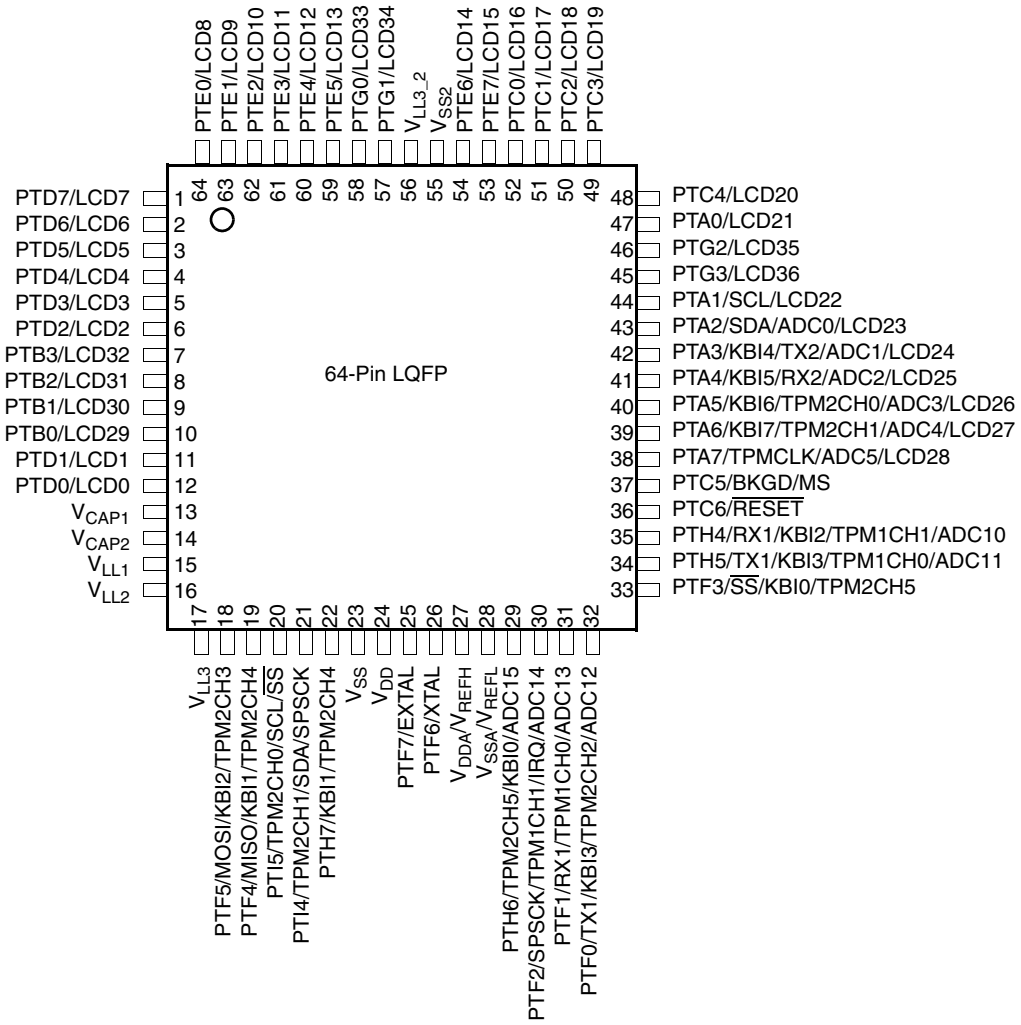


Figure 3. 64-Pin LQFP

NOTE

V_{REFH}/V_{REFL} are internally connected to V_{DDA}/V_{SSA}.

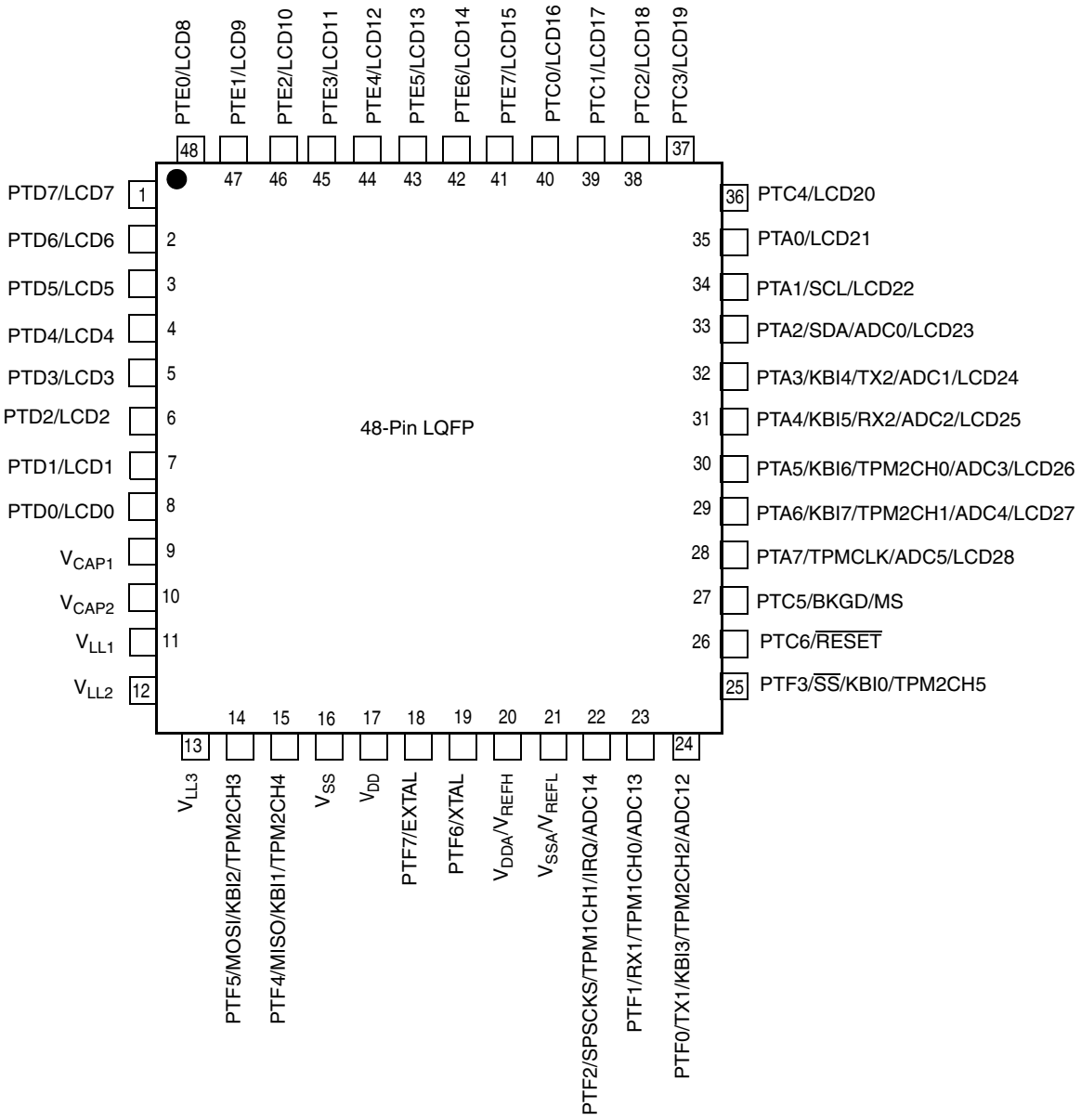


Figure 4. 48-Pin LQFP

NOTE

V_{REFH}/V_{REFL} are internally connected to V_{DDA}/V_{SSA}.

Table 2. Pin Availability by Package Pin-Count (continued)

Packages			<-- Lowest **Priority** --> Highest				
80	**64**	**48**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
39	31	23	PTF1	RX1	TPM1CH0	ADC13	—
40	32	24	PTF0	TX1	KBI3	TPM2CH2	ADC12
41	33	25	PTF3	$\overline{SS}$	KBI0	TPM2CH5	—
42	34	—	PTH5	TX1	KBI3	TPM1CH0	ADC11
43	35	—	PTH4	RX1	KBI2	TPM1CH1	ADC10
44	—	—	PTH3	KBI7	ADC9	—	—
45	—	—	PTH2	KBI6	ADC8	—	—
46	—	—	PTH1	KBI5	ADC7	—	—
47	—	—	PTH0	KBI4	ADC6	—	—
48	36	26	PTC6	$\overline{RESET}$	—	—	—
49	37	27	PTC5	BKGD/MS	—	—	—
50	38	28	PTA7	TPMCLK	ADC5	LCD28	—
51	39	29	PTA6	KBI7	TPM2CH1	ADC4	LCD27
52	40	30	PTA5	KBI6	TPM2CH0	ADC3	LCD26
53	41	31	PTA4	KBI5	RX2	ADC2	LCD25
54	42	32	PTA3	KBI4	TX2	ADC1	LCD24
55	43	33	PTA2	SDA	ADC0	LCD23	—
56	44	34	PTA1	SCL	LCD22	—	—
57	45	—	PTG3	LCD36	—	—	—
58	46	—	PTG2	LCD35	—	—	—
59	47	35	PTA0	LCD21	—	—	—
60	48	36	PTC4	LCD20	—	—	—
61	49	37	PTC3	LCD19	—	—	—
62	50	38	PTC2	LCD18	—	—	—
63	51	39	PTC1	LCD17	—	—	—
64	52	40	PTC0	LCD16	—	—	—
65	53	41	PTE7	LCD15	—	—	—
66	54	42	PTE6	LCD14	—	—	—
67	55	—	V_{SS2}	—	—	—	—
68	56	—	V_{LL3_2}	—	—	—	—
69	—	—	PTG7	LCD44	—	—	—
70	—	—	PTG6	LCD43	—	—	—
71	—	—	PTG5	LCD42	—	—	—
72	—	—	PTG4	LCD41	—	—	—
73	57	—	PTG1	LCD34	—	—	—
74	58	—	PTG0	LCD33	—	—	—
75	59	43	PTE5	LCD13	—	—	—
76	60	44	PTE4	LCD12	—	—	—

Table 4. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25 ±2	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages and use the largest of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in an external power supply going out of regulation. Ensure that the external V_{DD} load will shunt current greater than maximum injection current, this will be of greater risk when the MCU is not consuming power. For instance, if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

2.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in On-Chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to +105	°C
Maximum junction temperature	T_J	125	°C
Thermal resistance Single-layer board 80-pin LQFP 64-pin LQFP 48-pin LQFP	θ_{JA}	 61 71 80	°C/W
Thermal resistance Four-layer board 80-pin LQFP 64-pin LQFP 48-pin LQFP	θ_{JA}	 48 52 56	°C/W

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

Table 7. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	2500	—	V
2	Charge device model (CDM)	V_{CDM}	750	—	V
3	Latch-up current at T_A = 85 °C	I_{LAT}	±100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

2.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 8. DC Characteristics

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	—	Operating Voltage	—	2.7	—	5.5	V
2	P	Output high voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –0.6 mA	V_{OH}	 V_{DD} – 0.8 V_{DD} – 0.8	 — —	 — —	V
		Output high voltage — High Drive (PTxDSn = 1) V 5 V, I_{Load} = –10 mA 3 V, I_{Load} = –3 mA		 V_{DD} – 0.8 V_{DD} – 0.8	 — —	 — —	
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 0.6 mA	V_{OL}	—	 — —	 0.8 0.8	V
		Output low voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 10 mA 3 V, I_{Load} = 3 mA			 — —	 0.8 0.8	
4	P	Output high current — Max total I_{OH} for all ports 5 V 3 V	I_{OHT}	—	—	 100 60	mA
5	C	Output high current — Max total I_{OL} for all ports 5 V 3 V	I_{OLT}	—	—	 100 60	mA
6	P	Bandgap voltage reference	V_{BG}	—	1.225	—	V
7	P	Input high voltage; all digital inputs	V_{IH}	0.65 x V_{DD}	—	—	V
8	P	Input low voltage; all digital inputs	V_{IL}	—	—	0.35 x V_{DD}	V
9	P	Input hysteresis; all digital inputs	V_{hys}	0.06 x V_{DD}	—	—	mV
10	P	Input leakage current; input only pins[2] V_{In} = V_{DD} or V_{SS}	$\lvert I_{In} \rvert$	—	0.1	1	μA
11	P	High impedence (off-state) leakage current V_{In} = V_{DD} or V_{SS}	$\lvert I_{OZ} \rvert$	—	0.1	1	μA
12	P	Internal pullup resistors[3]	R_{PU}	20	45	65	kΩ
13	P	Internal pulldown resistors[4]	R_{PD}	20	45	65	kΩ

2.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	C	Run supply current FEI mode, all modules on	RI_{DD}	20 MHz	3	16.38	27.85	mA	–40 °C to 85 °C
	C						28.05		–40 °C to105 °C
	C			1 MHz		1.67	2.84		–40 °C to 85 °C
	C						2.87		–40 °C to105 °C
	P			20 MHz	5	16.55	28.14	mA	–40 °C to 85 °C
	P						28.35		–40 °C to105 °C
	C			1 MHz		1.77	3.01		–40 °C to 85 °C
	C						3.05		–40 °C to105 °C
2	T	Run supply current FEI mode, all modules off	RI_{DD}	20 MHz	3	11.9	20.25	mA	–40 °C to 85 °C
	T						21.72		–40 °C to105 °C
	T			1 MHz		1.16	1.95		–40 °C to 85 °C
	T						1.98		–40 °C to105 °C
	T			20 MHz	5	12.68	21.56	mA	–40 °C to 85 °C
	T						23.12		–40 °C to105 °C
	T			1 MHz		1.4	2.39		–40 °C to 85 °C
	T						2.41		–40 °C to105 °C
3	T	Wait mode supply current FEI mode, all modules off	WI_{DD}	20 MHz	3	7.9	13.42	mA	–40 °C to 85 °C
	T						13.59		–40 °C to105 °C
	T			1 MHz		0.88	1.49		–40 °C to 85 °C
	T						1.51		–40 °C to105 °C
	P			20 MHz	5	8.13	13.81	mA	–40 °C to 85 °C
	P						13.98		–40 °C to105 °C
	T			1 MHz		1.12	1.91		–40 °C to 85 °C
	T						1.94		–40 °C to105 °C
4	C	Stop2 mode supply current	$S2I_{DD}$	n/a	3	1.1	16.0	µA	–40 °C to 85 °C
	C						39.0		–40 °C to105 °C
	P				5	1.2	18.7	µA	–40 °C to 85 °C
	P						46.1		–40 °C to105 °C
5	C	Stop3 mode supply current No clocks active	$S3I_{DD}$	n/a	3	1.2	22.4	µA	–40 °C to 85 °C
	C						56.2		–40 °C to105 °C
	P				5	1.32	25.5	µA	–40 °C to 85 °C
	P						63.9		–40 °C to105 °C

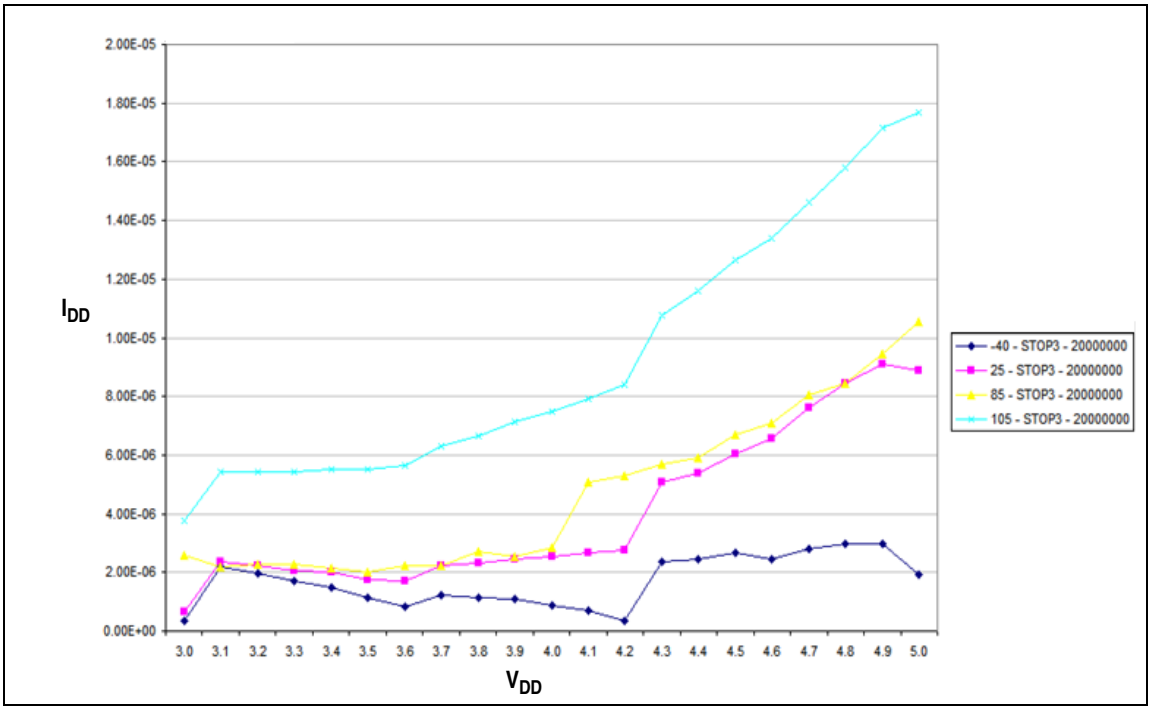


Figure 14. Typical Stop3 I_{DD}

2.8 External Oscillator (XOSC) Characteristics

Table 10. Oscillator Electrical Specifications (Temperature Range = –40 °C to 105 °C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	D	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) • Low range (RANGE = 0) • High range (RANGE = 1) FEE or FBE mode[2] • High range (RANGE = 1, HGO = 1) BLPE mode • High range (RANGE = 1, HGO = 0) BLPE mode	 f_{lo} f_{hi} f_{hi-hgo} f_{hi-lp}	 32 1 1 1	 — — — —	 38.4 5 16 8	 kHz MHz MHz MHz
2	D	Load capacitors	C_1 C_2	See crystal or resonator manufacturer's recommendation.			

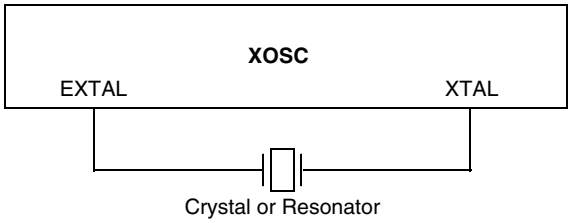


Figure 16. Typical Crystal or Resonator Circuit: Low Range/Low Power

2.9 Internal Clock Source (ICS) Characteristics

Table 11. ICS Frequency Specifications (Temperature Range = –40 °C to 105 °C Ambient)

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
1	P	Average internal reference frequency — factory trimmed at VDD = 5.0 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	C	Average internal reference frequency — user trimmed		f_{int_t}	31.25	—	39.0625	kHz
3	C	Internal reference start-up time		t_{IRST}	—	60	100	µs
4	P	DCO output frequency range — trimmed[2]	Low range (DRS = 00)	f_{dco_t}	16	—	20	MHz
	P		Mid range (DRS = 01)		32	—	40	
5	P	DCO output frequency[2] Reference = 32768 Hz and DMX32 = 1	Low range (DRS = 00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DRS = 01)		—	39.85	—	
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)[3]		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)[3]		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	P	Total deviation of trimmed DCO output frequency over voltage and temperature		Δf_{dco_t}	—	–1.0 to +0.5	±2	$\%f_{dco}$
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 °C to 70 °C[3]		Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	C	FLL acquisition time[3, 4]		$t_{Acquire}$	—	—	1	mS
11	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[5]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This parameter is characterized and not tested on each device.

4 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

5 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in the crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

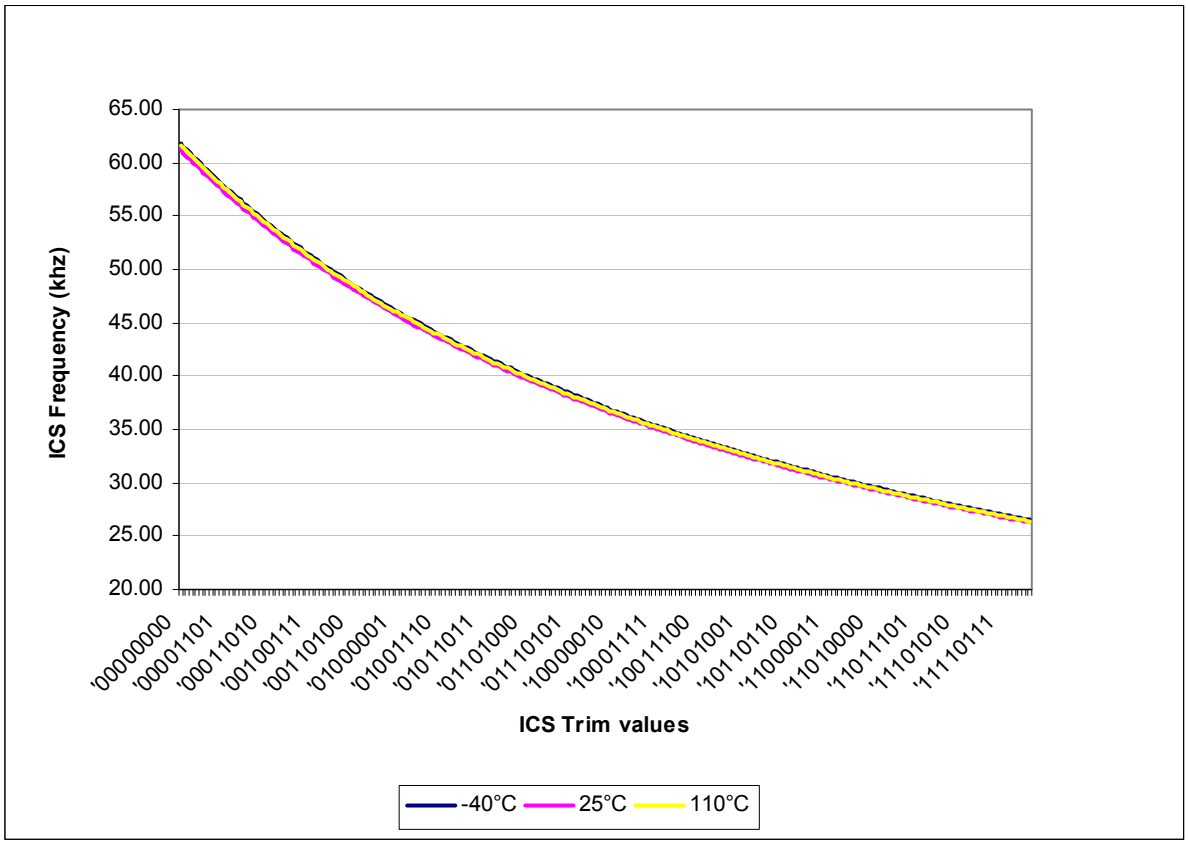


Figure 17. Internal Oscillator Deviation from Trimmed Frequency

2.10 ADC Characteristics

Table 12. 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDAD}	2.7	—	5.5	V	—
	Delta to V_{DD} ($V_{DD} - V_{DDAD}$)[2]	ΔV_{DDAD}	–100	0	+100	mV	—
Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSAD}$)[2]	ΔV_{SSAD}	–100	0	+100	mV	—
Ref Voltage High	—	V_{REFH}	—	—	—	V	V_{REFH} shorted to V_{DDAD}
Ref Voltage Low	—	V_{REFL}	—	—	—	V	V_{REFL} shorted to V_{SSAD}
Input Voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
Input Capacitance	—	C_{ADIN}	—	4.5	5.5	pF	—

Table 12. 12-bit ADC Operating Conditions (continued)

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Input Resistance	—	R_{ADIN}	—	5	7	kΩ	—
Analog Source Resistance	12-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
	10-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz		 — —	 — —	 5 10		
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC Conversion Clock Freq.	High Speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low Power (ADLPC = 1)		0.4	—	4.0		

1 Typical values assume V_{DDAD} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

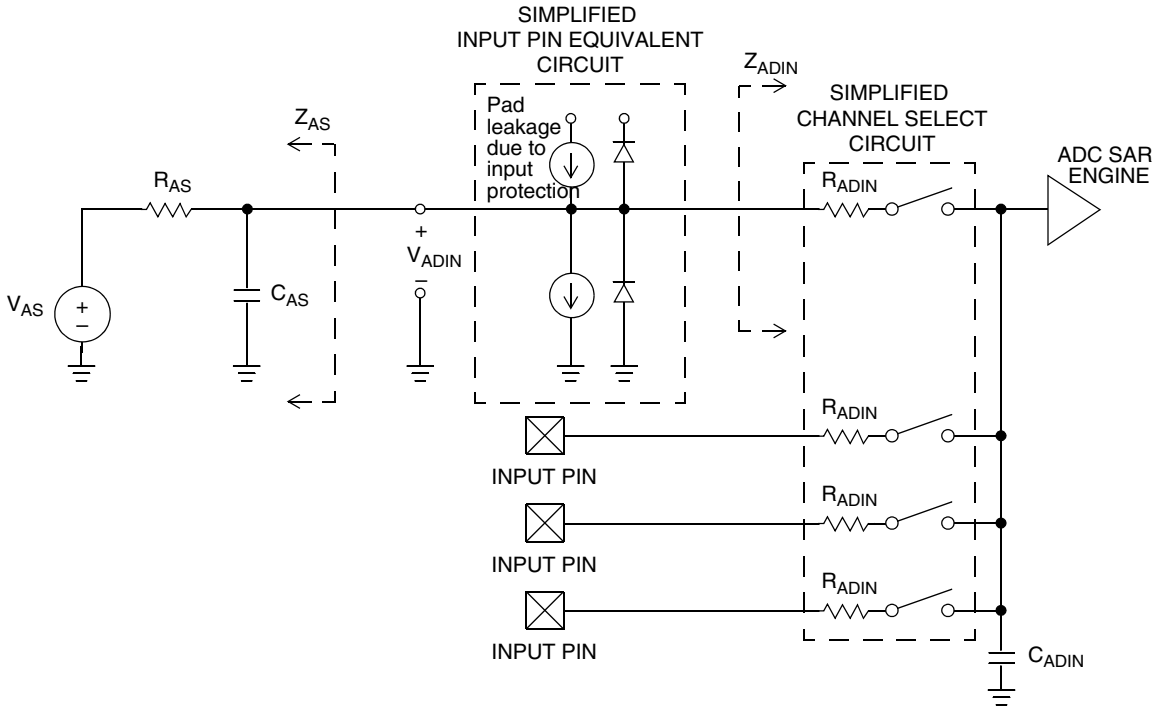


Figure 18. ADC Input Impedance Equivalency Diagram

Table 13. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD})

Num	C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
1	T	Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1	—	I_{DDAD}	—	195	—	µA	—
2	T	Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1	—	I_{DDAD}	—	347	—	µA	—
3	T	Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1	—	I_{DDAD}	—	407	—	µA	—
4	P	Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1	—	I_{DDAD}	—	0.755	1	mA	—
5	—	Supply Current	Stop, Reset, Module Off	IDDAD		0.011	1	µA	—
6	P	ADC Asynchronous Clock Source	High Speed (ADLPC=0)	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
			Low Power (ADLPC=1)		1.25	2	3.3		
7	C	Conversion Time (Including sample time)	Short sample (ADLSMP=0)	t_{ADC}	—	20	—	ADCK cycles	See *ADC chapter in the LG32 Reference Manual* for conversion time variances
			Long sample (ADLSMP=1)		—	40	—		
8	C	Sample Time	Short sample (ADLSMP=0)	t_{ADS}	—	3.5	—	ADCK cycles	
			Long sample (ADLSMP=1)		—	23.5	—		
9	T	Total Unadjusted Error	12-bit mode	E_{TUE}	—	±3.0	—	LSB^2	Includes quantization
	P		10-bit mode		—	±1	±2.5		
	T		8-bit mode		—	±0.5	±1		
10	T	Differential Non-Linearity	12-bit mode	DNL	—	±1.75	—	LSB^2	
	P		10-bit mode[3]		—	±0.5	±1.0		
	T		8-bit mode[3]		—	±0.3	±0.5		
11	T	Integral Non-Linearity	12-bit mode	INL	—	±1.5	—	LSB^2	
	P		10-bit mode		—	±0.5	±1		
	T		8-bit mode		—	±0.3	±0.5		
12	T	Zero-Scale Error	12-bit mode	E_{ZS}	—	±1.5	—	LSB^2	V_{ADIN} = V_{SSAD}
	P		10-bit mode		—	±0.5	±1.5		
	T		8-bit mode		—	±0.5	±0.5		

2.11 AC Characteristics

This section describes timing characteristics for each peripheral system.

2.11.1 Control Timing

Table 14. Control Timing

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1	D	Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	dc	—	20	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	µs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	66 x t_{cyc}	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	µs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	 t_{ILIH} t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	 t_{ILIH} t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
9	C	Port rise and fall time — (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	 t_{Rise} t_{Fall}	 — —	 3 30	 — —	ns

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 105 °C.

6 Except for LCD pins in Open Drain mode.

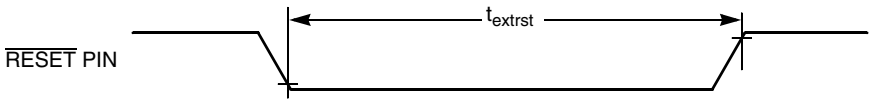
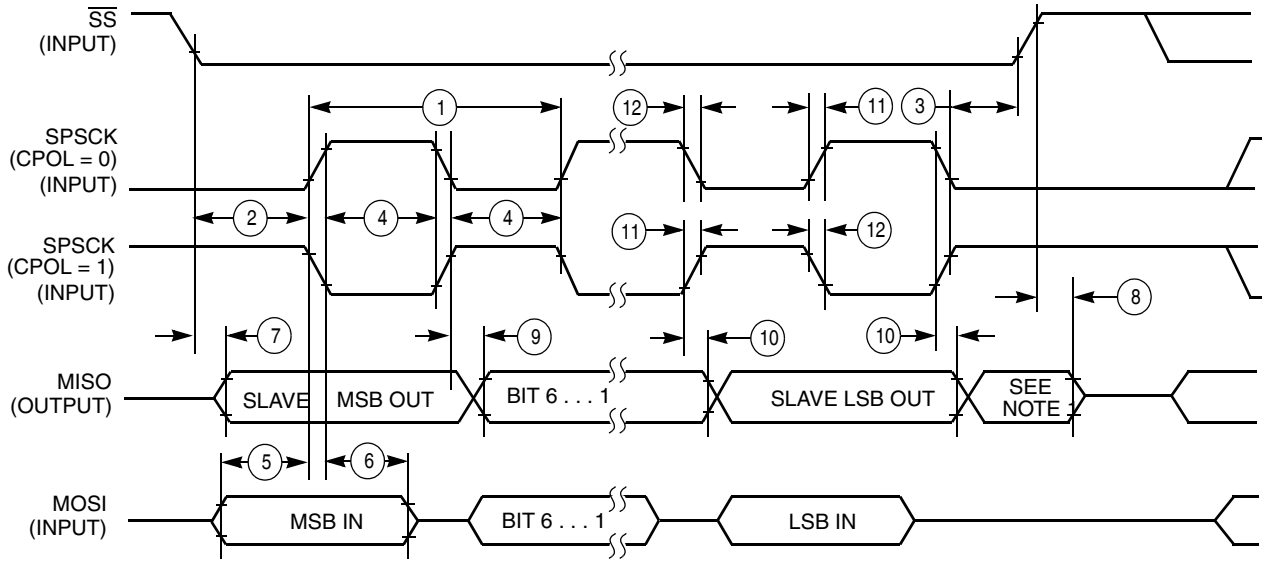
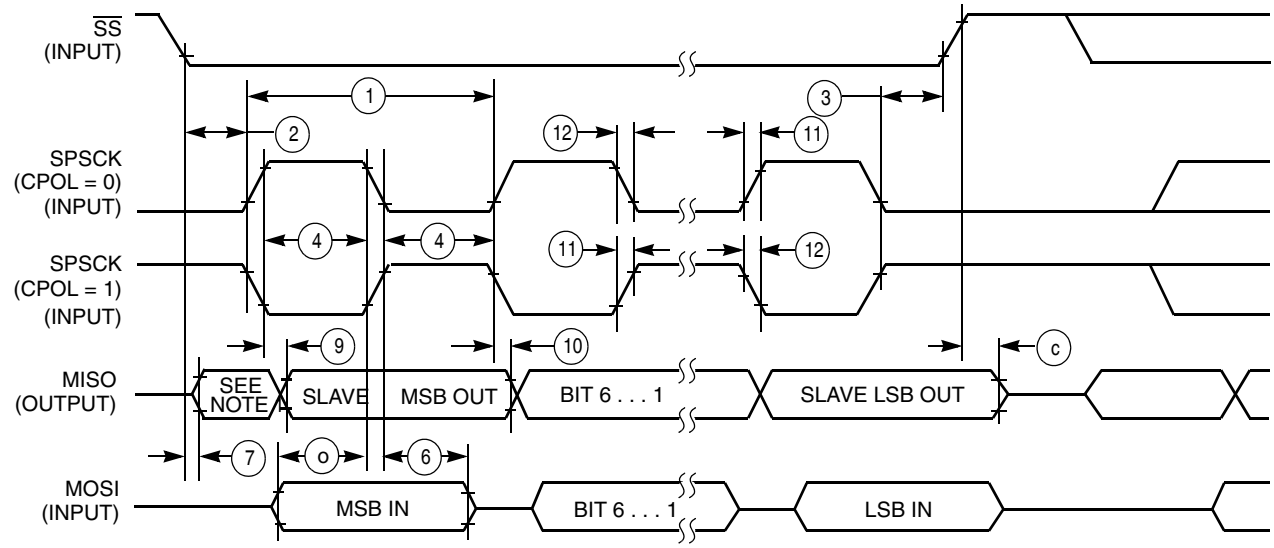


Figure 19. Reset Timing



NOTE:
1. Not defined but normally MSB of character just received.

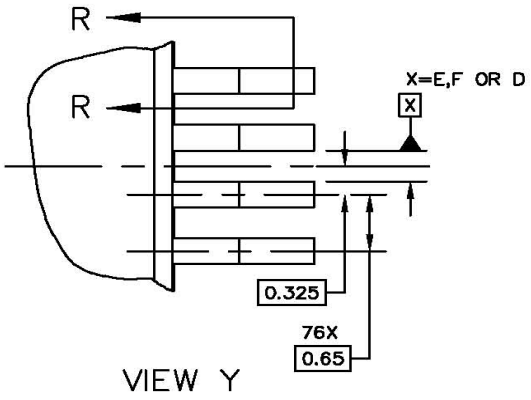
Figure 25. SPI Slave Timing (CPHA = 0)



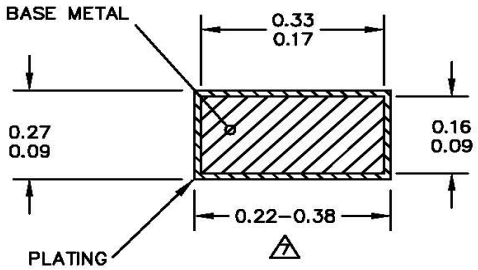
NOTE:
1. Not defined but normally LSB of character just received

Figure 26. SPI Slave Timing (CPHA = 1)

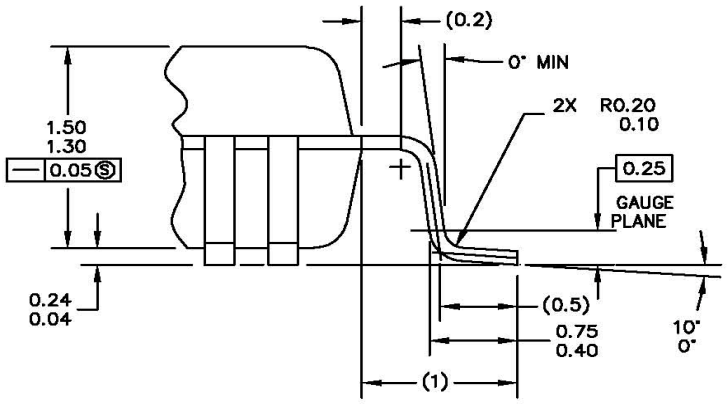
freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23237W
		PAGE: 917A
	DO NOT SCALE THIS DRAWING	REV: E



VIEW Y



SECTION R–R
ROTATED 90° CW



VIEW K

TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	CASE NUMBER: 917A–03	
	STANDARD: FREESCALE	
	PACKAGE CODE: 8258	SHEET: 2 OF 3

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23237W
		PAGE: 917A
	DO NOT SCALE THIS DRAWING	REV: E

NOTES:

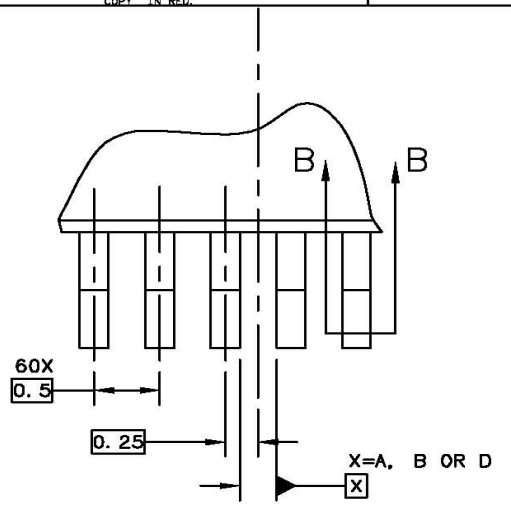
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION : MILIMETER.
3. DATUM PLANE H IS LOCATED AT THE BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUM E, F AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	CASE NUMBER: 917A–03	
	STANDARD: FREESCALE	
	PACKAGE CODE: 8258	SHEET: 3 OF 3

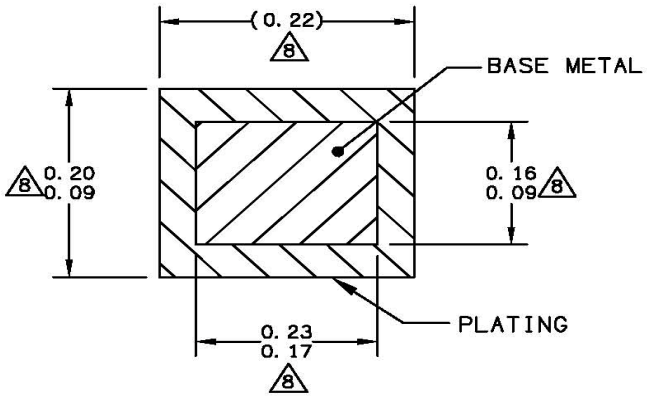
Figure 33. 80-pin LQFP Package Drawing (Case 917A, Doc #98ASS23237W)

freescale semiconductor

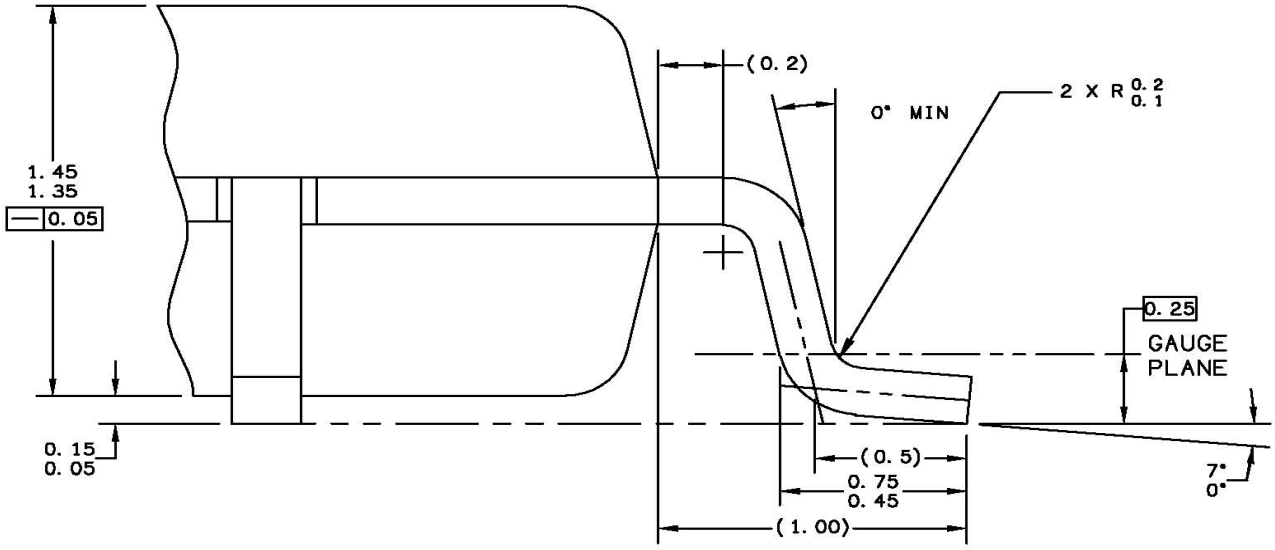
MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23234W
	PAGE: 840F
DO NOT SCALE THIS DRAWING	REV: E



VIEW Y



SECTION B–B



VIEW AA

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F–02	
	STANDARD: JEDEC MS–026 BCD	
	PACKAGE CODE: 8426	SHEET: 2 OF 3

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASH00962A
		PAGE: 932
	DO NOT SCALE THIS DRAWING	REV: G

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

TITLE: LQFP, 48 LEAD, 0.50 PITCH (7.0 X 7.0 X 1.4)	CASE NUMBER: 932–03	
	STANDARD: JEDEC MS–026–BBC	
	PACKAGE CODE: 6089	SHEET: 2 OF 2

Figure 35. 48-pin LQFP Package Drawing (Case 932, Doc #98ASH00962A)

5 Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web are the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://www.freescale.com

The following revision history table summarizes changes contained in this document.

Table 24. Revision History

Revision	Date	Description of Changes
1	8/2008	First Initial release.
2	9/2008	Second Initial Release.
3	11/2008	Alpha Customer Release.
4	2/2009	Launch Release.
5	4/2009	Added EMC Radiated Emission and Transient Susceptibility data in Table 19 and Table 20.
6	4/2009	Updated EMC performance data.
7	8/2009	Updated auto part numbers, changed TCLK, T0CH0, T0CH1, T1CH0, T1CH1, T1CH2, T1CH3, T1CH3, T1CH4, and T1CH5 to TPMCLK, TPM0CH0, TPM0CH1,TPM1CH0, TPM1CH1, TPM1CH2, TPM1CH3, TPM1CH4, and TPM1CH5, and changed the maximum LCD frame frequency to 64 Hz.
8	8/2011	Updated Table “ICS Frequency Specifications (Temperature Range = –40 ×C to 105 ×C Ambient)”. Changed the value of row 8 column C from C to P.
9	9/2011	Updated Table “ICS Frequency Specifications (Temperature Range = –40 ×C to 105 ×C Ambient)”. Removed Footnote from Row 8. Updated the Revision History

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Rev. 10
04/2015