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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.9K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08lg32j0clkr

Freescale Semiconductor, Inc.
Data Sheet Addendum

Document Number: MC9S08LG32AD
Rev. 0, 04/2015

Addendum to Rev. 9 of the MC9S08LG32 Series Covers: MC9S08LG32 and MC9S08LG16

This addendum identifies changes to Rev. 9 of the MC9S08LG32 Series data sheet (covering MC9S08LG32 and MC9S08LG16). The changes described in this addendum have not been implemented in the specified pages.

1 Add min values for I_{IC} (DC injection current)

Location:	Table 8. DC Characteristics, Page 14

In Table 8, “DC Characteristics,” add min values for I_{IC} (row number 14) as follows:

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
14	D	DC injection current [5, 6, 7] $V_{IN} < V_{SS}$ (min) $V_{IN} > V_{DD}$ (max)	Single pin limit	I_{IC}	**-0.2**	—	2	mA
			Total MCU limit, includes sum of all stressed pins		**-5**	—	25	mA

2 Change the max value of t_{LPO} (low power oscillator period)

Location:	Table 14. Control Timing, Page 29

In Table 14, “Control Timing,” change the max value of t_{LPO} (row number 2) from 1300 to 1500 µs.

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Freescale Semiconductor
Data Sheet: Technical Data

Document Number: MC9S08LG32
Rev. 9 , 09/2011

MC9S08LG32 Series
Covers: MC9S08LG32 and MC9S08LG16

MC9S08LG32


80-LQFP
Case 917A
14 mm × 14 mm


64-LQFP
Case 840F
10 mm × 10 mm


48-LQFP
Case 932
7 mm × 7mm

Features

- 8-bit HCS08 Central Processor Unit (CPU)
  - Up to 40 MHz CPU at 5.5 V to 2.7 V across temperature range of –40 °C to 85 °C and –40 °C to 105 °C
  - HCS08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - 32 KB or 18 KB dual array flash; read/program/erase over full operating voltage and temperature
  - 1984 byte random access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
  - Two low-power stop modes (stop2 and stop3)
  - Reduced-power wait mode
  - Peripheral clock gating register can disable clocks to unused modules, thereby reducing currents
  - Low power On-Chip crystal oscillator (XOSC) that can be used in low-power modes to provide accurate clock source to real time counter and LCD controller
  - 100 µs typical wakeup time from stop3 mode
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports bus frequencies from 1 MHz to 20 MHz.
- System Protection
  - COP reset with option to run from dedicated 1 kHz internal clock or bus clock
  - Low-voltage warning with interrupt
  - Low-voltage detection with reset
  - Illegal opcode detection with reset
  - Illegal address detection with reset
  - Flash and RAM protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging and plus two more breakpoints in On-Chip debug module
  - On-Chip in-circuit emulator (ICE) debug module containing three comparators and nine trigger modes; eight deep FIFO for storing change-of-flow addresses and event-only data; debug module supports both tag and force breakpoints
- Peripherals
  - **LCD** — Up to 4 × 41 or 8 × 37 LCD driver with internal charge pump.
  - **ADC** — Up to 16-channel, 12-bit resolution, 2.5 µs conversion time, automatic compare function, temperature sensor, internal bandgap reference channel, runs in stop3 and can wake up the system, fully functional from 5.5 V to 2.7 V
  - **SCI** — Full duplex non-return to zero (NRZ), LIN master extended break generation, LIN slave extended break detection, wakeup on active edge
  - **SPI** — Full-duplex or single-wire bidirectional, double-buffered transmit and receive, master or slave mode, MSB-first or LSB-first shifting
  - **IIC** — With up to 100 kbps with maximum bus loading, multi-master operation, programmable slave address, interrupt driven byte-by-byte data transfer, supports broadcast mode and 10-bit addressing
  - **TPMx** — One 6 channel and one 2 channel, selectable input capture, output compare, or buffered edge or center-aligned PWM on each channel
  - **MTIM** — 8-bit counter with match register,, four clock sources with prescaler dividers, can be used for periodic wakeup
  - **RTC** — 8-bit modulus counter with binary or decimal based prescaler, three clock sources including one external source, can be used for time base, calendar, or task scheduling functions
  - **KBI** — One keyboard control module capable of supporting 8 × 8 keyboard matrix
  - **IRQ** — External pin for wakeup from low-power modes
- Input/Output
  - 39, 53, or 69 GPIOs
  - 8 KBI and 1 IRQ interrupt with selectable polarity
  - Hysteresis and configurable pullup device on all input pins, configurable slew rate and drive strength on all output pins.
- Package Options
  - 48-pin LQFP, 64-pin LQFP, and 80-pin LQFP

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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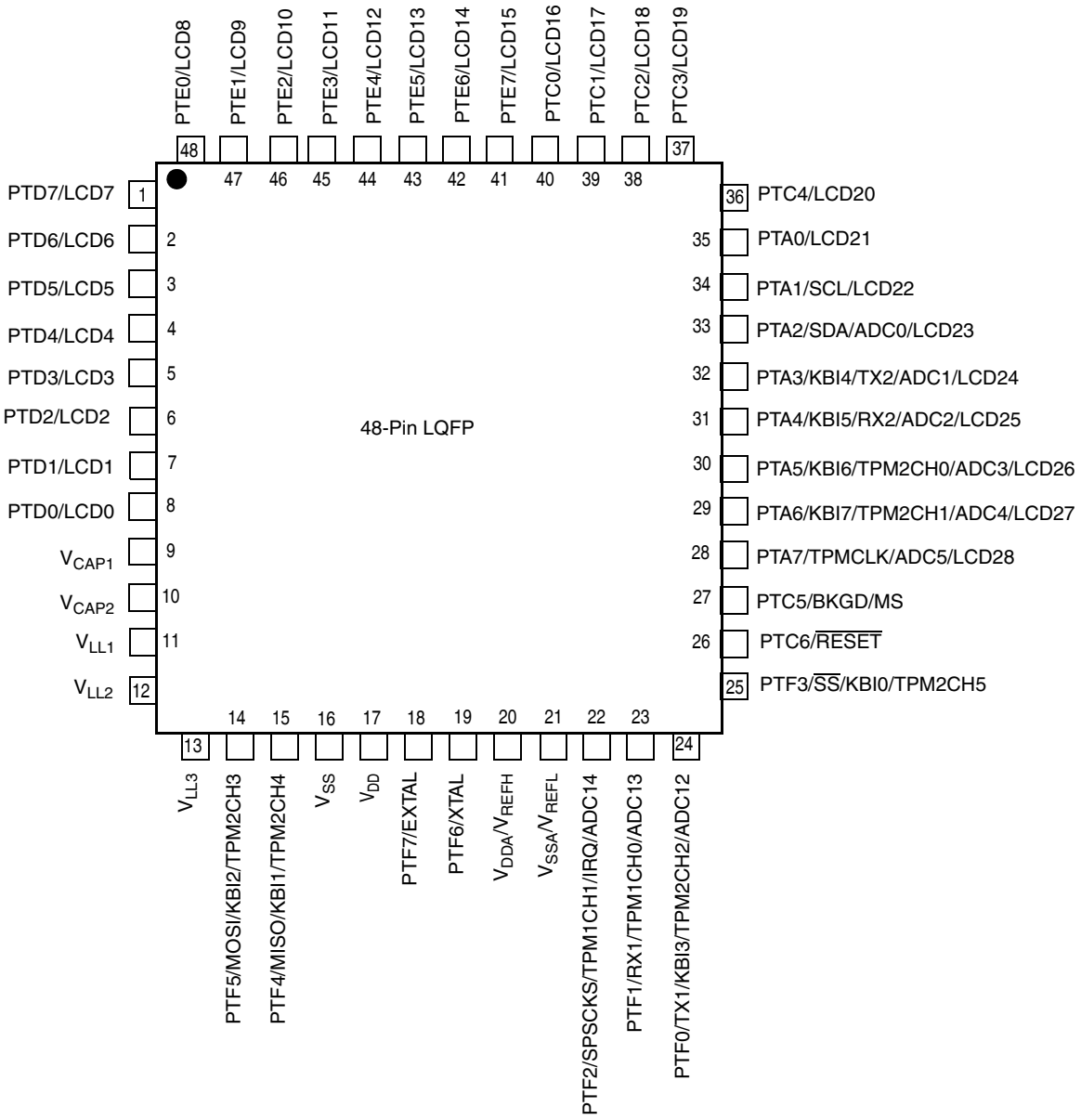


Figure 4. 48-Pin LQFP

NOTE

V_{REFH}/V_{REFL} are internally connected to V_{DDA}/V_{SSA}.

Table 2. Pin Availability by Package Pin-Count

Packages			<-- Lowest **Priority** --> Highest				
80	**64**	**48**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	1	1	PTD7	LCD7	—	—	—
2	2	2	PTD6	LCD6	—	—	—
3	3	3	PTD5	LCD5	—	—	—
4	4	4	PTD4	LCD4	—	—	—
5	5	5	PTD3	LCD3	—	—	—
6	6	6	PTD2	LCD2	—	—	—
7	7	—	PTB3	LCD32	—	—	—
8	8	—	PTB2	LCD31	—	—	—
9	—	—	PTB7	LCD40	—	—	—
10	—	—	PTB6	LCD39	—	—	—
11	—	—	PTB5	LCD38	—	—	—
12	—	—	PTB4	LCD37	—	—	—
13	9	—	PTB1	LCD30	—	—	—
14	10	—	PTB0	LCD29	—	—	—
15	11	7	PTD1	LCD1	—	—	—
16	12	8	PTD0	LCD0	—	—	—
17	13	9	V_{CAP1}	—	—	—	—
18	14	10	V_{CAP2}	—	—	—	—
19	15	11	V_{LL1}	—	—	—	—
20	16	12	V_{LL2}	—	—	—	—
21	17	13	V_{LL3}	—	—	—	—
22	18	14	PTF5	MOSI	KBI2	TPM2CH3	—
23	19	15	PTF4	MISO	KBI1	TPM2CH4	—
24	20	—	PTI5	TPM2CH0	SCL	$\overline{SS}$	—
25	21	—	PTI4	TPM2CH1	SDA	SPSCK	—
26	—	—	PTI3	TPM2CH2	MOSI	—	—
27	—	—	PTI2	TPM2CH3	MISO	—	—
28	—	—	PTI1	TMRCLK	TX2	—	—
29	—	—	PTI0	RX2	—	—	—
30	22	—	PTH7	KBI1	TPM2CH4	—	—
31	23	16	V_{SS}	—	—	—	—
32	24	17	V_{DD}	—	—	—	—
33	25	18	PTF7	EXTAL	—	—	—
34	26	19	PTF6	XTAL	—	—	—
35	27	20	V_{DDA}	V_{REFH}	—	—	—
36	28	21	V_{SSA}	V_{REFL}	—	—	—
37	29	—	PTH6	TPM2CH5	KBI0	ADC15	—
38	30	22	PTF2	SPSCK	TPM1CH1	IRQ	ADC14

Table 2. Pin Availability by Package Pin-Count (continued)

Packages			<-- Lowest **Priority** --> Highest				
80	**64**	**48**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
77	61	45	PTE3	LCD11	—	—	—
78	62	46	PTE2	LCD10	—	—	—
79	63	47	PTE1	LCD9	—	—	—
80	64	48	PTE0	LCD8	—	—	—

2 Electrical Characteristics

2.1 Introduction

This section contains electrical and timing specifications for the MC9S08LG32 series of microcontrollers available at the time of publication.

2.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 3. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 4 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry that protects against damage due to high static voltage or electrical fields. However, it is advised that normal precautions should be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 4. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25 ±2	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages and use the largest of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in an external power supply going out of regulation. Ensure that the external V_{DD} load will shunt current greater than maximum injection current, this will be of greater risk when the MCU is not consuming power. For instance, if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

2.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in On-Chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H –40 to +105	°C
Maximum junction temperature	T_J	125	°C
Thermal resistance Single-layer board 80-pin LQFP 64-pin LQFP 48-pin LQFP	θ_{JA}	 61 71 80	°C/W
Thermal resistance Four-layer board 80-pin LQFP 64-pin LQFP 48-pin LQFP	θ_{JA}	 48 52 56	°C/W

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

Table 8. DC Characteristics (continued)

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
14	D	DC injection current [5, 6, 7] $V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	Single pin limit	I_{IC}	—	—	2	mA
			Total MCU limit, includes sum of all stressed pins		—	—	25	mA
15	C	Input Capacitance, all non-supply pins		C_{In}	—	—	8	pF
16	C	RAM retention voltage		V_{RAM}	2	—	—	V
17	P	POR rearm voltage		V_{POR}	0.9	1.4	2.0	V
18	D	POR rearm time		t_{POR}	10	—	—	µs
19	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising		V_{LVD1}	 3.9 4.0	 4.0 4.1	 4.1 4.2	V
20	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising		V_{LVD0}	 2.48 2.54	 2.56 2.62	 2.64 2.70	V
21	P	Low-voltage warning threshold — high range 1 V_{DD} falling V_{DD} rising		V_{LVW3}	 4.5 4.6	 4.6 4.7	 4.7 4.8	V
22	P	Low-voltage warning threshold — high range 0 V_{DD} falling V_{DD} rising		V_{LVW2}	 4.2 4.3	 4.3 4.4	 4.4 4.5	V
23	P	Low-voltage warning threshold — low range 1 V_{DD} falling V_{DD} rising		V_{LVW1}	 2.84 2.90	 2.92 2.98	 3.00 3.06	V
24	P	Low-voltage warning threshold — low range 0 V_{DD} falling V_{DD} rising		V_{LVW0}	 2.66 2.72	 2.74 2.80	 2.82 2.88	V
25	P	Low-voltage inhibit reset/recover hysteresis 5 V 3 V		V_{hys}	—	 100 60	—	mV

1 Typical values are measured at 25 °C. Characterized, not tested

2 Measured with $V_{In} = V_{DD}$ or V_{SS}.

3 Measured with $V_{In} = V_{SS}$.

4 Measured with $V_{In} = V_{DD}$.

5 All functional non-supply pins, except for PTC6 are internally clamped to V_{SS} and V_{DD}.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. For instance, if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

Table 9. Supply Current Characteristics (continued)

Num	C	Parameter		Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
8	T	Stop3 adders:	EREFSTEN = 1	—	n/a	3	4.58	—	µA	–40 °C to 105 °C
			IREFSTEN = 1				71.7	—		
			LVD				94.35	—		
			EREFSTEN = 1			5	4.61	—	µA	
			IREFSTEN = 1				71.69	—		
			LVD				107.34	—		

1 Typical values are measured at 25 °C. Characterized, not tested.

2 LCD configured for Charge Pump Enabled V_{LL3} connected to V_{DD}.

3 This does not include current required for 32 kHz oscillator.

4 This is the maximum current when all LCD inputs/outputs are used.

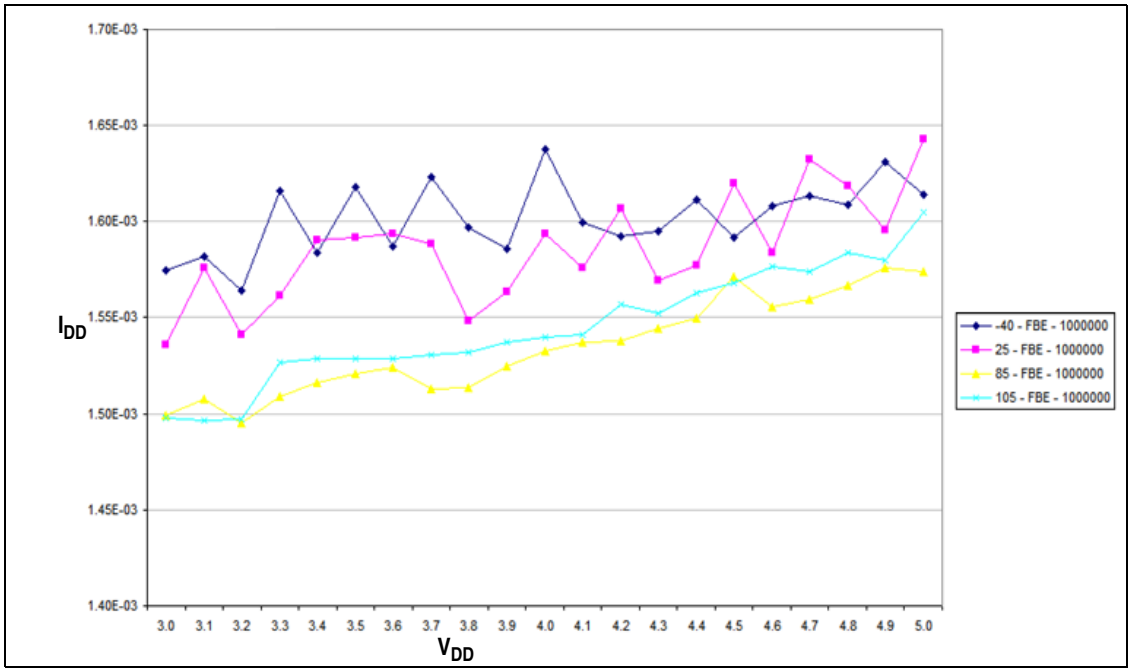


Figure 9. Typical Run I_{DD} for FBE Mode at 1 MHz

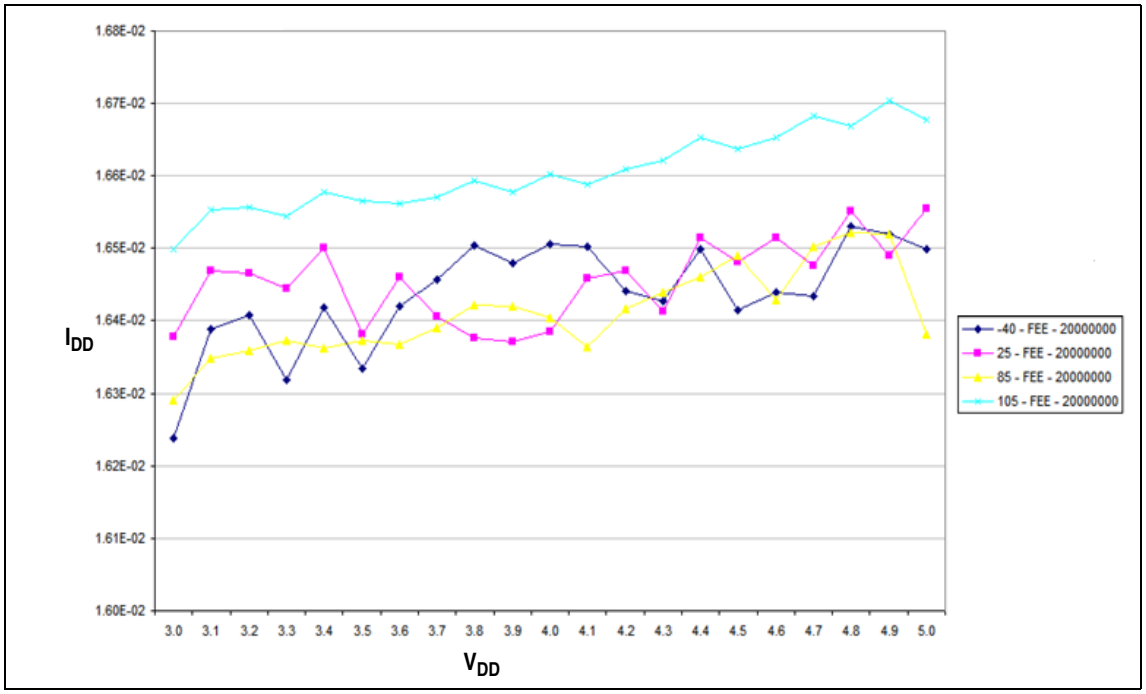


Figure 12. Typical Run I_{DD} for FEE Mode at 20 MHz

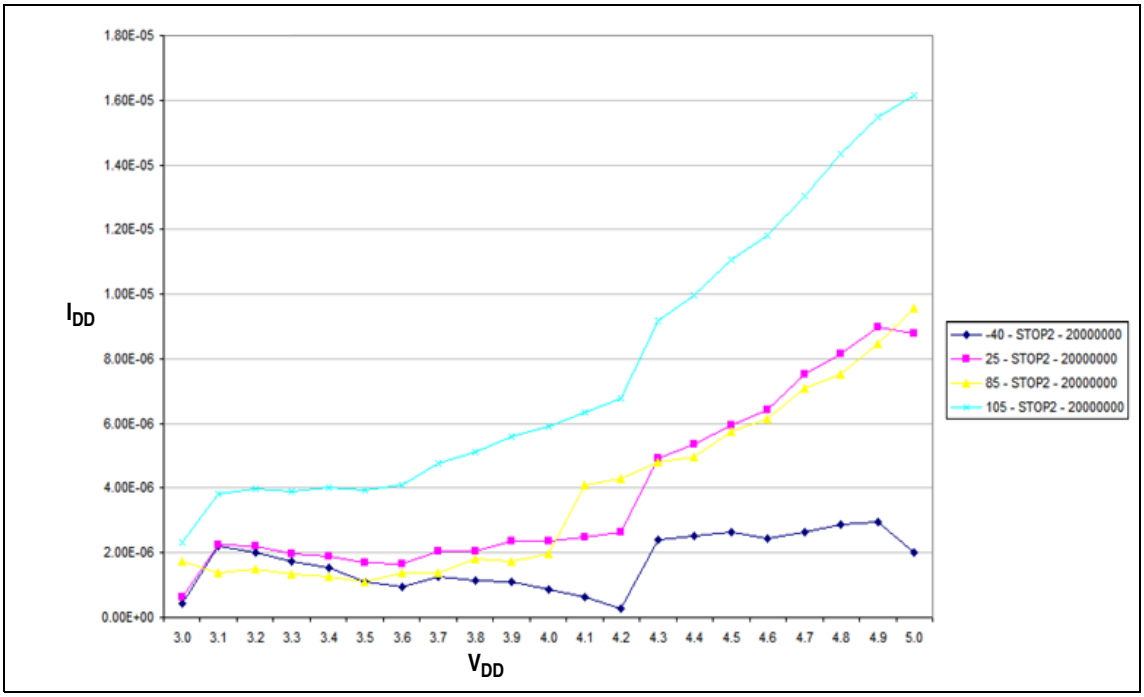


Figure 13. Typical Stop2 I_{DD}

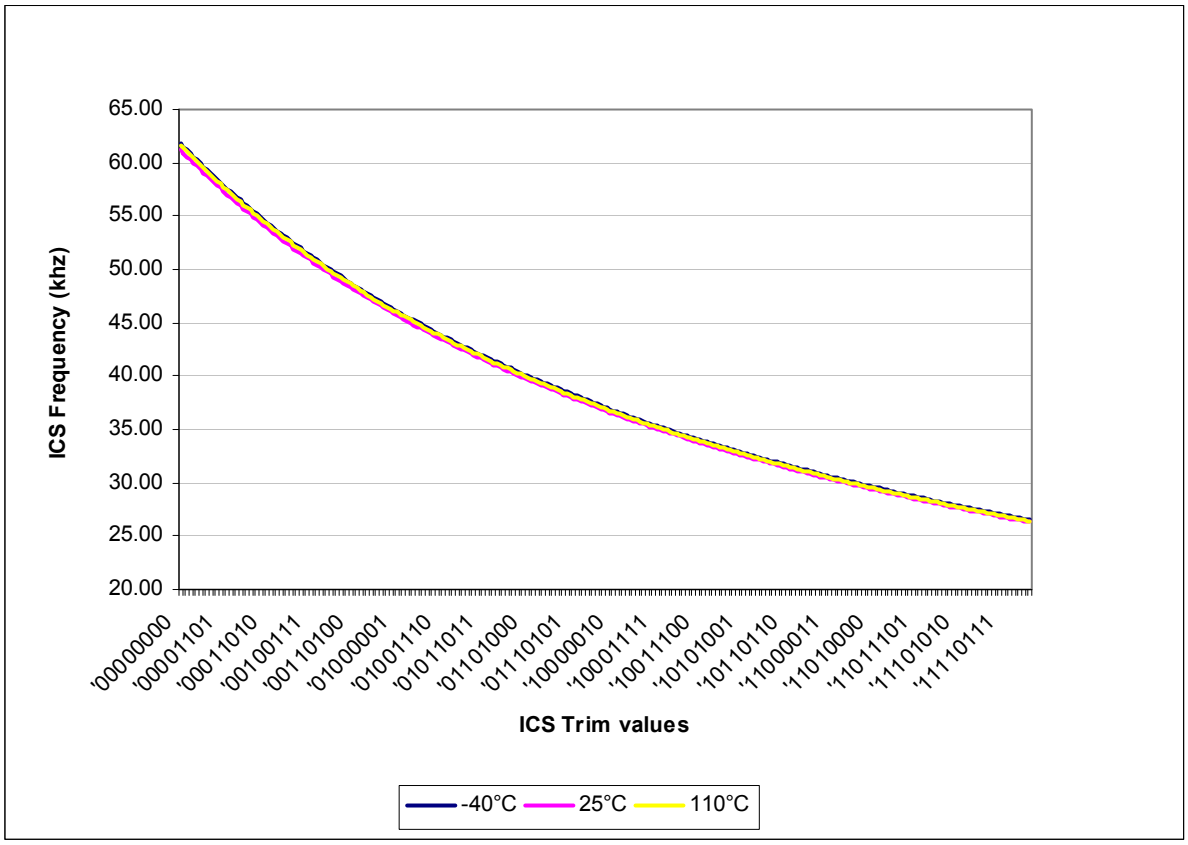


Figure 17. Internal Oscillator Deviation from Trimmed Frequency

2.10 ADC Characteristics

Table 12. 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDAD}	2.7	—	5.5	V	—
	Delta to V_{DD} ($V_{DD} - V_{DDAD}$)[2]	ΔV_{DDAD}	–100	0	+100	mV	—
Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSAD}$)[2]	ΔV_{SSAD}	–100	0	+100	mV	—
Ref Voltage High	—	V_{REFH}	—	—	—	V	V_{REFH} shorted to V_{DDAD}
Ref Voltage Low	—	V_{REFL}	—	—	—	V	V_{REFL} shorted to V_{SSAD}
Input Voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
Input Capacitance	—	C_{ADIN}	—	4.5	5.5	pF	—

Table 13. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
13	T	Full-Scale Error	12-bit mode	E_{FS}	—	±1	—	LSB[2]	V_{ADIN} = V_{DDAD}
	P		10-bit mode		—	±0.5	±1		
	T		8-bit mode		—	±0.5	±0.5		
14	D	Quantization Error	12-bit mode	E_Q	—	–1 to 0	—	LSB[2]	—
			10-bit mode		—	—	±0.5		
			8-bit mode		—	—	±0.5		
15	D	Input Leakage Error	12-bit mode	E_{IL}	—	±1	—	LSB[2]	Pad leakage[4] * R_{AS}
			10-bit mode		—	±0.2	±2.5		
			8-bit mode		—	±0.1	±1		
16	C	Temp Sensor Slope	–40 °C to 25 °C	m	—	1.646	—	mV/°C	—
			25 °C to 125°C		—	1.769	—		
17	C	Temp Sensor Voltage	25 °C	V_{TEMP25}	—	701.2	—	mV	—

1 Typical values assume V_{DDAD} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes

4 Based on input pad leakage current. Refer to pad electricals.

2.11 AC Characteristics

This section describes timing characteristics for each peripheral system.

2.11.1 Control Timing

Table 14. Control Timing

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1	D	Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	dc	—	20	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	µs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	66 x t_{cyc}	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	µs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	 t_{ILIH} t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	 t_{ILIH} t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
9	C	Port rise and fall time — (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	 t_{Rise} t_{Fall}	 — —	 3 30	 — —	ns

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 105 °C.

6 Except for LCD pins in Open Drain mode.

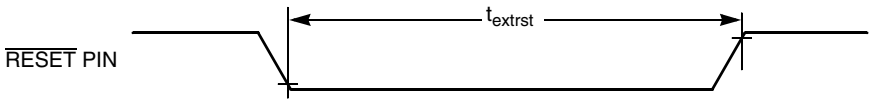


Figure 19. Reset Timing

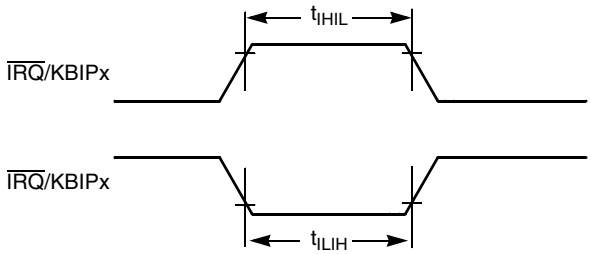


Figure 20. IRQ/KBIPx Timing

2.11.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 15. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

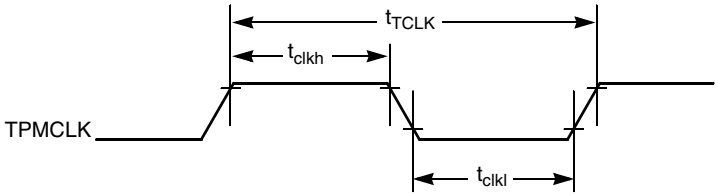


Figure 21. Timer External Clock

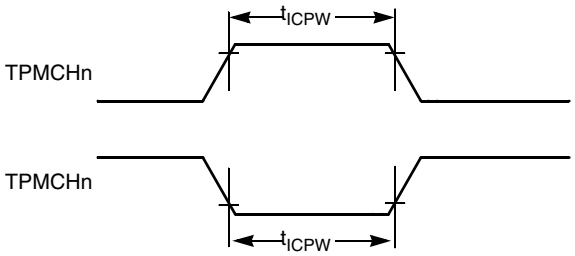
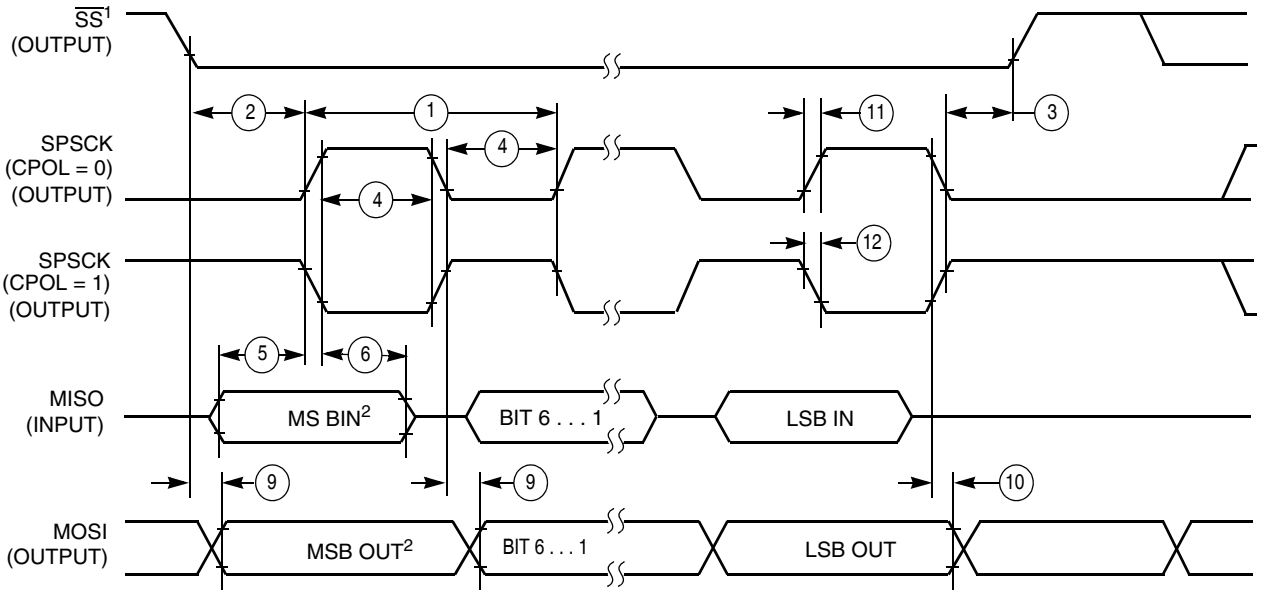
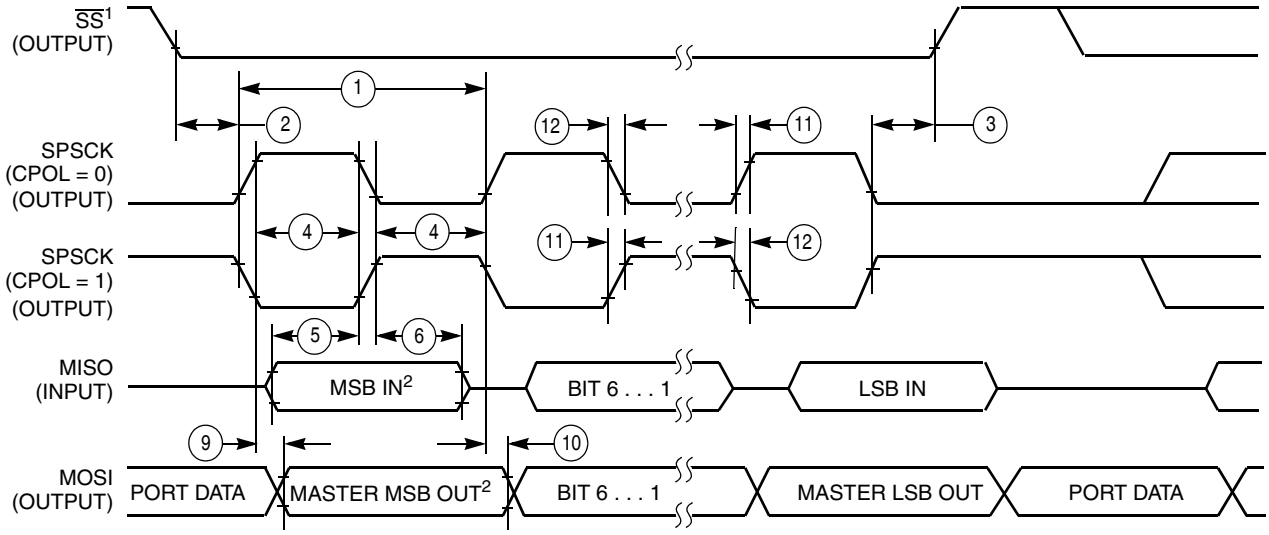


Figure 22. Timer Input Capture Pulse



NOTES:
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

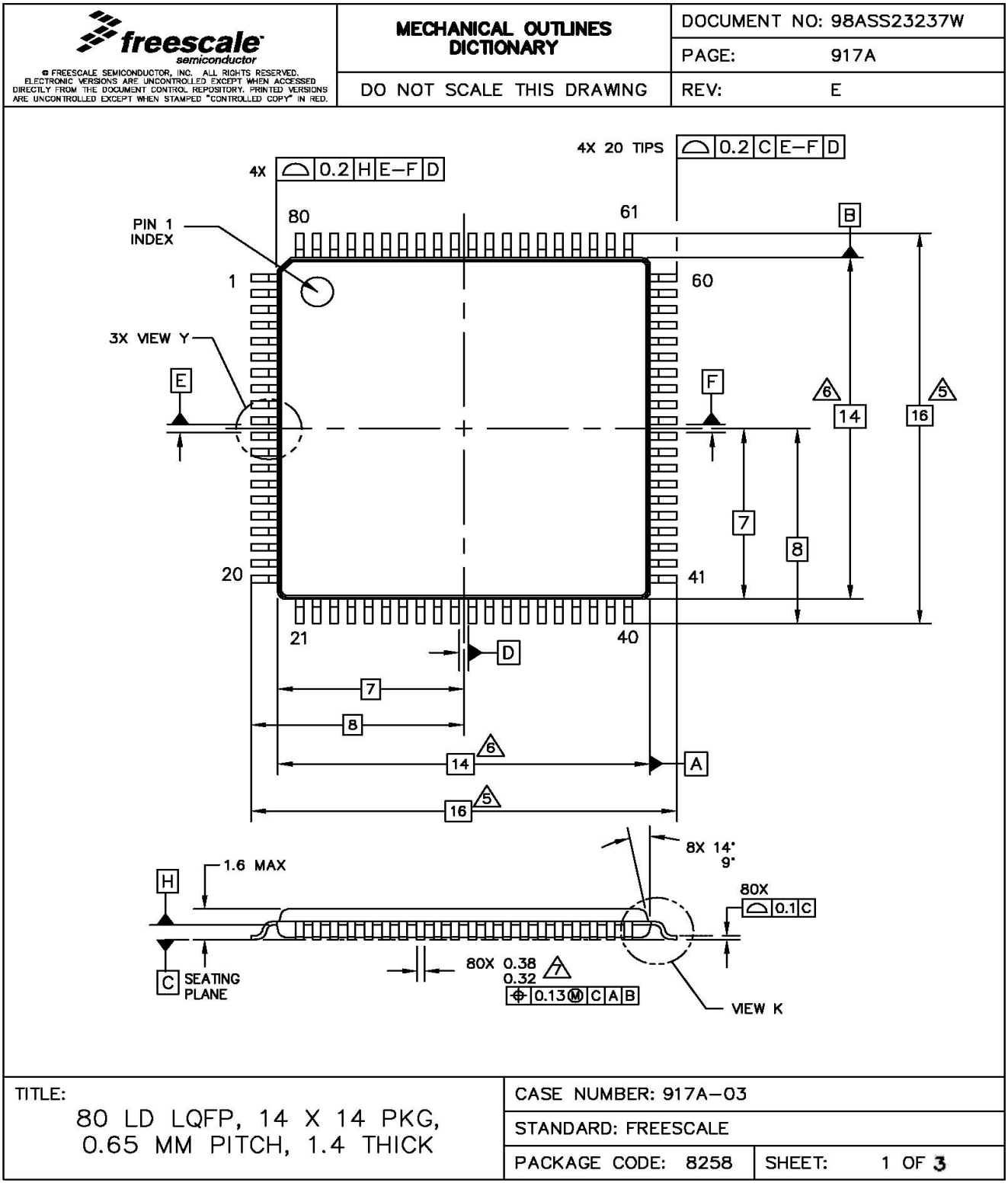
Figure 23. SPI Master Timing (CPHA = 0)



NOTES:
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 24. SPI Master Timing (CPHA =1)

4.1.1 80-pin LQFP



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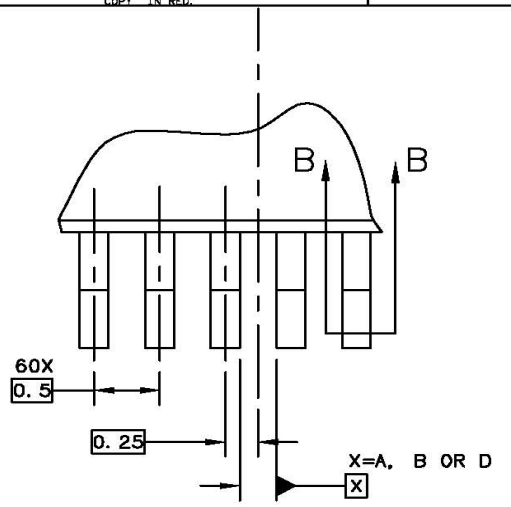
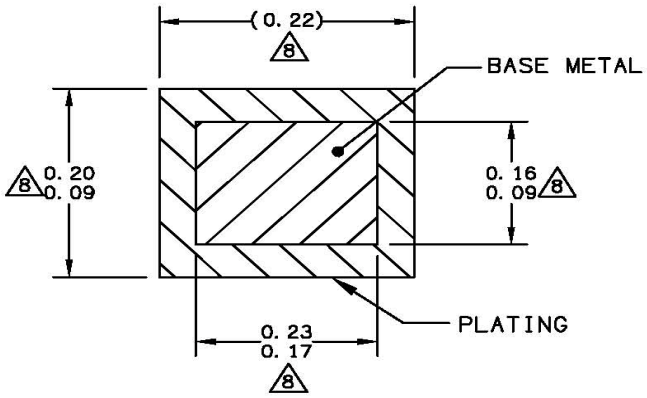
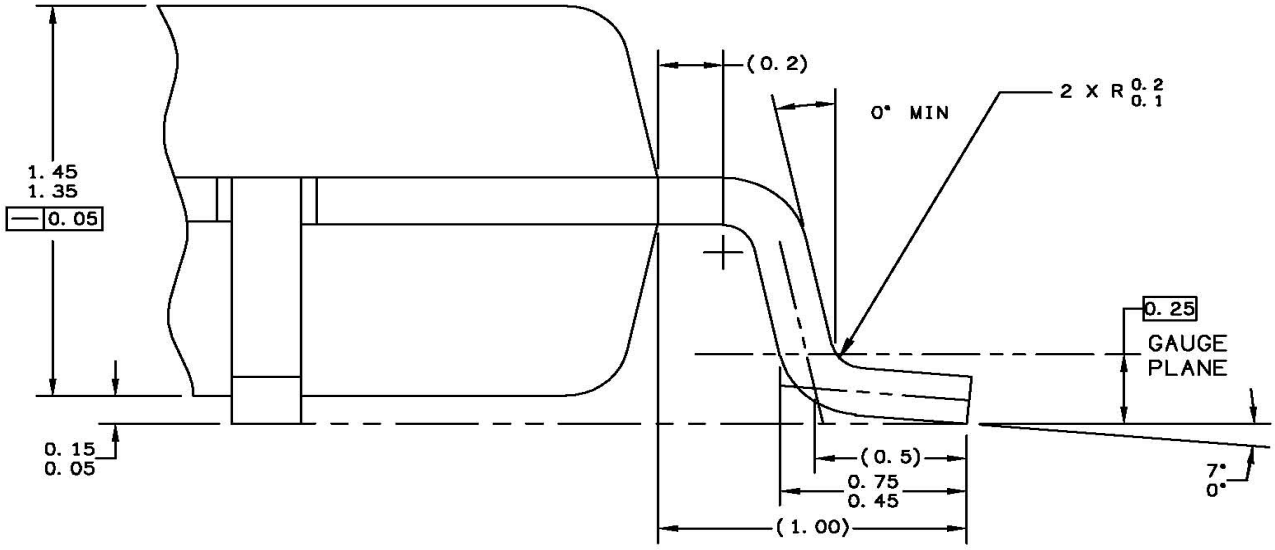


VIEW Y



SECTION B–B



VIEW AA

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F–02	
	STANDARD: JEDEC MS–026 BCD	
	PACKAGE CODE: 8426	SHEET: 2 OF 3

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		PAGE: 840F
	DO NOT SCALE THIS DRAWING	REV: E

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F–02	
	STANDARD: JEDEC MS–026 BCD	
	PACKAGE CODE: 8426	SHEET: 3 OF 3

Figure 34. 64-pin LQFP Package Drawing (Case 840F, Doc #98ASS23234W)

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		PAGE: 932
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NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

TITLE: LQFP, 48 LEAD, 0.50 PITCH (7.0 X 7.0 X 1.4)	CASE NUMBER: 932–03	
	STANDARD: JEDEC MS–026–BBC	
	PACKAGE CODE: 6089	SHEET: 2 OF 2

Figure 35. 48-pin LQFP Package Drawing (Case 932, Doc #98ASH00962A)

5 Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web are the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://www.freescale.com

The following revision history table summarizes changes contained in this document.

Table 24. Revision History

Revision	Date	Description of Changes
1	8/2008	First Initial release.
2	9/2008	Second Initial Release.
3	11/2008	Alpha Customer Release.
4	2/2009	Launch Release.
5	4/2009	Added EMC Radiated Emission and Transient Susceptibility data in Table 19 and Table 20.
6	4/2009	Updated EMC performance data.
7	8/2009	Updated auto part numbers, changed TCLK, T0CH0, T0CH1, T1CH0, T1CH1, T1CH2, T1CH3, T1CH3, T1CH4, and T1CH5 to TPMCLK, TPM0CH0, TPM0CH1,TPM1CH0, TPM1CH1, TPM1CH2, TPM1CH3, TPM1CH4, and TPM1CH5, and changed the maximum LCD frame frequency to 64 Hz.
8	8/2011	Updated Table “ICS Frequency Specifications (Temperature Range = –40 ×C to 105 ×C Ambient)”. Changed the value of row 8 column C from C to P.
9	9/2011	Updated Table “ICS Frequency Specifications (Temperature Range = –40 ×C to 105 ×C Ambient)”. Removed Footnote from Row 8. Updated the Revision History

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04/2015