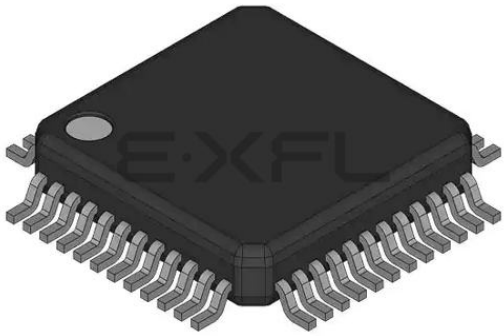

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.9K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 9x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s9s08lg32j0vlf

Freescale Semiconductor
Data Sheet: Technical Data

Document Number: MC9S08LG32
Rev. 9 , 09/2011

MC9S08LG32 Series
Covers: MC9S08LG32 and MC9S08LG16

MC9S08LG32


80-LQFP
Case 917A
14 mm × 14 mm


64-LQFP
Case 840F
10 mm × 10 mm


48-LQFP
Case 932
7 mm × 7mm

Features

- 8-bit HCS08 Central Processor Unit (CPU)
  - Up to 40 MHz CPU at 5.5 V to 2.7 V across temperature range of –40 °C to 85 °C and –40 °C to 105 °C
  - HCS08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - 32 KB or 18 KB dual array flash; read/program/erase over full operating voltage and temperature
  - 1984 byte random access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
  - Two low-power stop modes (stop2 and stop3)
  - Reduced-power wait mode
  - Peripheral clock gating register can disable clocks to unused modules, thereby reducing currents
  - Low power On-Chip crystal oscillator (XOSC) that can be used in low-power modes to provide accurate clock source to real time counter and LCD controller
  - 100 µs typical wakeup time from stop3 mode
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports bus frequencies from 1 MHz to 20 MHz.
- System Protection
  - COP reset with option to run from dedicated 1 kHz internal clock or bus clock
  - Low-voltage warning with interrupt
  - Low-voltage detection with reset
  - Illegal opcode detection with reset
  - Illegal address detection with reset
  - Flash and RAM protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging and plus two more breakpoints in On-Chip debug module
  - On-Chip in-circuit emulator (ICE) debug module containing three comparators and nine trigger modes; eight deep FIFO for storing change-of-flow addresses and event-only data; debug module supports both tag and force breakpoints
- Peripherals
  - **LCD** — Up to 4 × 41 or 8 × 37 LCD driver with internal charge pump.
  - **ADC** — Up to 16-channel, 12-bit resolution, 2.5 µs conversion time, automatic compare function, temperature sensor, internal bandgap reference channel, runs in stop3 and can wake up the system, fully functional from 5.5 V to 2.7 V
  - **SCI** — Full duplex non-return to zero (NRZ), LIN master extended break generation, LIN slave extended break detection, wakeup on active edge
  - **SPI** — Full-duplex or single-wire bidirectional, double-buffered transmit and receive, master or slave mode, MSB-first or LSB-first shifting
  - **IIC** — With up to 100 kbps with maximum bus loading, multi-master operation, programmable slave address, interrupt driven byte-by-byte data transfer, supports broadcast mode and 10-bit addressing
  - **TPMx** — One 6 channel and one 2 channel, selectable input capture, output compare, or buffered edge or center-aligned PWM on each channel
  - **MTIM** — 8-bit counter with match register,, four clock sources with prescaler dividers, can be used for periodic wakeup
  - **RTC** — 8-bit modulus counter with binary or decimal based prescaler, three clock sources including one external source, can be used for time base, calendar, or task scheduling functions
  - **KBI** — One keyboard control module capable of supporting 8 × 8 keyboard matrix
  - **IRQ** — External pin for wakeup from low-power modes
- Input/Output
  - 39, 53, or 69 GPIOs
  - 8 KBI and 1 IRQ interrupt with selectable polarity
  - Hysteresis and configurable pullup device on all input pins, configurable slew rate and drive strength on all output pins.
- Package Options
  - 48-pin LQFP, 64-pin LQFP, and 80-pin LQFP

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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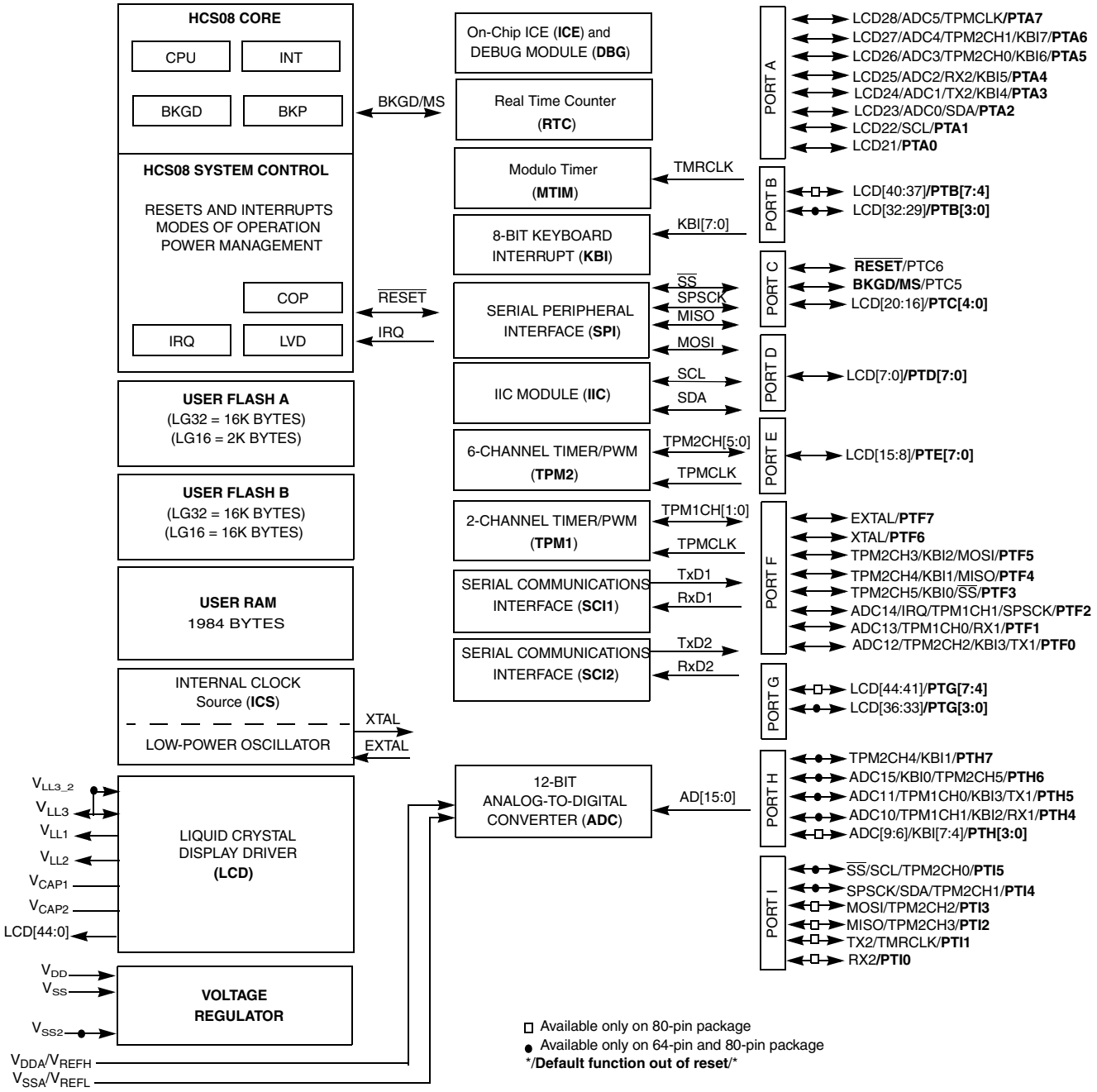


Figure 1. MC9S08LG32 Series Block Diagram

Table 2. Pin Availability by Package Pin-Count

Packages			<-- Lowest **Priority** --> Highest				
80	**64**	**48**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	1	1	PTD7	LCD7	—	—	—
2	2	2	PTD6	LCD6	—	—	—
3	3	3	PTD5	LCD5	—	—	—
4	4	4	PTD4	LCD4	—	—	—
5	5	5	PTD3	LCD3	—	—	—
6	6	6	PTD2	LCD2	—	—	—
7	7	—	PTB3	LCD32	—	—	—
8	8	—	PTB2	LCD31	—	—	—
9	—	—	PTB7	LCD40	—	—	—
10	—	—	PTB6	LCD39	—	—	—
11	—	—	PTB5	LCD38	—	—	—
12	—	—	PTB4	LCD37	—	—	—
13	9	—	PTB1	LCD30	—	—	—
14	10	—	PTB0	LCD29	—	—	—
15	11	7	PTD1	LCD1	—	—	—
16	12	8	PTD0	LCD0	—	—	—
17	13	9	V_{CAP1}	—	—	—	—
18	14	10	V_{CAP2}	—	—	—	—
19	15	11	V_{LL1}	—	—	—	—
20	16	12	V_{LL2}	—	—	—	—
21	17	13	V_{LL3}	—	—	—	—
22	18	14	PTF5	MOSI	KBI2	TPM2CH3	—
23	19	15	PTF4	MISO	KBI1	TPM2CH4	—
24	20	—	PTI5	TPM2CH0	SCL	$\overline{SS}$	—
25	21	—	PTI4	TPM2CH1	SDA	SPSCK	—
26	—	—	PTI3	TPM2CH2	MOSI	—	—
27	—	—	PTI2	TPM2CH3	MISO	—	—
28	—	—	PTI1	TMRCLK	TX2	—	—
29	—	—	PTI0	RX2	—	—	—
30	22	—	PTH7	KBI1	TPM2CH4	—	—
31	23	16	V_{SS}	—	—	—	—
32	24	17	V_{DD}	—	—	—	—
33	25	18	PTF7	EXTAL	—	—	—
34	26	19	PTF6	XTAL	—	—	—
35	27	20	V_{DDA}	V_{REFH}	—	—	—
36	28	21	V_{SSA}	V_{REFL}	—	—	—
37	29	—	PTH6	TPM2CH5	KBI0	ADC15	—
38	30	22	PTF2	SPSCK	TPM1CH1	IRQ	ADC14

2.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	C	Run supply current FEI mode, all modules on	RI_{DD}	20 MHz	3	16.38	27.85	mA	–40 °C to 85 °C
	C						28.05		–40 °C to105 °C
	C			1 MHz		1.67	2.84		–40 °C to 85 °C
	C						2.87		–40 °C to105 °C
	P			20 MHz	5	16.55	28.14	mA	–40 °C to 85 °C
	P						28.35		–40 °C to105 °C
	C			1 MHz		1.77	3.01		–40 °C to 85 °C
	C						3.05		–40 °C to105 °C
2	T	Run supply current FEI mode, all modules off	RI_{DD}	20 MHz	3	11.9	20.25	mA	–40 °C to 85 °C
	T						21.72		–40 °C to105 °C
	T			1 MHz		1.16	1.95		–40 °C to 85 °C
	T						1.98		–40 °C to105 °C
	T			20 MHz	5	12.68	21.56	mA	–40 °C to 85 °C
	T						23.12		–40 °C to105 °C
	T			1 MHz		1.4	2.39		–40 °C to 85 °C
	T						2.41		–40 °C to105 °C
3	T	Wait mode supply current FEI mode, all modules off	WI_{DD}	20 MHz	3	7.9	13.42	mA	–40 °C to 85 °C
	T						13.59		–40 °C to105 °C
	T			1 MHz		0.88	1.49		–40 °C to 85 °C
	T						1.51		–40 °C to105 °C
	P			20 MHz	5	8.13	13.81	mA	–40 °C to 85 °C
	P						13.98		–40 °C to105 °C
	T			1 MHz		1.12	1.91		–40 °C to 85 °C
	T						1.94		–40 °C to105 °C
4	C	Stop2 mode supply current	$S2I_{DD}$	n/a	3	1.1	16.0	µA	–40 °C to 85 °C
	C						39.0		–40 °C to105 °C
	P				5	1.2	18.7	µA	–40 °C to 85 °C
	P						46.1		–40 °C to105 °C
5	C	Stop3 mode supply current No clocks active	$S3I_{DD}$	n/a	3	1.2	22.4	µA	–40 °C to 85 °C
	C						56.2		–40 °C to105 °C
	P				5	1.32	25.5	µA	–40 °C to 85 °C
	P						63.9		–40 °C to105 °C

Table 9. Supply Current Characteristics (continued)

Num	C	Parameter		Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
6	T	Stop2 adders:	RTC using LPO	—	n/a	3	210	—	nA	–40 °C to 105 °C
			RTC using low power crystal oscillator				4.25	—	µA	
			LCD[2] with rbias (Low Gain)				1.2[3]	—		
			LCD[2] with rbias (High Gain)				18[4]	—		
			LCD[2] with Cpump				4.05[3]	—		–40 °C to 85 °C
			RTC using LPO			5	210	—	nA	–40 °C to 105 °C
			RTC using low power crystal oscillator				4.22	—	µA	
			LCD[2] with rbias (Low Gain)				1.5[3]	—		
			LCD[2] with rbias (High Gain)				32[4]	—		
			LCD[2] with Cpump				7.12[3]	—		–40 °C to 85 °C
7	T	Stop3 adders:	RTC using LPO	—	n/a	3	210	—	nA	–40 °C to 105 °C
			RTC using low power crystal oscillator				4.75	—	µA	
			LCD[2] with rbias (Low Gain)				1.2[3]	—		
			LCD[2] with rbias (High Gain)				18[4]	—		
			LCD[2] with Cpump				4.35[3]	—		–40 °C to 85 °C
			RTC using LPO			5	230	—	nA	–40 °C to 105 °C
			RTC using low power crystal oscillator				4.74	—	µA	
			LCD[2] with rbias (Low Gain)				1.5[3]	—		
			LCD[2] with rbias (High Gain)				32[4]	—		
			LCD[2] with Cpump				7.49[3]	—		–40 °C to 85 °C

Table 9. Supply Current Characteristics (continued)

Num	C	Parameter		Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
8	T	Stop3 adders:	EREFSTEN = 1	—	n/a	3	4.58	—	µA	–40 °C to 105 °C
			IREFSTEN = 1				71.7	—		
			LVD				94.35	—		
			EREFSTEN = 1			5	4.61	—	µA	
			IREFSTEN = 1				71.69	—		
			LVD				107.34	—		

1 Typical values are measured at 25 °C. Characterized, not tested.

2 LCD configured for Charge Pump Enabled V_{LL3} connected to V_{DD}.

3 This does not include current required for 32 kHz oscillator.

4 This is the maximum current when all LCD inputs/outputs are used.

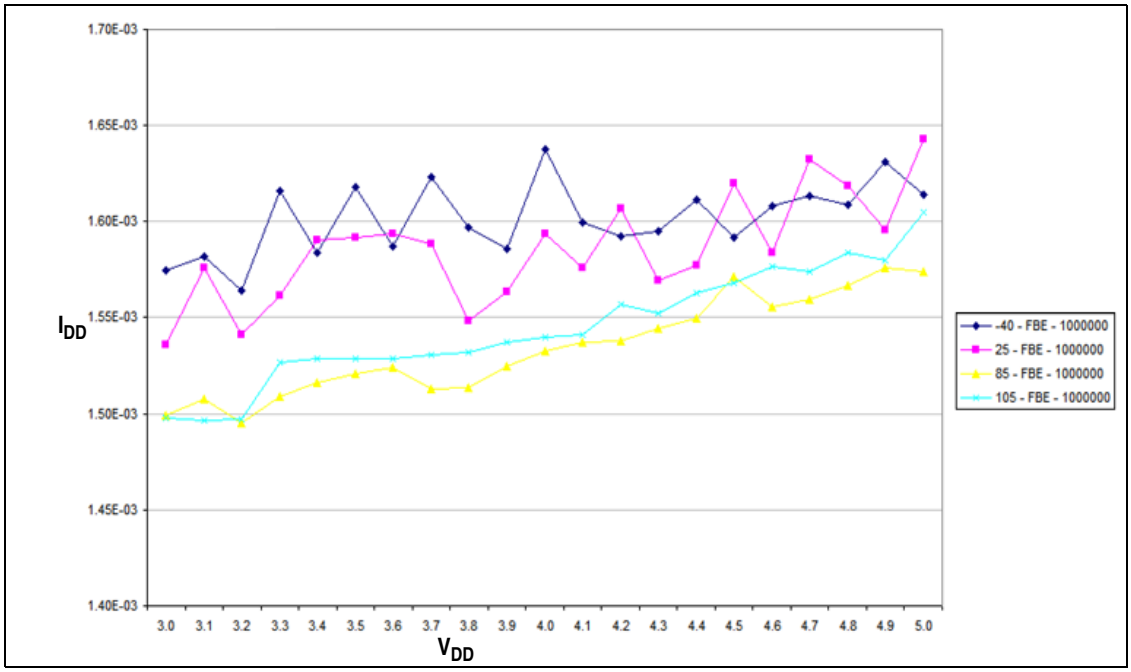


Figure 9. Typical Run I_{DD} for FBE Mode at 1 MHz

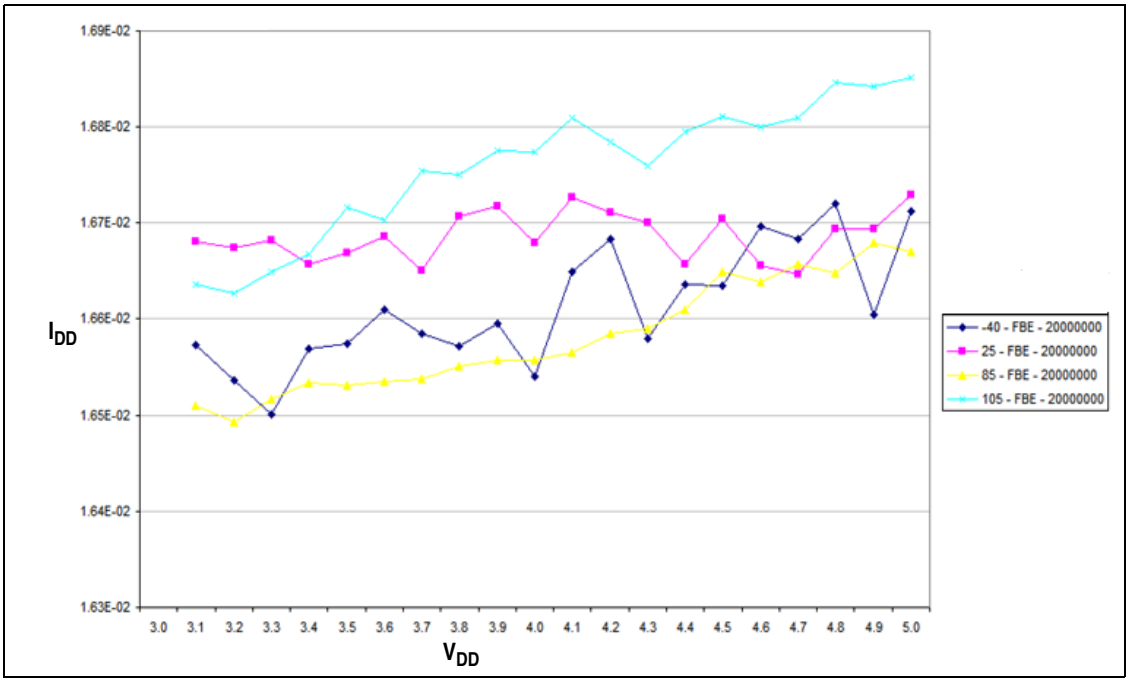


Figure 10. Typical Run I_{DD} for FBE Mode at 20 MHz

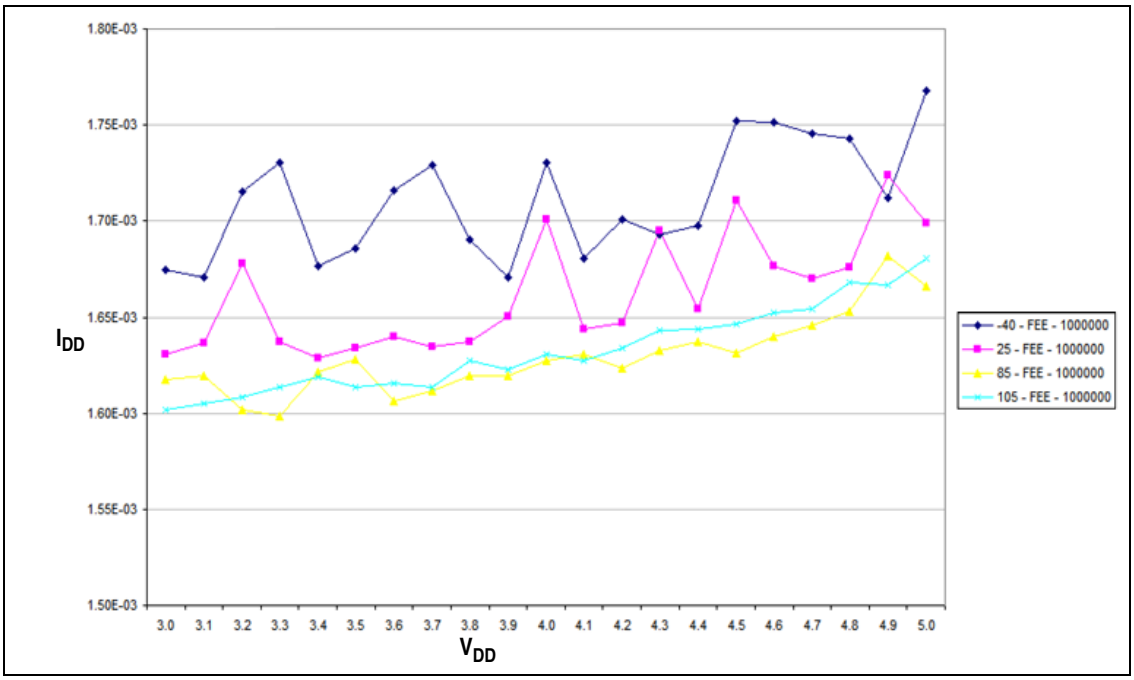


Figure 11. Typical Run I_{DD} for FEE Mode at 1 MHz

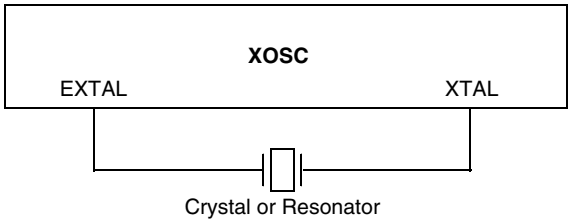


Figure 16. Typical Crystal or Resonator Circuit: Low Range/Low Power

2.9 Internal Clock Source (ICS) Characteristics

Table 11. ICS Frequency Specifications (Temperature Range = –40 °C to 105 °C Ambient)

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
1	P	Average internal reference frequency — factory trimmed at VDD = 5.0 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	C	Average internal reference frequency — user trimmed		f_{int_t}	31.25	—	39.0625	kHz
3	C	Internal reference start-up time		t_{IRST}	—	60	100	µs
4	P	DCO output frequency range — trimmed[2]	Low range (DRS = 00)	f_{dco_t}	16	—	20	MHz
	P		Mid range (DRS = 01)		32	—	40	
5	P	DCO output frequency[2] Reference = 32768 Hz and DMX32 = 1	Low range (DRS = 00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DRS = 01)		—	39.85	—	
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)[3]		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)[3]		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	P	Total deviation of trimmed DCO output frequency over voltage and temperature		Δf_{dco_t}	—	–1.0 to +0.5	±2	$\%f_{dco}$
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 °C to 70 °C[3]		Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	C	FLL acquisition time[3, 4]		$t_{Acquire}$	—	—	1	mS
11	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[5]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This parameter is characterized and not tested on each device.

4 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

5 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in the crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

Table 13. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD})

Num	C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
1	T	Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1	—	I_{DDAD}	—	195	—	µA	—
2	T	Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1	—	I_{DDAD}	—	347	—	µA	—
3	T	Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1	—	I_{DDAD}	—	407	—	µA	—
4	P	Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1	—	I_{DDAD}	—	0.755	1	mA	—
5	—	Supply Current	Stop, Reset, Module Off	IDDAD		0.011	1	µA	—
6	P	ADC Asynchronous Clock Source	High Speed (ADLPC=0)	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
			Low Power (ADLPC=1)		1.25	2	3.3		
7	C	Conversion Time (Including sample time)	Short sample (ADLSMP=0)	t_{ADC}	—	20	—	ADCK cycles	See *ADC chapter in the LG32 Reference Manual* for conversion time variances
			Long sample (ADLSMP=1)		—	40	—		
8	C	Sample Time	Short sample (ADLSMP=0)	t_{ADS}	—	3.5	—	ADCK cycles	
			Long sample (ADLSMP=1)		—	23.5	—		
9	T	Total Unadjusted Error	12-bit mode	E_{TUE}	—	±3.0	—	LSB^2	Includes quantization
	P		10-bit mode		—	±1	±2.5		
	T		8-bit mode		—	±0.5	±1		
10	T	Differential Non-Linearity	12-bit mode	DNL	—	±1.75	—	LSB^2	
	P		10-bit mode[3]		—	±0.5	±1.0		
	T		8-bit mode[3]		—	±0.3	±0.5		
11	T	Integral Non-Linearity	12-bit mode	INL	—	±1.5	—	LSB^2	
	P		10-bit mode		—	±0.5	±1		
	T		8-bit mode		—	±0.3	±0.5		
12	T	Zero-Scale Error	12-bit mode	E_{ZS}	—	±1.5	—	LSB^2	V_{ADIN} = V_{SSAD}
	P		10-bit mode		—	±0.5	±1.5		
	T		8-bit mode		—	±0.5	±0.5		

Table 13. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
13	T	Full-Scale Error	12-bit mode	E_{FS}	—	±1	—	LSB[2]	V_{ADIN} = V_{DDAD}
	P		10-bit mode		—	±0.5	±1		
	T		8-bit mode		—	±0.5	±0.5		
14	D	Quantization Error	12-bit mode	E_Q	—	–1 to 0	—	LSB[2]	—
			10-bit mode		—	—	±0.5		
			8-bit mode		—	—	±0.5		
15	D	Input Leakage Error	12-bit mode	E_{IL}	—	±1	—	LSB[2]	Pad leakage[4] * R_{AS}
			10-bit mode		—	±0.2	±2.5		
			8-bit mode		—	±0.1	±1		
16	C	Temp Sensor Slope	–40 °C to 25 °C	m	—	1.646	—	mV/°C	—
			25 °C to 125°C		—	1.769	—		
17	C	Temp Sensor Voltage	25 °C	V_{TEMP25}	—	701.2	—	mV	—

1 Typical values assume V_{DDAD} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes

4 Based on input pad leakage current. Refer to pad electricals.

2.11 AC Characteristics

This section describes timing characteristics for each peripheral system.

2.11.1 Control Timing

Table 14. Control Timing

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1	D	Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	dc	—	20	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	µs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	66 x t_{cyc}	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	µs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	 t_{ILIH} t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	 t_{ILIH} t_{IHIL}	 100 1.5 x t_{cyc}	 — —	 — —	ns
9	C	Port rise and fall time — (load = 50 pF)[5, 6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	 t_{Rise} t_{Fall}	 — —	 3 30	 — —	ns

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 105 °C.

6 Except for LCD pins in Open Drain mode.

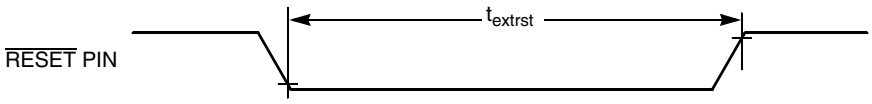


Figure 19. Reset Timing

2.11.3 SPI Timing

Table 16 and Figure 23 through Figure 26 describe the timing requirements for the SPI system.

Table 16. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	 $f_{Bus}/2048$ 0	 $f_{Bus}/2$ $f_{Bus}/4$	Hz
①	D	SPSCK period Master Slave	t_{SPSCK}	 2 4	 2048 —	 t_{cyc} t_{cyc}
②	D	Enable lead time Master Slave	t_{Lead}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}
③	D	Enable lag time Master Slave	t_{Lag}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}
④	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	 $t_{cyc} - 30$ $t_{cyc} - 30$	 1024 t_{cyc} —	 ns ns
⑤	D	Data setup time (inputs) Master Slave	t_{SU}	 15 15	 — —	 ns ns
⑥	D	Data hold time (inputs) Master Slave	t_{HI}	 0 25	 — —	 ns ns
⑦	D	Slave access time	t_a	—	1	t_{cyc}
⑧	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
⑨	D	Data valid (after SPSCK edge) Master Slave	t_v	 — —	 25 25	 ns ns
⑩	D	Data hold time (outputs) Master Slave	t_{HO}	 0 0	 — —	 ns ns
⑪	D	Rise time Input Output	 t_{RI} t_{RO}	 — —	 $t_{cyc} - 25$ 25	 ns ns
⑫	D	Fall time Input Output	 t_{FI} t_{FO}	 — —	 $t_{cyc} - 25$ 25	 ns ns

3 Except pins PHT1, PTH2, PTH3, PTH4, PTH5. See figures below for values.
4 Except pins PTF3, PTH5, PTH4, PHT0, Reset, and BKGD. See figures below for values.

Individual performance of each pin is shown in Figure 27, Figure 28, Figure 29, and Figure 30.

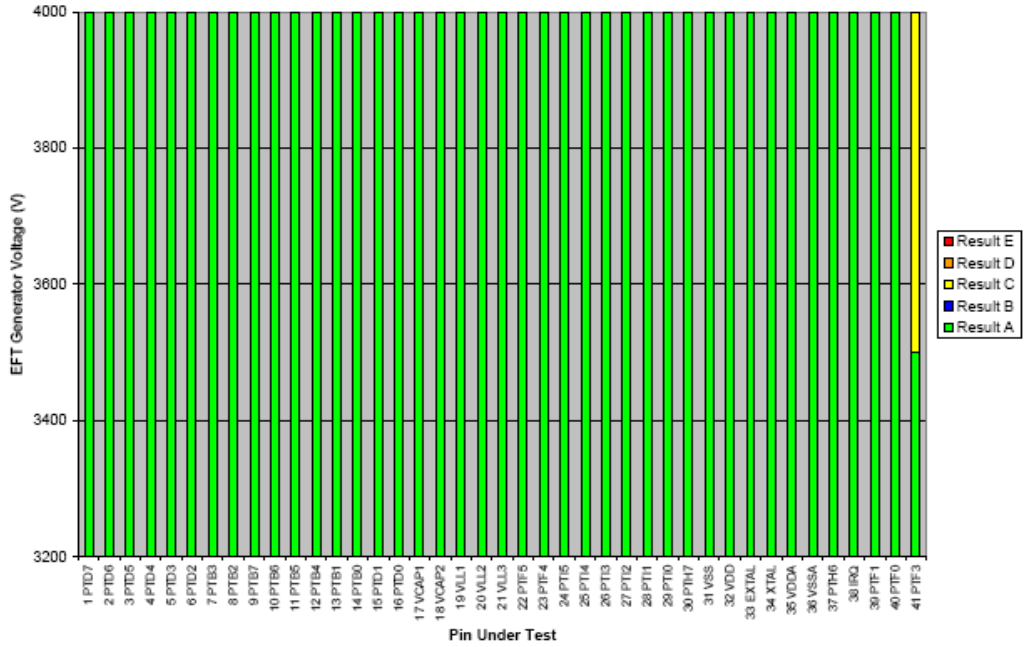
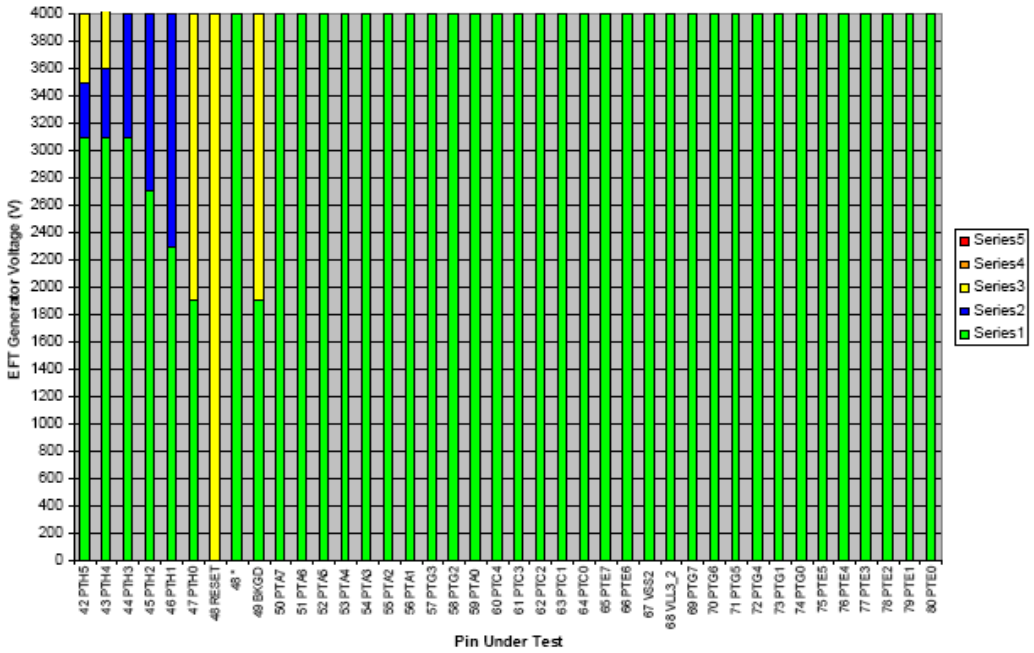


Figure 27. 4 MHz, Positive Polarity Pins 1 – 41



Note:
RESET retested with 0.1 μF capacitor from pin to ground is Class A compliant as shown by 48*.

Figure 28. 4 MHz, Positive Polarity Pins 42 – 80

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23237W
		PAGE: 917A
	DO NOT SCALE THIS DRAWING	REV: E

NOTES:

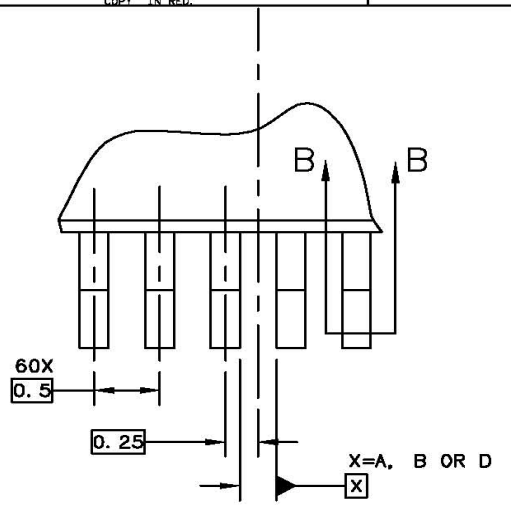
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION : MILIMETER.
3. DATUM PLANE H IS LOCATED AT THE BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUM E, F AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	CASE NUMBER: 917A–03	
	STANDARD: FREESCALE	
	PACKAGE CODE: 8258	SHEET: 3 OF 3

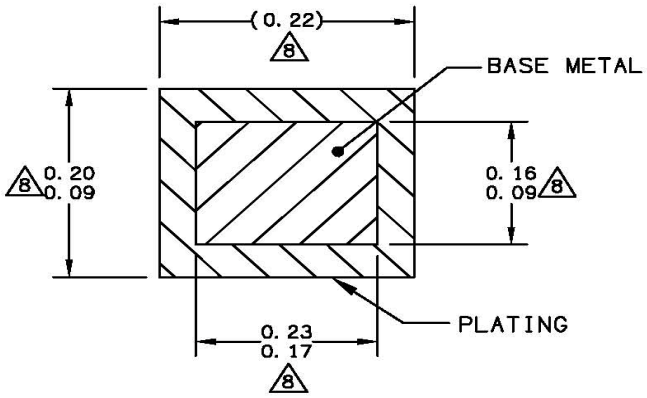
Figure 33. 80-pin LQFP Package Drawing (Case 917A, Doc #98ASS23237W)

freescale semiconductor

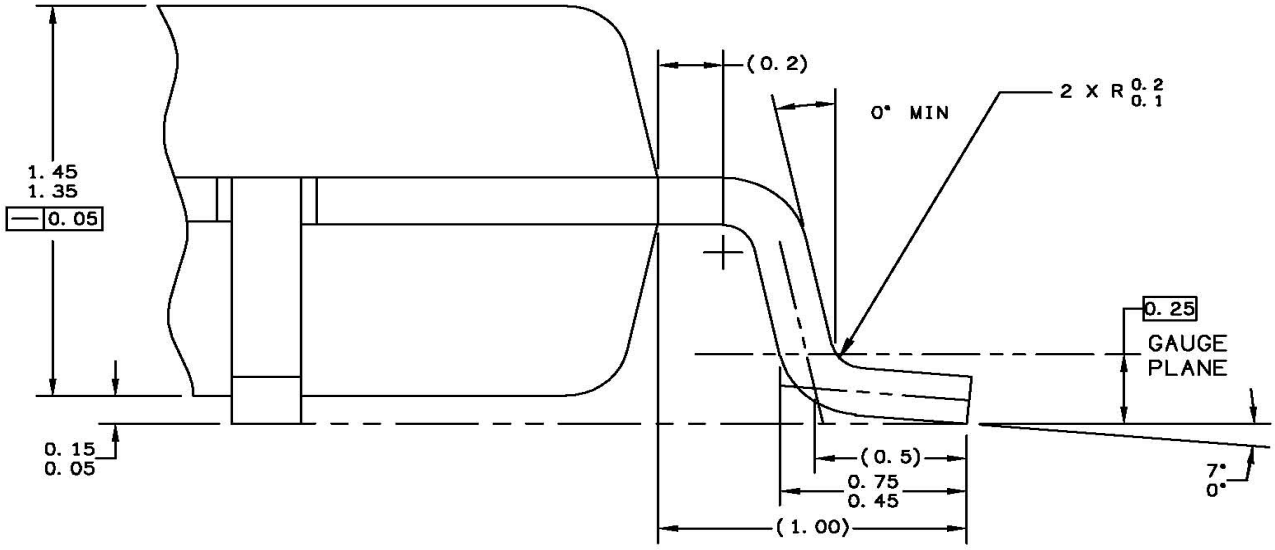
MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23234W
	PAGE: 840F
DO NOT SCALE THIS DRAWING	REV: E



VIEW Y



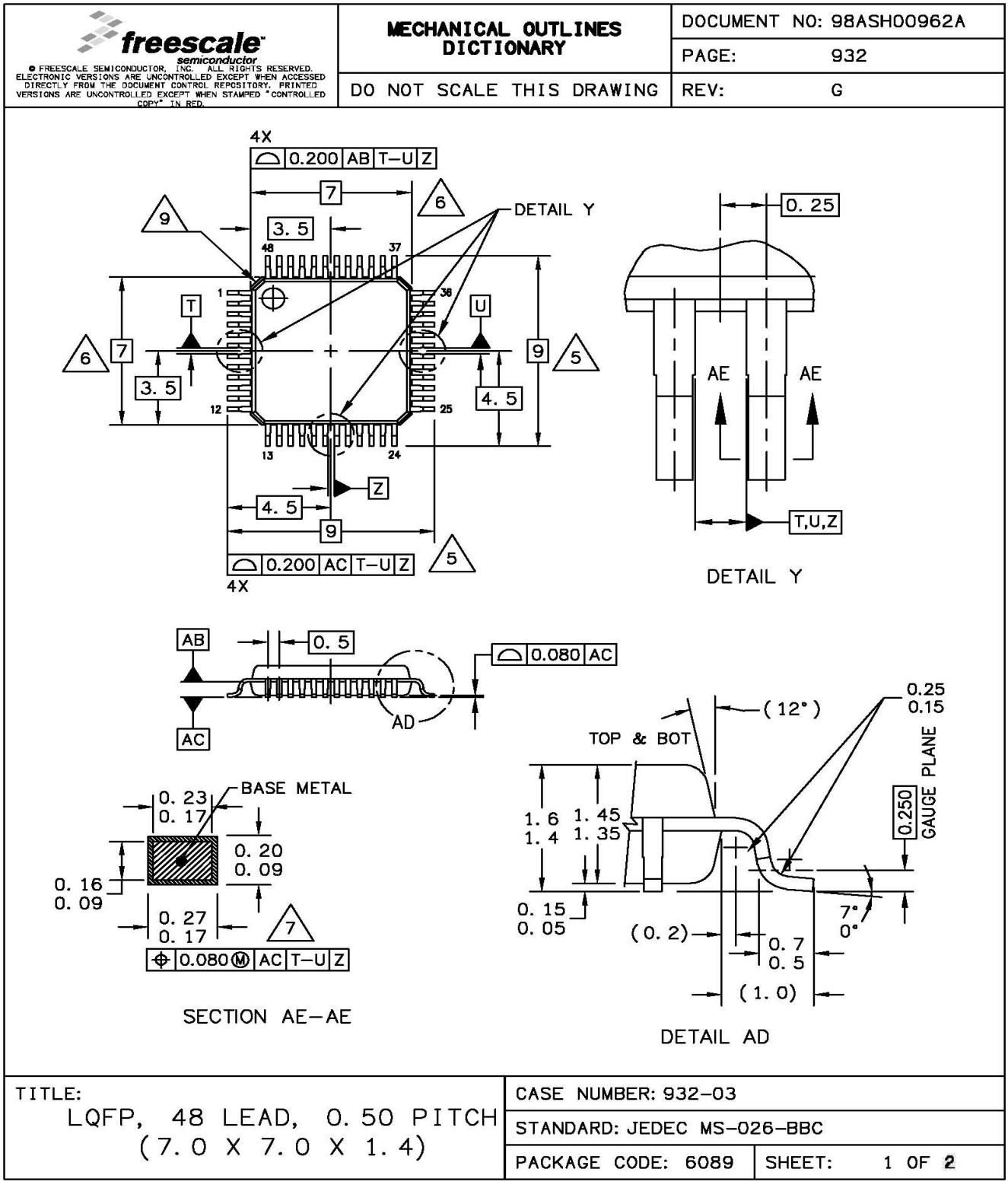
SECTION B–B



VIEW AA

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F–02	
	STANDARD: JEDEC MS–026 BCD	
	PACKAGE CODE: 8426	SHEET: 2 OF 3

4.1.3 48-pin LQFP



freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASH00962A
		PAGE: 932
	DO NOT SCALE THIS DRAWING	REV: G

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

TITLE: LQFP, 48 LEAD, 0.50 PITCH (7.0 X 7.0 X 1.4)	CASE NUMBER: 932–03	
	STANDARD: JEDEC MS–026–BBC	
	PACKAGE CODE: 6089	SHEET: 2 OF 2

Figure 35. 48-pin LQFP Package Drawing (Case 932, Doc #98ASH00962A)

5 Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web are the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://www.freescale.com

The following revision history table summarizes changes contained in this document.

Table 24. Revision History

Revision	Date	Description of Changes
1	8/2008	First Initial release.
2	9/2008	Second Initial Release.
3	11/2008	Alpha Customer Release.
4	2/2009	Launch Release.
5	4/2009	Added EMC Radiated Emission and Transient Susceptibility data in Table 19 and Table 20.
6	4/2009	Updated EMC performance data.
7	8/2009	Updated auto part numbers, changed TCLK, T0CH0, T0CH1, T1CH0, T1CH1, T1CH2, T1CH3, T1CH3, T1CH4, and T1CH5 to TPMCLK, TPM0CH0, TPM0CH1,TPM1CH0, TPM1CH1, TPM1CH2, TPM1CH3, TPM1CH4, and TPM1CH5, and changed the maximum LCD frame frequency to 64 Hz.
8	8/2011	Updated Table “ICS Frequency Specifications (Temperature Range = –40 ×C to 105 ×C Ambient)”. Changed the value of row 8 column C from C to P.
9	9/2011	Updated Table “ICS Frequency Specifications (Temperature Range = –40 ×C to 105 ×C Ambient)”. Removed Footnote from Row 8. Updated the Revision History

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